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Characterization of monolithic CMOS pixel matrices with various pitch fabricated in a 65 nm process

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The performance of monolithic CMOS pixel sensors depends on their fabrication process and especially the feature size which directly drives the pixel size. A consortium led by the CERN EP R&D program, the ALICE experiment and various European projects (AIDAinnova, EURIZON) is investigating the benefits of a 65-nm CMOS imager process to design a new generation of pixel sensors. These developments target a first application for an upgraded version of the inner layers (ITS3) of the ALICE experiments and foster further studies for detector including those for future e+e- colliders that are still currently unmatched by any technology.

Two fabrications of a variety of prototype sensors already took place, in 2020 and 2022. This contribution reports on the characterization of the first version of some of them, the CE-65 sensor family. They include analogue output matrices featuring 2048 (or 1536) pixels with either 15-μm or 25-μm pixels. Three versions of the sensing node were fabricated in order to modify the charge sharing between pixels. Sensors were irradiated to non-ionizing fluences between 10^{13} and 10^{16} n_{eq}/cm^2 as well to 100 and 500 Mrad ionizing radiations.

Illumination with 55Fe source allowed to estimate the equivalent collection node capacitance and its pixel-to-pixel fluctuation, as well as the leakage current before and after irradiation. Non-irradiated sensors were tested in a 10-GeV electron beam to study in detail the charge sharing among pixels and extract the sensor detection efficiencies as well as their position resolutions. The evolution of the latter with digitization strategies, simulated from the data, was also investigated in order to explore the potential of pixels with binary or few bits output, designed in this 65-nm process.

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