Characterization of monolithic CMOS pixel matrices with various pitch fabricated in a 65 nm process

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On behalf of ALICE ITS3

PICSEL

C4PI-Platform

Outline

- Motivations for TPSCo 65 nm technology
- First submission in TPSCo 65 nm CIS process
- Doping variants and experimental set-up
- Impact of process modification on sensor performances
- Impact of pixel pitch on sensor performances
- Summary

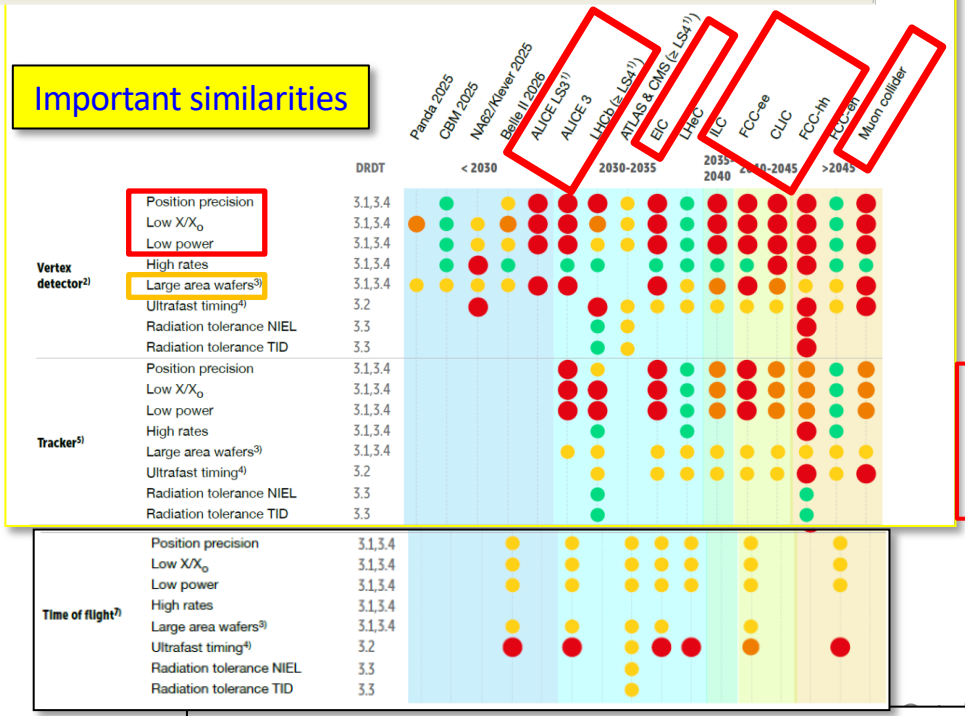
Motivations for exploring the TPSCO 65 nm process

ECFA recognizes the need for the experimental and theoretical communities involved in physics studies, experiment designs and detector technologies at future Higgs factories to gather. ***ECFA supports a series of workshops*** *with the aim to* ***share challenges and expertise, to explore synergies in their efforts*** *and to respond coherently to this priority in the European Strategy for Particle Physics (ESPP).*

Goal: bring the entire e^+e^- Higgs factory effort together, foster cooperation across various projects; collaborative research programmes are to emerge

K. Jakobs, FCC Physics Workshop, Feb 2022

Important similarities



Spatial resolution requirement
- Higgs Factories : 3 um
- Alice ITS3 : 5 um

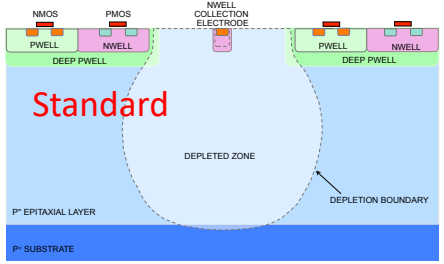
- Low material budget : 0.05 to 0.15 % X_0 per layer
- Low Power consumption (< 100 mW/cm²)

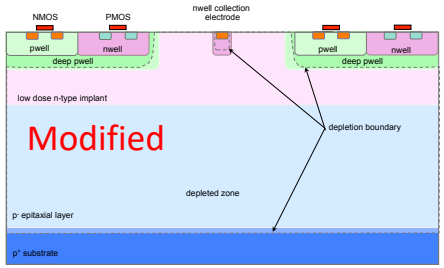
compatible with air cooling.

J. Baudot, 2nd AIDANOVA annual meeting, 2023

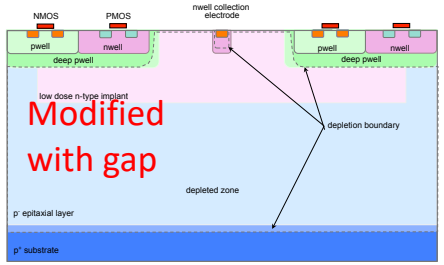
TPSCo 65 nm: benefits & specificities

- Benefits : 65 nm vs 180 nm
  - Better spatial resolution due to smaller feature size
  - Larger wafers : 300 mm vs 200 mm => final sensor : 27x9 cm^2
  - Lower power supply : 1.2 V vs 1.8 V => Low power consumption
  - Lower material budget : thinner sensitive layer (~$10\mu m$)
- Provides 2D stitching
- 7 metal layers
- Process modifications for full depletion:
  - Standard (no modifications)
  - Modified (low dose n-type implant)
  - Modified with gap (low dose n-type implant with gaps)





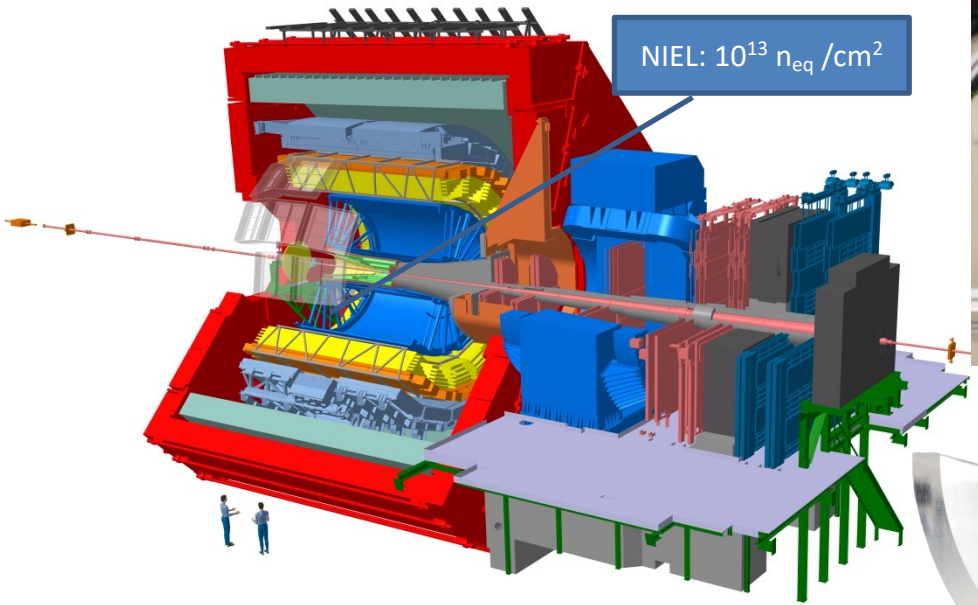
https://doi.org/10.1016/j.nima.2017.07.046

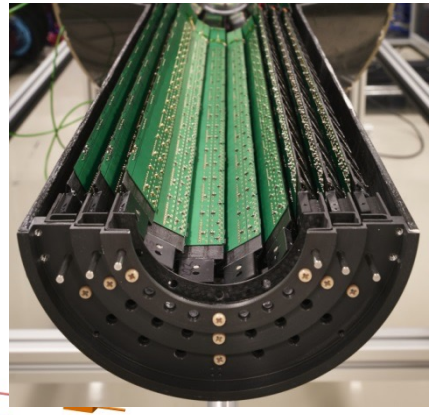


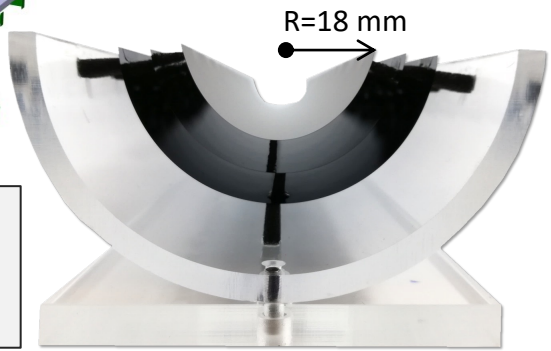
https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013

ALICE detector LS3 upgrade: ITS2 (180 nm) → ITS3 (65 nm)

R. Ricci, PSD 2023







ALICE – general purpose detector at LHC:
- Tracking (100 MeV/c – 100 GeV/c)
- Particle identification: π, K, p, e (0.1 – 50 GeV/c)

ITS2:

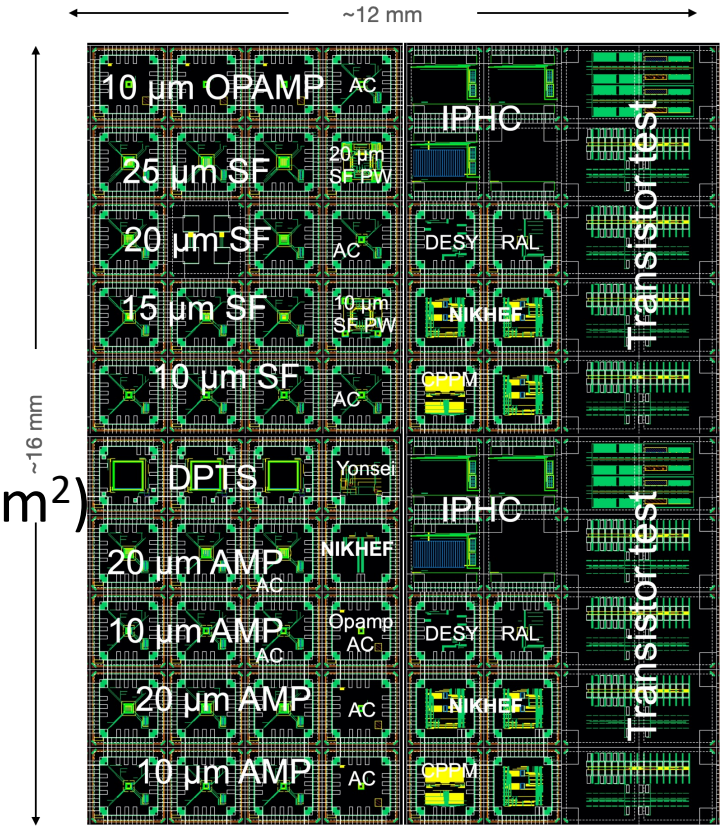
(S.Beolé, iWoRiD 2022)
- 7 layers of MAPS
- TJ 180 nm CMOS
- 12.5 Giga pixels
- Pixel size: 27×29 µm^2
- Water cooling
- **0.3 % X_0 / inner layer**

ITS3

(M. Šuljić, iWoRiD 2023)
- 4 outer layers of ITS2
- 3 new fully cylindrical inner layers
  - Sensor size up to 27×9 cm
  - Thickness <= 50 µm
  - No FPCs
  - Air cooling in active area
- **0.05 % X_0 / inner layer**

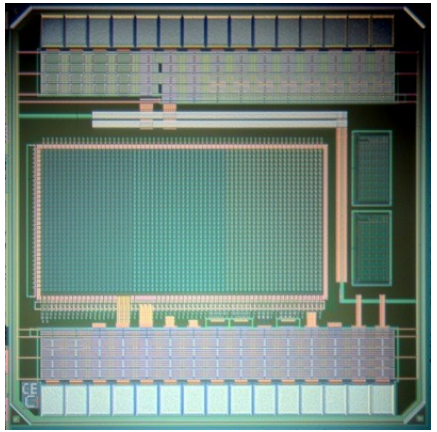
First Test Submission : MLR1

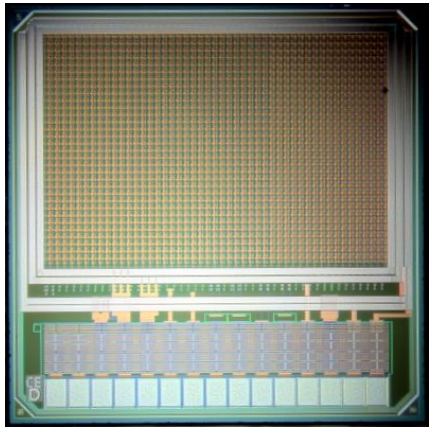
- Submitted in December 2020
- Main goals:
  - Learn technology features
  - Characterize charge collection
  - Validate radiation tolerance
- Each reticle (12×16 mm^2):
  - 10 transistor test structures (3×1.5 mm^2)
  - 60 chips (1.5×1.5 mm^2)
    - Analogue blocks
    - Digital blocks
    - **Pixel prototype chips: APTS, CE65, DPTS**



CE65 : Circuit Exploratoire 65 nm

- 2 matrix sizes
  - 64×32 with 15 µm pitch
  - 48×32 matrix with 25 µm pitch
- Rolling shutter readout (50 µs integration time)
- 3 in-pixel architectures:
  - AC-coupled amplifier
  - DC-coupled amplifier
  - Source follower
- 4 chip variants:
  - **Standard process 15 µm pitch**
  - Modified process 15 µm pitch
  - **Modified process with gaps 15 µm pitch**
  - Standard process 25 µm pitch
- Fabrication in September 2021
- Presented results from CERN PS beam test : May 2022





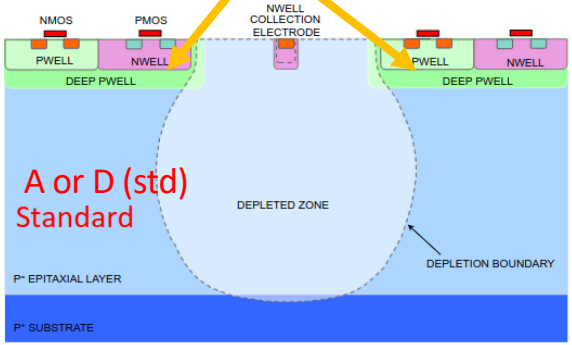
1.5×1.5 mm^2

CE65 variants

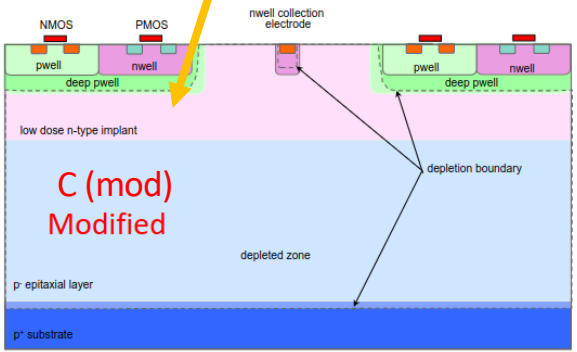
Variant	Process	Pitch	Matrix	Sub-matrix
CE65-A	std	15μm	64×32	AC/21, DC/21, SF/22
CE65-B	mod_gap	15μm	64×32	AC/21, DC/21, SF/22
CE65-C	mod	15μm	64×32	AC/21, DC/21, SF/22
CE65-D	std	25μm	48×32	AC/16, DC/16, SF/16

Pixel pitch impact was evaluated on standard process only

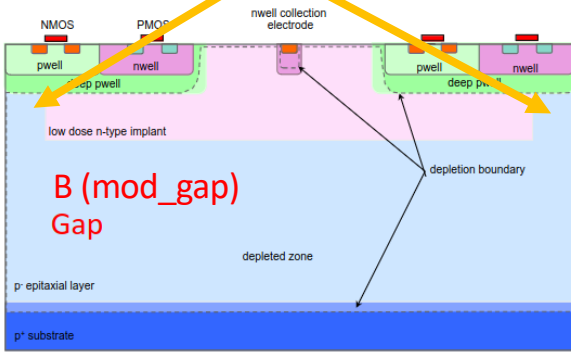
Prevent circuitry's nwells from collecting charge



To obtain a full depletion



To overcome the weak electric field near the edges



Experimental beam test setup

Telescope:

Reference Arms : 4 ALPIDE planes for track reconstruction

DUT : CE65

TRG : DPTS

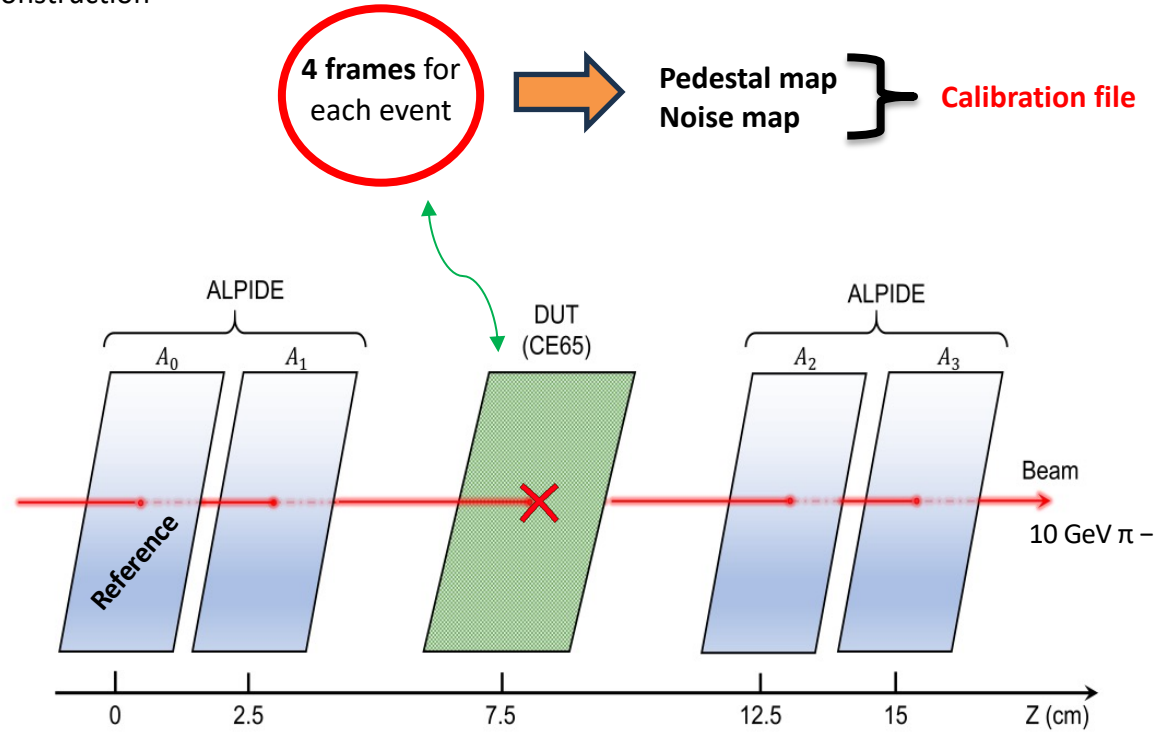
Test beam:

May 2022 at CERN-PS

Data acquisition:
EUDAQ2
Event reconstruction algorithm and data analysis framework:
Corryvreckan

Noise run-**Beam** run:
correlated double sampling method (**CDS**)

Support provided by Alice Collaboration



Corryvreckan analysis parameters (A & D, HV = 10)

- Tracking: spatial cut at $80\mu m$ and $\chi^2/Ndf < 1$ and for DUT association
- Clustering: Set 2 Thresholds and calculate position by **centre of gravity** for 3x3 window around the seed

SF: seeding charge > 150 ADCu , SNR>3
AC: seeding charge > 500 ADCu, SNR>3
DC: seeding charge > 500 ADCu, SNR>3

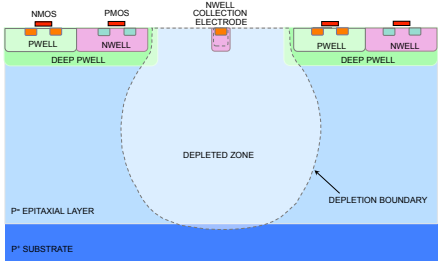
} **Prepared pedestal and noise maps**

- Edge: only use cluster containing **3x3 pixels**, and drop track with interception at **2 pixels** to DUT edge.

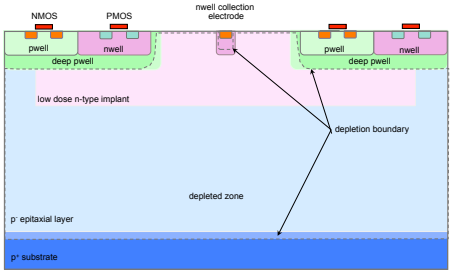
- Seeding method: **multi** (probability of having multiple clusters per event)

Process modification impact

S. Senyukov, iWoRiD 2022

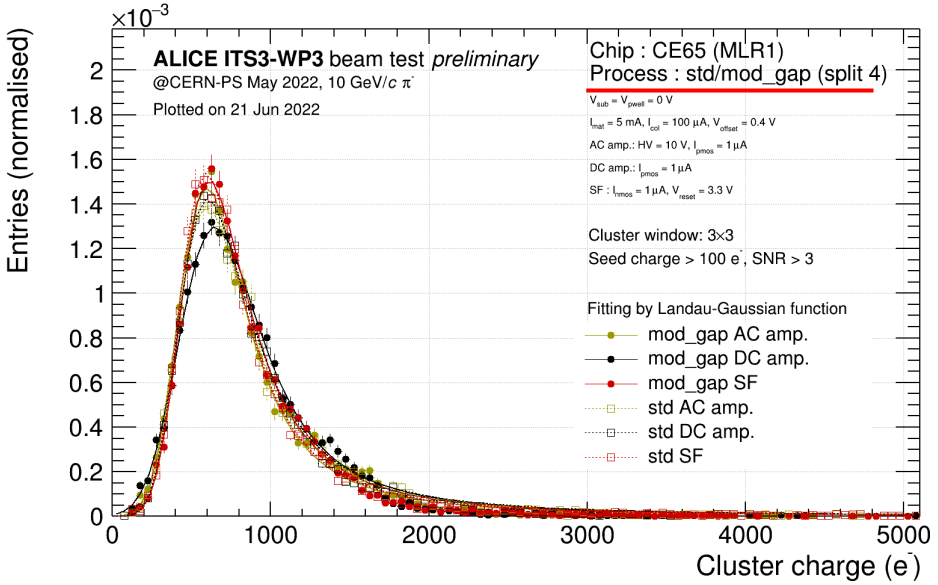


Standard

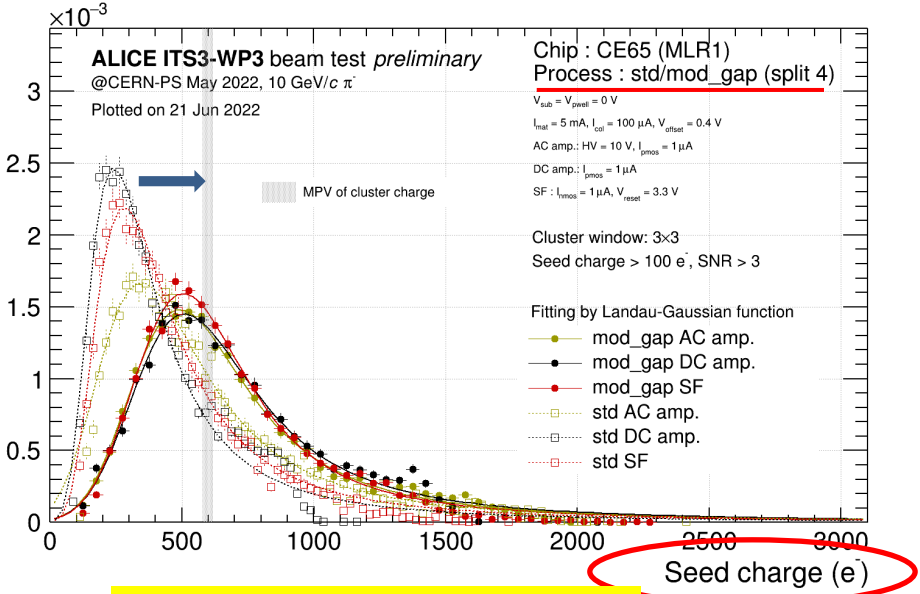


Modified with gap

Modified process effective for depletion

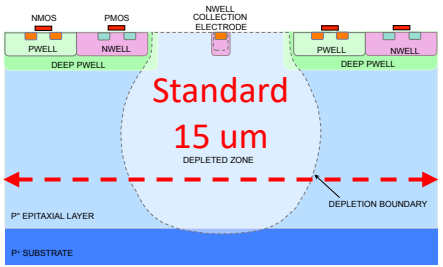


Cluster charge is not affected by process modification

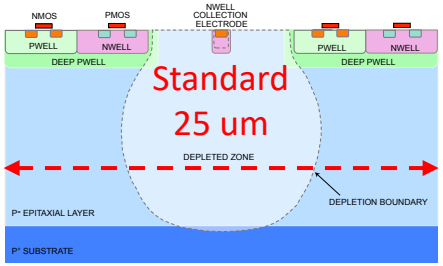


Seed charge is affected by process modification

Pixel pitch impact



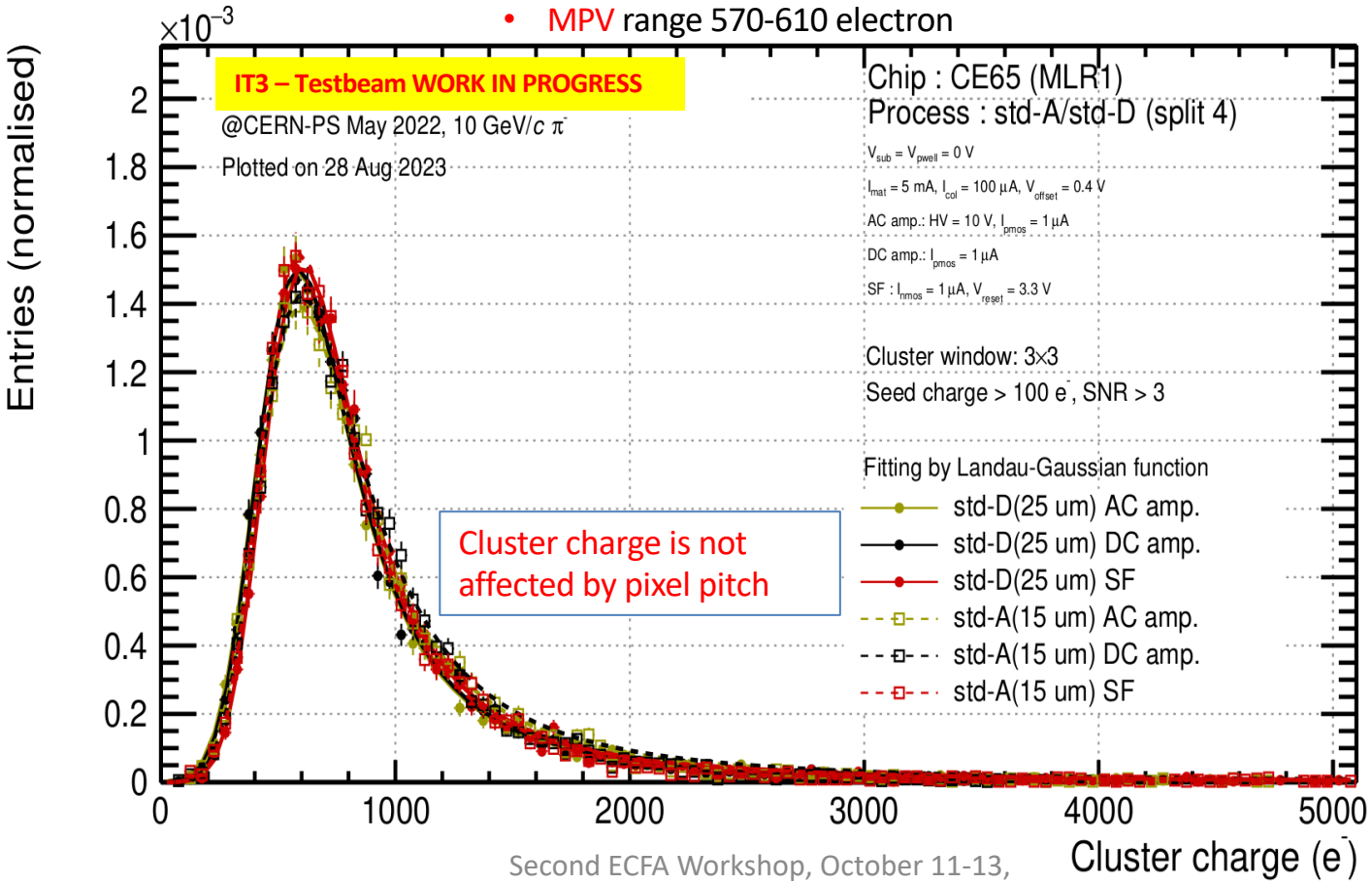
A



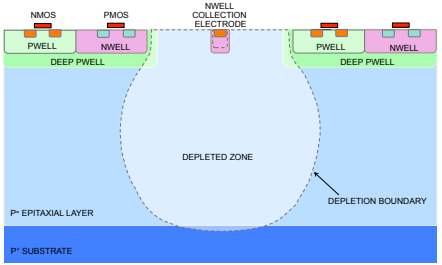
D

Cluster charge

- MPV range 570-610 electron



Pixel pitch evaluation for standard process only



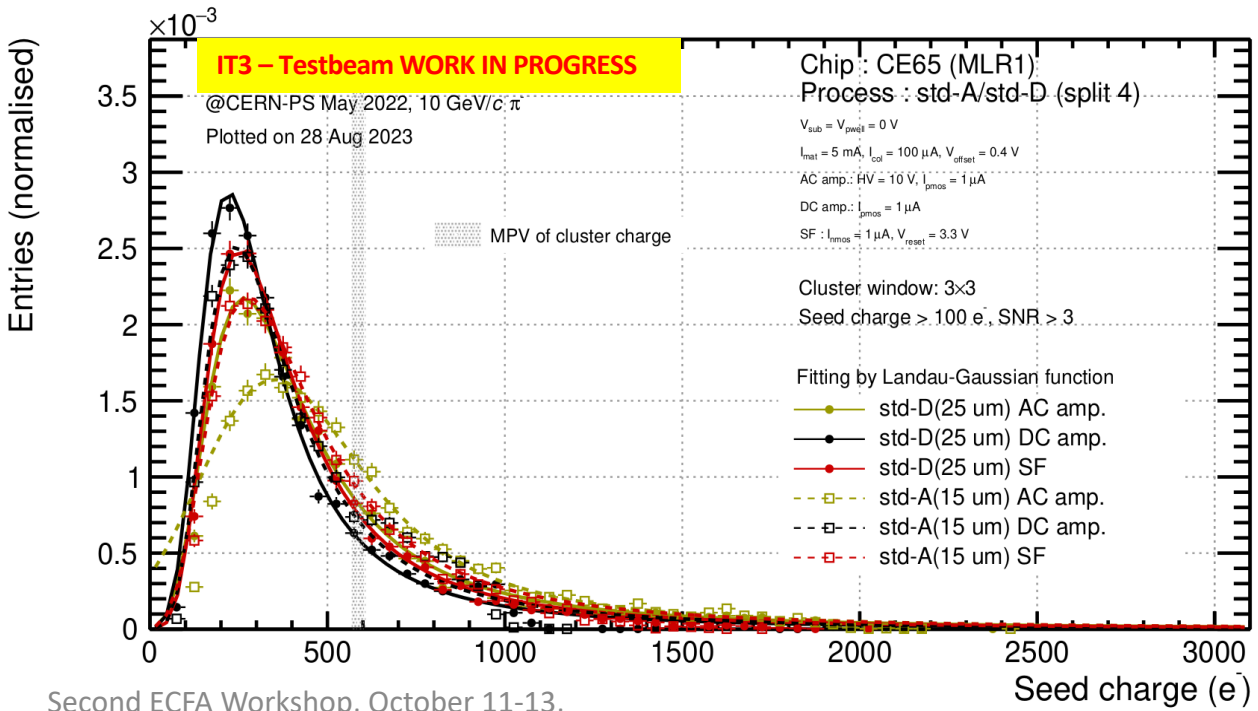
Seed charge

- Seed peaks

Charge sharing increase

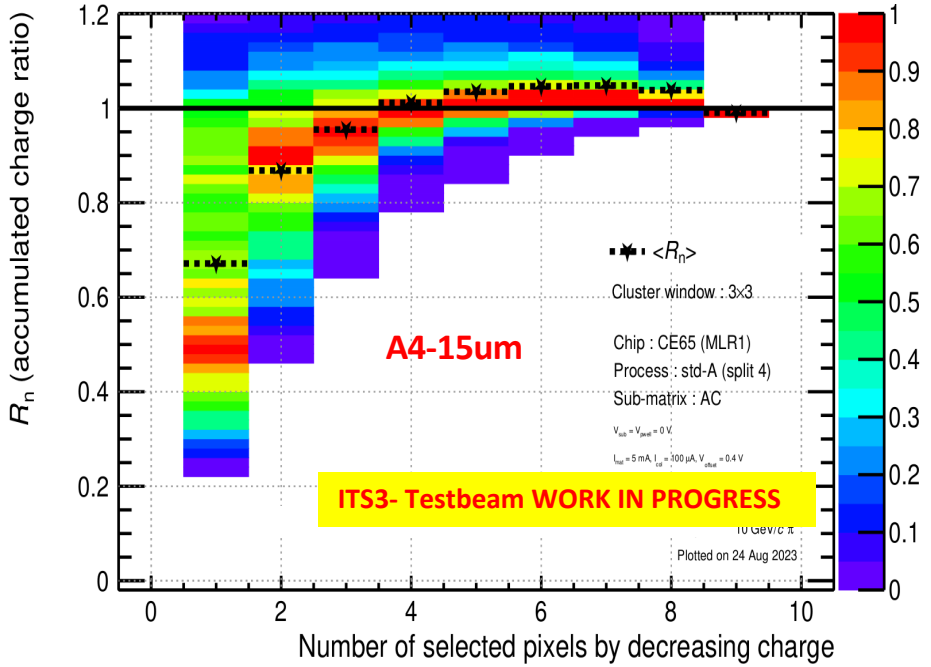
Charge sharing increase

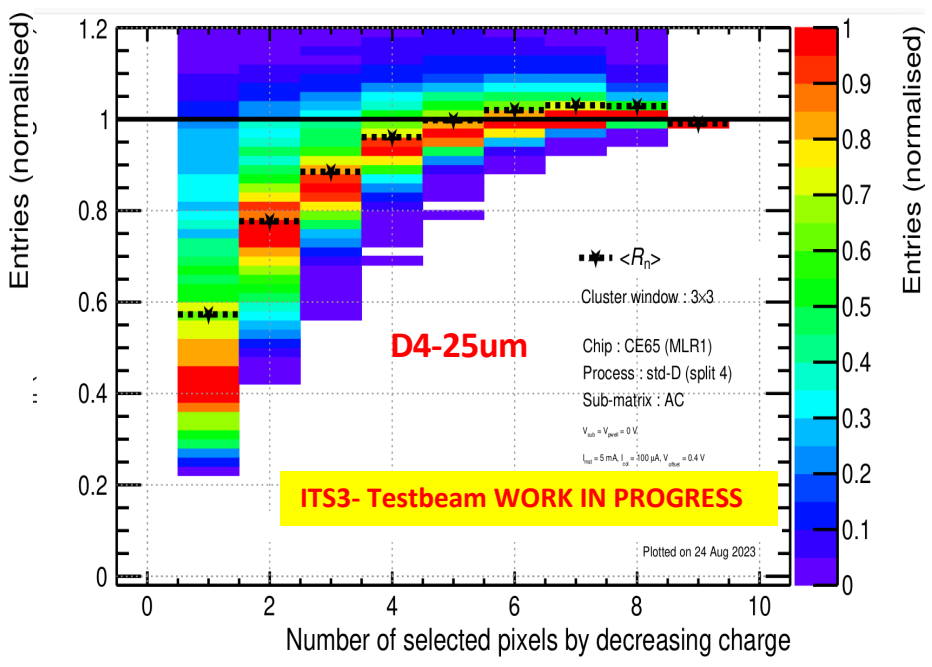
	A4-std 15 um	D4-std 25 um
AC	311	284
SF	297	269
DC	261	232



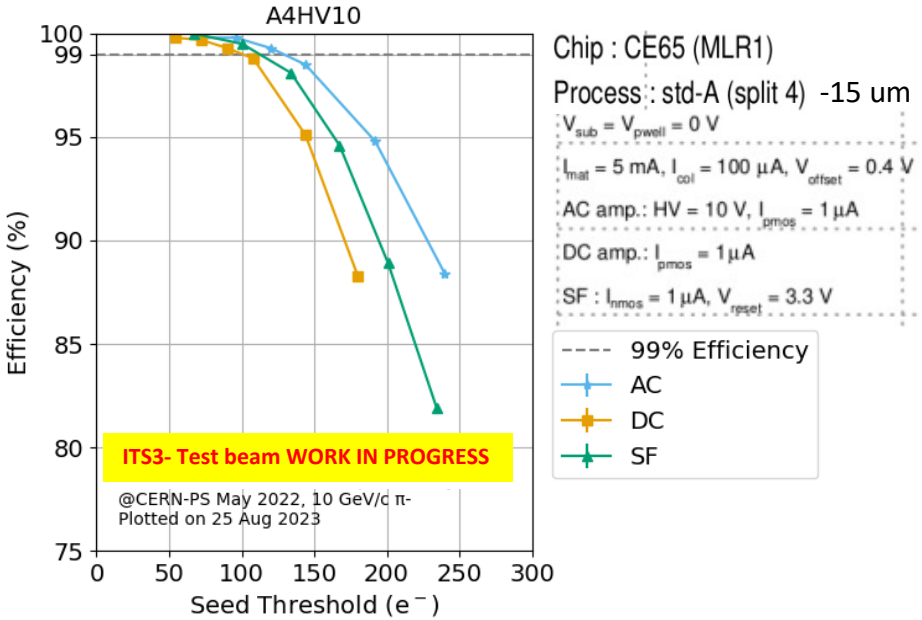
Charge sharing

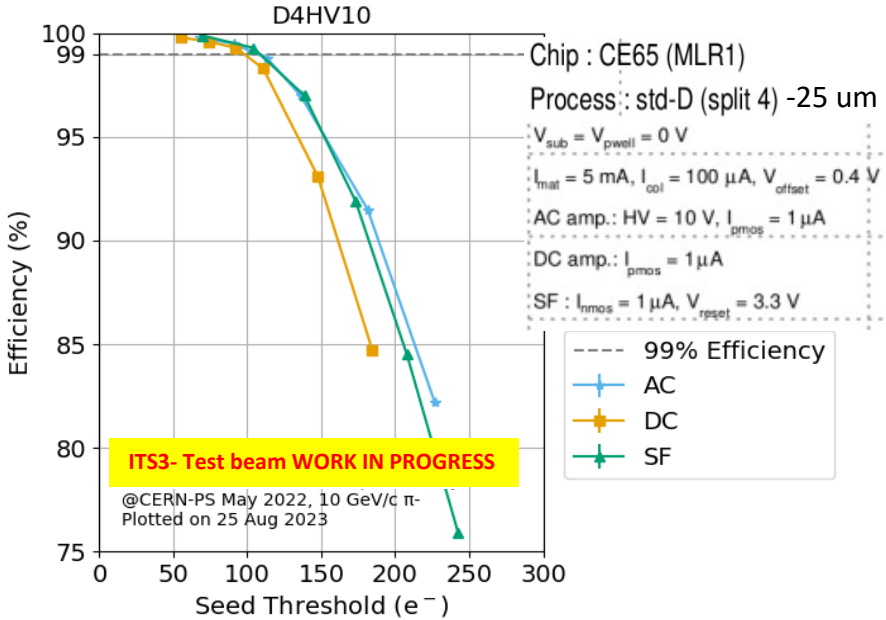
- 4 pixels contain all cluster charge for AC submatrix in A4-15um where it needs 5-6 pixels for D4-25um.
- Seed pixel contains: **more** then 60% in average for A4
  a little bit **less** then 60% in average for D4



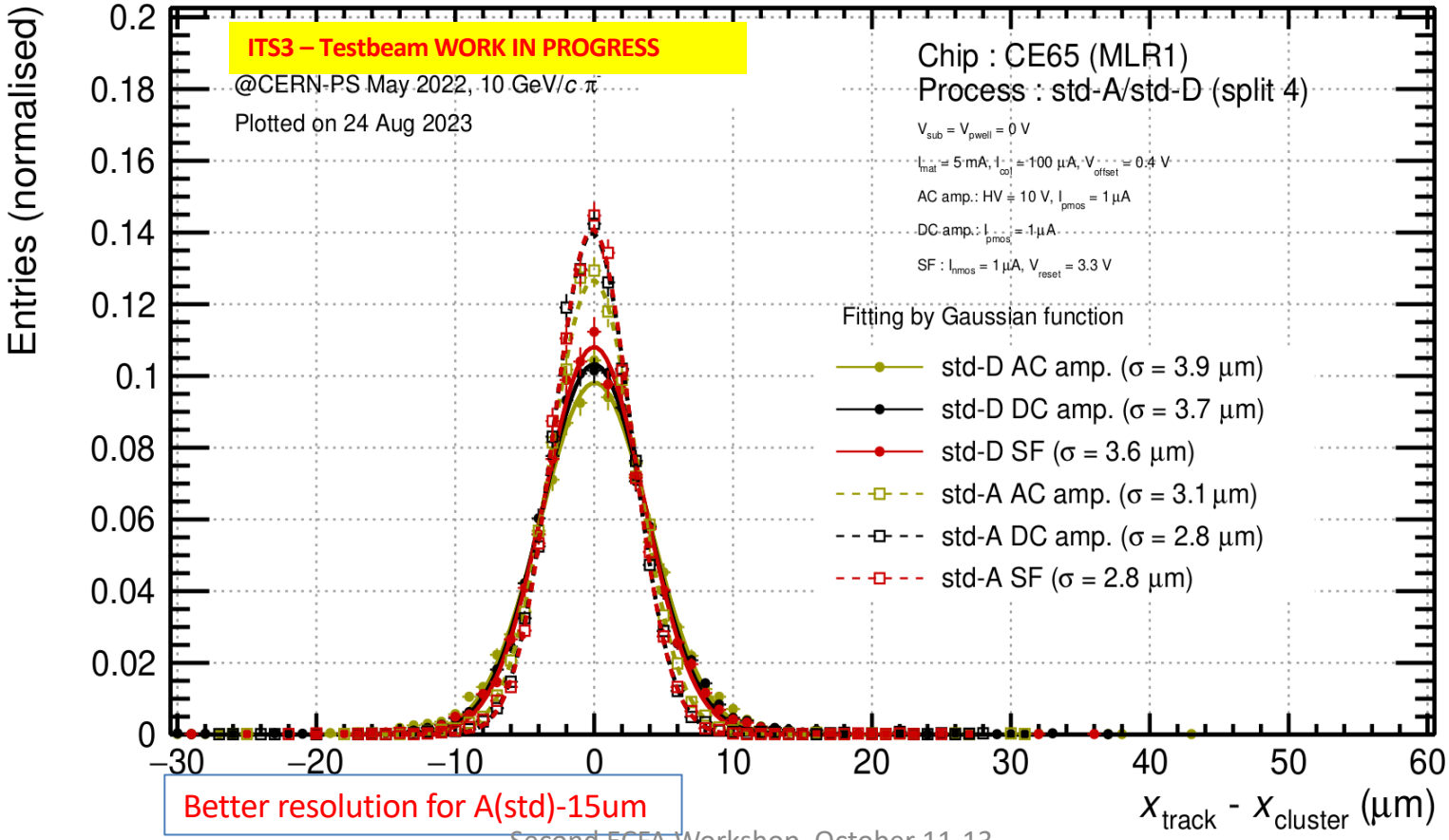


Detection efficiency





Residual

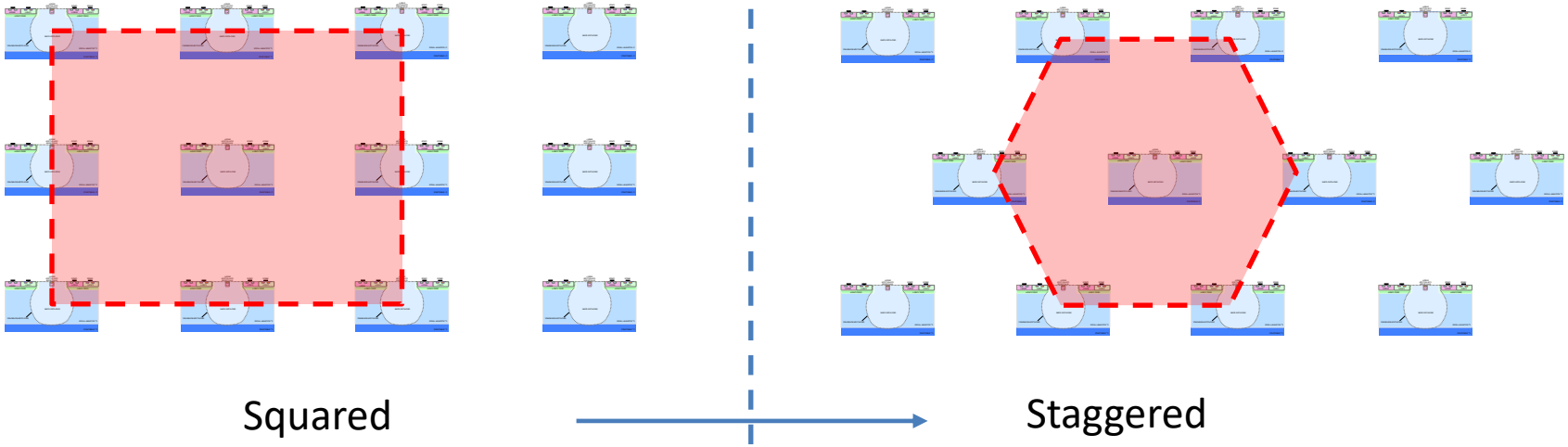

ITS3 – Testbeam WORK IN PROGRESS
@CERN-PS May 2022, 10 GeV/c π
Plotted on 24 Aug 2023
Chip : CE65 (MLR1)
Process : std-A/std-D (split 4)
$V_{sub} = V_{pwell} = 0$ V
$I_{mat} = 5$ mA, $I_{col} = 100$ µA, $V_{offset} = 0.4$ V
AC amp.: HV = 10 V, $I_{pmos} = 1$ µA
DC amp.: $I_{pmos} = 1$ µA
SF : $I_{nmos} = 1$ µA, $V_{reset} = 3.3$ V
Fitting by Gaussian function
std-D AC amp. (σ = 3.9 µm)
std-D DC amp. (σ = 3.7 µm)
std-D SF (σ = 3.6 µm)
std-A AC amp. (σ = 3.1 µm)
std-A DC amp. (σ = 2.8 µm)
std-A SF (σ = 2.8 µm)
Entries (normalised)
$x_{track} - x_{cluster}$ (µm)
Better resolution for A(std)-15um

Summary

- Charge sharing is more significant in larger pitch pixel (standard process) : diffusion dominate depletion (D vs A)!
- As expected, better resolution is achieved for the pixel of 15 um (w.r.t. 25 um : ~1 um improvement).
- Ongoing work on efficiency evaluation confirms the trend of the charge sharing w.r.t pixel pitch.
- Approval of TPSCo 65 nm technology for HEP is on the rails !

On going and future work

- ER1 :
  - ✓ Submitted end 2022.
  - ✓ Received last month (August 2023) and first tests on going.
- Various pitch sizes : 18 and 22 um.
- Diode arrangement and its impact on share sharing (AC pixel).



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