

# Silicon detectors for tracking and vertexing

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# Outline

- Vertex and tracker requirements
- Detector concepts
- DRDT and WGs
- R&D in progress
- Summary

**APOLOGIES**  
**if your favorite R&D is not presented !!**

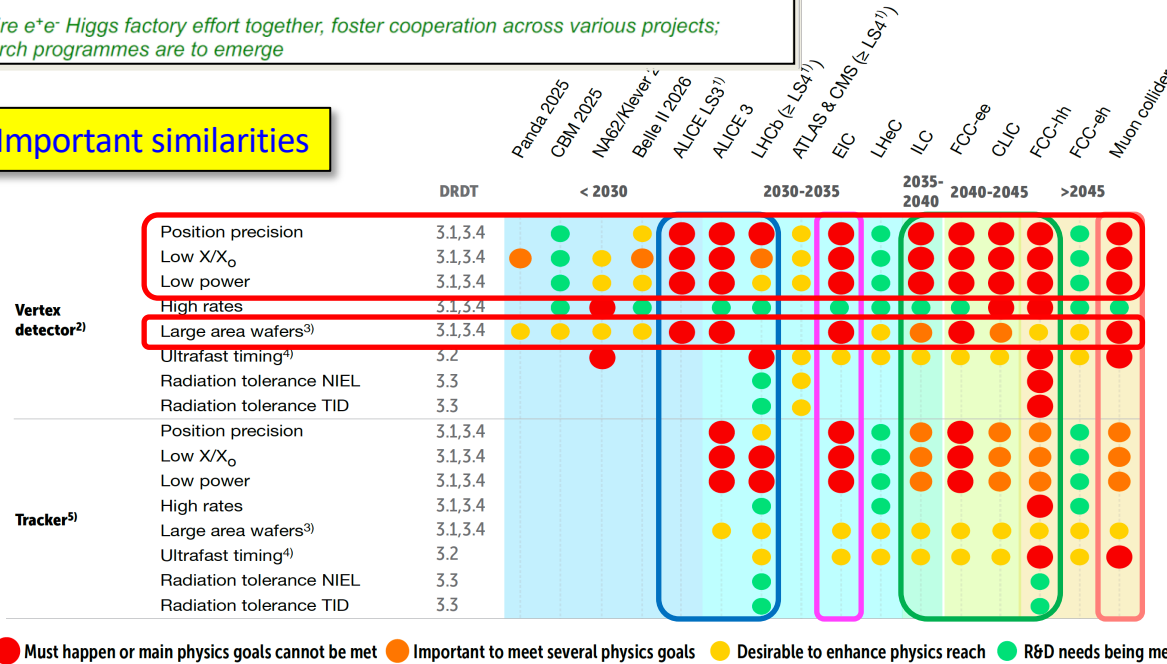
# ECFA recommendation & synergies

ECFA recognizes the need for the experimental and theoretical communities involved in physics studies, experiment designs and detector technologies at future Higgs factories to gather. **ECFA supports a series of workshops** with the aim to **share challenges and expertise, to explore synergies in their efforts** and to respond coherently to this priority in the European Strategy for Particle Physics (ESPP).

[K. Jakobs, FCC Physics Workshop, Feb 2022](#)

Goal: bring the entire  $e^+e^-$  Higgs factory effort together, foster cooperation across various projects; collaborative research programmes are to emerge

## Important similarities



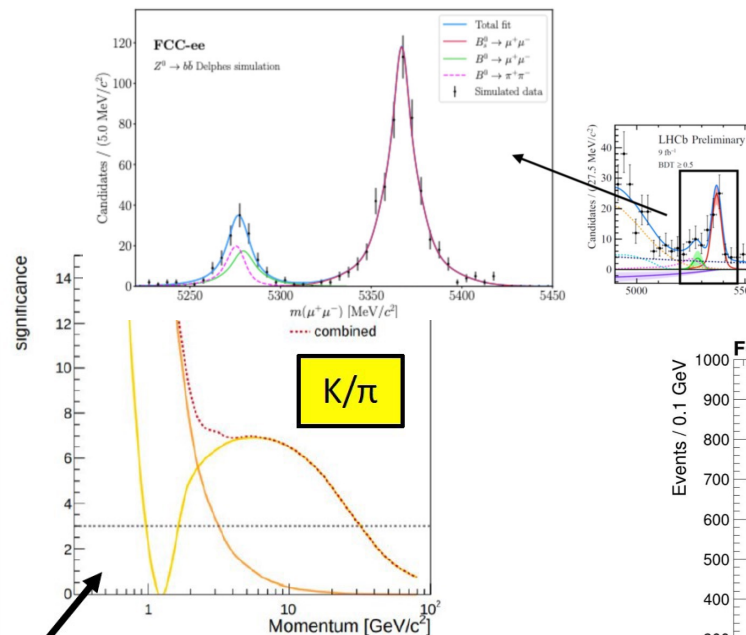
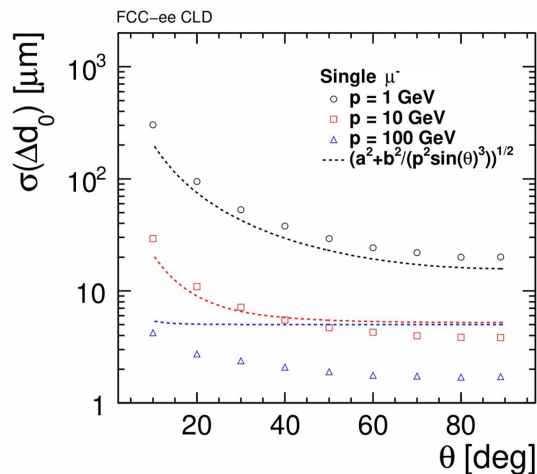
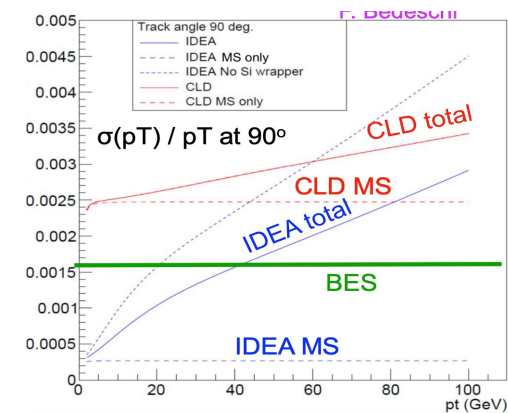
[ECFA 2021: R&D Detector Roadmap](#)

# Requirements

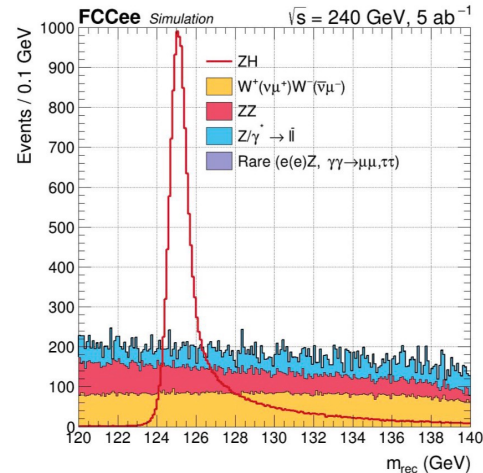
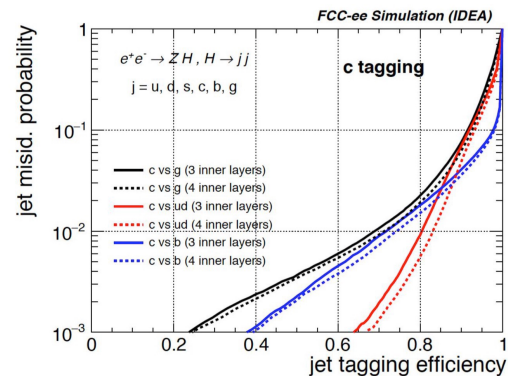
"Technical" Start Date of Facility (This means, where the dates are not known, the earliest technically feasible start date is indicated - such that detector R&D readiness is not the delaying factor)				< 2030				2030-2035				2035 - 2040	2040-2045		> 2045				
				Panda 2025	CBM 2025	NA62/Kleevr 2025	Belle II 2026	ALICE LS3 <sup>1)</sup>	ALICE3	LHCb ( $\geq$ LS4) <sup>1)</sup>	ATLAS/CMS ( $\geq$ LS4) <sup>1)</sup>	EIC	LHeC	IILC <sup>2)</sup>	FCC-ee	CLIC <sup>2)</sup>	FCC-hh	FCC-eh	Muon Collider
Vertex Detector <sup>3)</sup>	MAPS Planar/3D/Passive CMOS LGADs	DRDT 3.1 DRDT 3.4	Position precision $\sigma_{hit}$ ( $\mu\text{m}$ )		$\approx$ 5		$\approx$ 5	$\approx$ 3	$\approx$ 3	$\approx$ 10	$\approx$ 15	$\approx$ 3	$\approx$ 3	$\approx$ 3	$\approx$ 7	$\approx$ 5	$\approx$ 5		
			X/X <sub>0</sub> (%/layer)	$\approx$ 0.1	$\approx$ 0.5	$\approx$ 0.5	$\approx$ 0.1	$\approx$ 0.05	$\approx$ 0.05	$\approx$ 1		$\approx$ 0.05	$\approx$ 0.1	$\approx$ 0.05	$\approx$ 0.05	$\approx$ 0.2	$\approx$ 1	$\approx$ 0.1	$\approx$ 0.2
			Power (mW/cm <sup>2</sup> )		$\approx$ 60			$\approx$ 20	$\approx$ 20			$\approx$ 20		$\approx$ 20	$\approx$ 20	$\approx$ 50			
			Rates (GHz/cm <sup>2</sup> )		$\approx$ 0.1	$\approx$ 1	$\approx$ 0.1		$\approx$ 0.1	$\approx$ 6		$\approx$ 0.1	$\approx$ 0.1	$\approx$ 0.05	$\approx$ 0.05	$\approx$ 5	$\approx$ 30	$\approx$ 0.1	
			Wafers area (") <sup>4)</sup>					12	12			12				12			12
		DRDT 3.2	Timing precision $\sigma_t$ (ns) <sup>5)</sup>	10		$\approx$ 0.05	100		25	$\approx$ 0.05	$\approx$ 0.05	25	25	500	25	$\approx$ 5	$\approx$ 0.02	25	$\approx$ 0.02
		DRDT3.3	Radiation tolerance NIEL ( $\times 10^{16}$ neq/cm <sup>2</sup> )						$\approx$ 6	$\approx$ 2						$\approx$ 10 <sup>3</sup>			
			Radiation tolerance TID (Grad)						$\approx$ 1	$\approx$ 0.5						$\approx$ 30			
		Tracker <sup>6)</sup>	MAPS Planar/3D/Passive CMOS LGADs	DRDT 3.1 DRDT 3.4	Position precision $\sigma_{hit}$ ( $\mu\text{m}$ )					$\approx$ 6	$\approx$ 5			$\approx$ 6	$\approx$ 6	$\approx$ 7	$\approx$ 10	$\approx$ 6	
					X/X <sub>0</sub> (%/layer)					$\approx$ 1	$\approx$ 1			$\approx$ 1	$\approx$ 1	$\approx$ 1	$\approx$ 1	$\approx$ 2	$\approx$ 1
Power (mW/cm <sup>2</sup> )								$\approx$ 100	$\approx$ 100			$\approx$ 100		$\approx$ 100	$\approx$ 100	$\approx$ 150			
Rates (GHz/cm <sup>2</sup> )									$\approx$ 0.16			$\approx$ 0.16							
Wafers area (") <sup>4)</sup>								12				12		12	12	12	12		12
DRDT 3.2	Timing precision $\sigma_t$ (ns) <sup>5)</sup>							25	$\approx$ 25		25	25	$\approx$ 0.1	$\approx$ 0.1	$\approx$ 0.1	$\approx$ 0.02	25	$\approx$ 0.02	
DRDT3.3	Radiation tolerance NIEL ( $\times 10^{16}$ neq/cm <sup>2</sup> )								$\approx$ 0.3							$\approx$ 1			
	Radiation tolerance TID (Grad)								$\approx$ 0.25							$\approx$ 1			



# Exploring new physics...

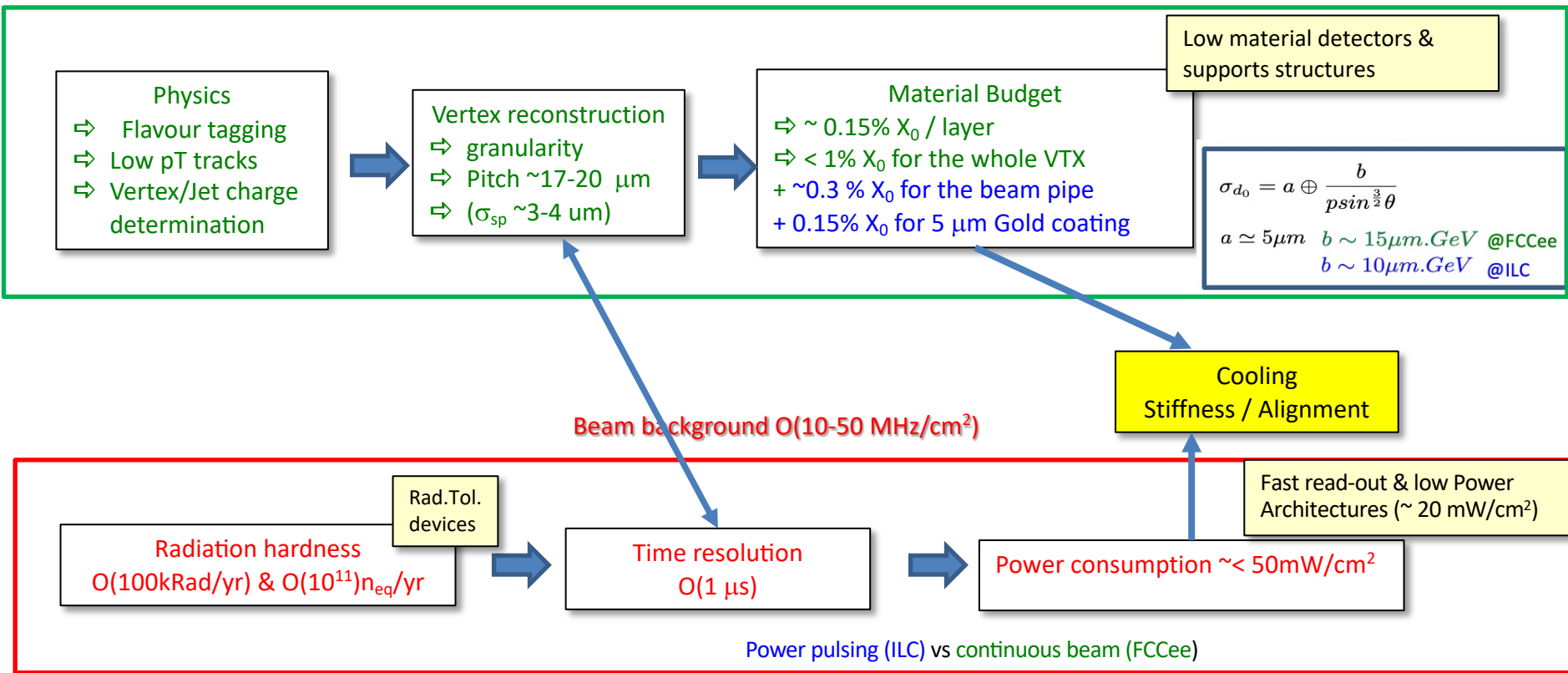


**3-sigma separation for tracks with  $p < 30\text{GeV}$**



# Constraints on vertex and tracker

Physics  $O(\text{Hz}/\text{cm}^2)$



# Requirements in summary

- Spatial resolution :  $\sim 3 \text{ um}$  (except LHCb, FCChh and Muon Colliders)
- Low material budget : 0.05 to 0.15 %  $X_0$
- Fast readout, low power consumption ( $< 20 \text{ mW/cm}^2$  except for CLIC) compatible with air cooling.
- Increase Radiation Hardness and more R&D for Ultra-Fast timing for future Hadrons and Muon Colliders

# Vertex/tracking detector concepts

D. Dannheim., 11th BTTB 2023

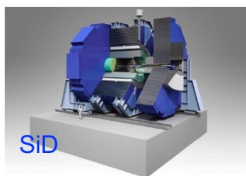
Collider	ILC		CLIC	FCC-ee			CEPC	
Detector Concept	SiD	ILD	CLICdet	CLD	FCC-ee IDEA	Noble LAr/LKr	CEPC baseline	CEPC IDEA
B-field [T]	5	4	4	2	2	2	3	2
Vertex inner radius [mm]	14	14	31	17 → 12	17 → 12	17 → 12	16	16
Tracker out. radius [m]	1.25	1.8	1.5	2.2	2.0	2.0	1.81	2.05
Vertex	Si-pixel	Si-pixel	Si-pixel	Si-pixel	Si-pixel	Si-pixel	Si-pixel	Si-pixel
Tracker	Si-strips	TPC/ Si-strips	Si-pixel	Si-pixel	DC/ Si-strips	DC/Si-strips or Si-pixel	TPC/Si-strips or Si-strips	DC/ Si-strips

[arXiv:1306.6329](https://arxiv.org/abs/1306.6329)

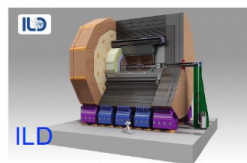
[arXiv:1812.07337](https://arxiv.org/abs/1812.07337) [arXiv:1911.12230](https://arxiv.org/abs/1911.12230)

[doi.org/10.1140/epjst/e2019-900045-4](https://doi.org/10.1140/epjst/e2019-900045-4)

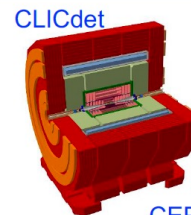
[arXiv:1811.10545](https://arxiv.org/abs/1811.10545)



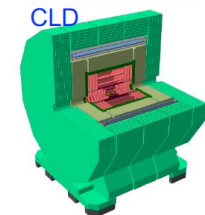
SiD



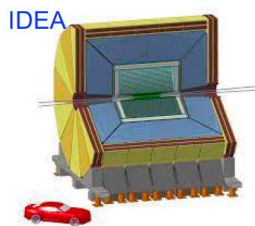
ILD



CLICdet



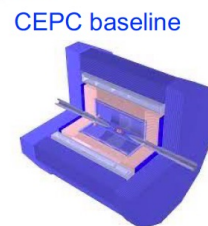
CLD



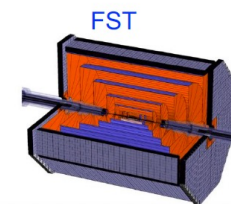
IDEA



Noble LAr/LKr

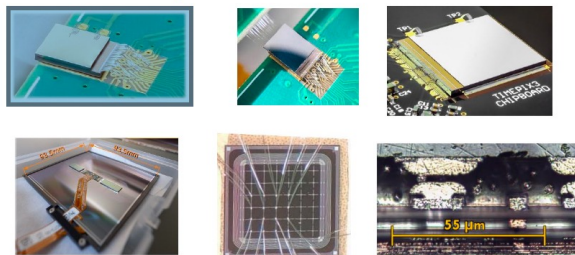


CEPC baseline

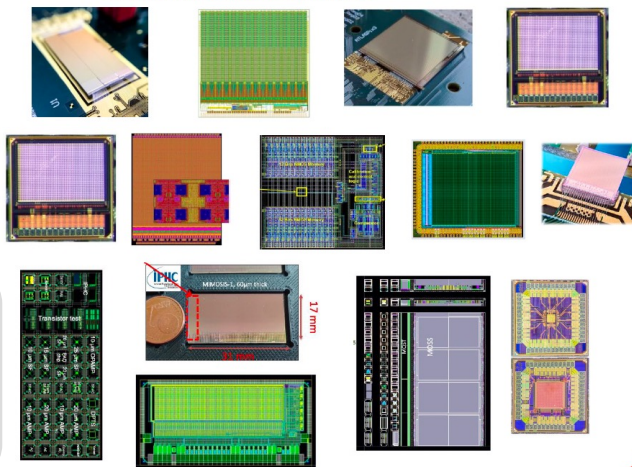


FST

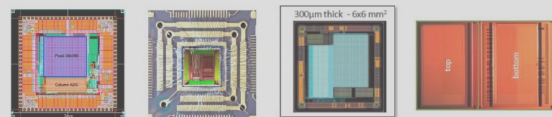
## Hybrid detectors



## Monolithic Sensors

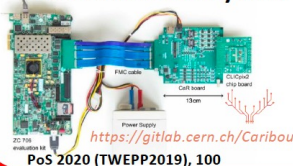


## Silicon on Insulator

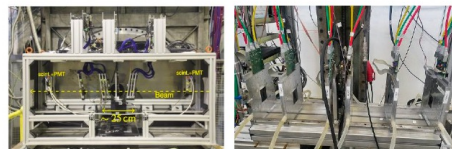


## Tools

### Caribou readout system



### CLICdp + AIDA telescopes



### MC Simulation framework: Allpix Squared



<https://gitlab.cern.ch/allpix-squared/allpix-squared>

NIM A 901 (2018) 164-172

### Analysis & reconstruction framework: Corryvreckan



<https://gitlab.cern.ch/corryvreckan/corryvreckan>

2021 JINST 16 P03008

- Diverse R&D performed within various collaborative frameworks (ILD, SiD, CLICdp, IDEA, CERN EP R&D, AIDAInnova, DRD3/7, ...), with strong links to other developments (HL-LHC, Belle II, Mu3e, CBM@FAIR, ...)
- Mostly focusing on conceptual studies + technology demonstrators
- Flexible tools developed, to support the R&D and exploit synergies between the various R&D lines

## Task Force 3 Solid State Detectors has identified the essential Detector R&D Themes (DRDT) which capture the most critical requirements:

- DRDT 3.1 - Achieve full integration of sensing and microelectronics in monolithic CMOS pixel sensors.
- DRDT 3.2 - Develop solid state sensors with 4D-capabilities for tracking and calorimetry.
- DRDT 3.3 - Extend capabilities of solid state sensors to operate at extreme fluences.
- DRDT 3.4 - Develop full 3D-interconnection technologies for solid state devices in particle physics.

**Implementation of TF3 Solid State Detectors**

22-23 mars 2023  
CERN  
Panneau horaire Europe/Zurich

Entrer le texte à rechercher

**Accueil**  
Ordre du jour  
Liste des contributions  
Inscription  
Videoconférence

The workshop will be on March 22-23rd at CERN.  
It is a mixed-mode meeting, in person and remote.  
Please send the DRD3 questionnaire (linked below) by January 27th.

Commence le 22 mars 2023, 09:00  
Finit le 23 mars 2023, 20:30  
Europe/Zurich

CERN  
223R-001  
Aller à la carte

Eva Vilella Figueras  
Gianluigi Casse  
Giovanni Calderini  
Giulio Pellegrini  
Gregor Kramberger  
Joana Pintilie  
Ivan Vila Alvarez  
Michael Moll  
Nicolo Cartiglia

Questionnaire DRD3.docx  
Questionnaire DRD3.pdf

Institutes that have expressed interest (presently, 96 institutes filled out the questionnaire):

- Austria: HEPHY
- Brazil: USP
- Canada: Carleton/NRC (Ottawa), SFU, TRIUMF
- Chile: UNAB/SAPHIR, UTFSM
- China: Dalian Univ. of Tech, IHEP, Jilin Univ., USTC
- Croatia: RBI
- Czech Republic: Charles Univ. Prague, FNSPE CTU, FZU Czech Academy
- Finland: Helsinki-FIP, LUT University of Technology
- France: APC, cppm.in2p3, IJCLab, IP2I, IPHC, Irfu CEA, LPNHE Paris
- Germany: Bonn, CIS, DESY, Dortmund, Freiburg, Gottingen, GSI, Heidelberg, HU Berlin, IZM, KIT, MPG HLL, MP
- Greece: Demokritos
- India: IITM
- Israel: Tel Aviv, WIS
- Italy: FBK, INFN Ba, INFN CNR Perugia, INFN FI, INFN Genova, INFN Pisa, INFN To, UniFi, UniMi, UniPavia
- Japan: KEK
- Lithuania: Vilnius University
- Montenegro: University of Montenegro
- Netherlands: ESA, Nikhef, PARTREC
- Poland: AGH Krakow
- Romania: NIMP
- Slovenia: JSI
- Spain: CNA, GIE, ETSI-Sevilla, IFAE-RD50, IFCA-Santander, IFIC-Valencia, IGFAE-USC, IMB-CNM-CSIC, ITAINN
- Switzerland: CERN, ETH, PSI, UNIGE, UZH
- Türkiye: Istanbul Univ.
- UK: BILPA/Birmingham, Bristol, Brunel Univ, Cambridge, Daresbury, Glasgow, Liverpool, Manchester, Oxford, C
- USA: BNL, FNAL, Los Alamos, OSU, SCIPP, Univ. of Illinois, Chicago, Univ. of New Mexico, UTK



# Working Groups

- WG1 Monolithic CMOS Sensors
- WG2 Sensors for Tracking and Calorimetry
- WG3 Radiation damage and extreme fluences
- WG4 Simulation
- WG5 Characterization techniques, facilities
- WG6 Wide bandgap and innovative sensor materials
- WG7 Interconnect and device fabrication
- WG8 Dissemination and outreach

# R&D

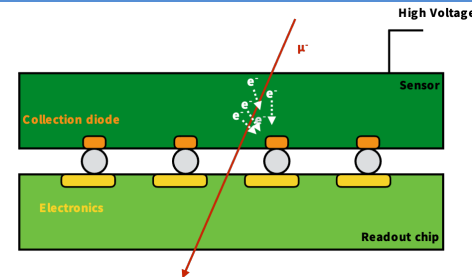
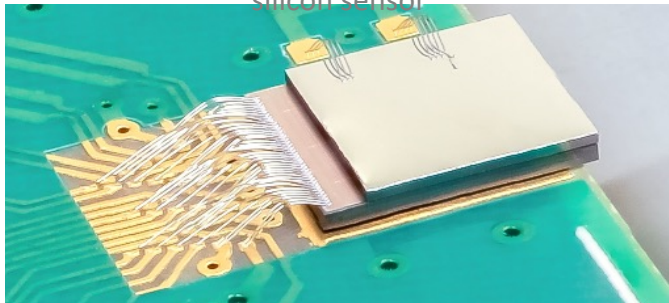


# Hybrid pixel detectors

*P. Svihra et al., BTTB 2023*

- Enable to factorise R&D on sensors and readout ASICs.
- Take advantage of advancements in ASIC technologies and performances
- Bumping remains the main challenge as well as material budget, cost and minimal pitch achieving.
- R&D with Fraunhofer IZM for development of single-die bonding process
  - Based on support wafer processing with SnAg bumps
  - Verified for multiple CLICpix2 assemblies in lab and beam-test
    - 128x128 pixels with **25  $\mu\text{m}$  pixel pitch**
    - 50  $\mu\text{m}$ , 100  $\mu\text{m}$ , 130  $\mu\text{m}$  sensor thickness

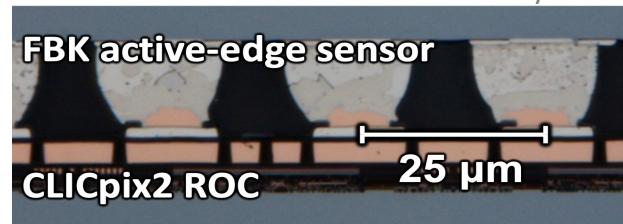
CLICpix2 ASIC bump-bonded to an active edge silicon sensor



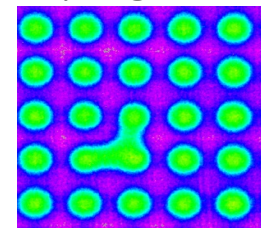
[Reference 1](#)  
[Reference 2](#)



Cross-section of bonded assembly



IZM  
X ray image of bumps



provided by Nikon XT V  
160  
by Abishek Sharma

Interconnection yield above **99.7%**  
for four tested devices

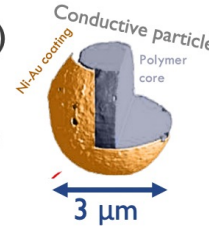
[10.1088/1748-0221/18/03/C03008](https://doi.org/10.1088/1748-0221/18/03/C03008)

## ANISOTROPIC CONDUCTIVE ADHESIVE BONDING



EP R&D

- **Anisotropic Conductive Film/Paste (or Non-conductive) – ACF/ACP or NCF/NCP**
  - ACF widely used in industry (display manufacture, ...)
  - Process needs adapting for 2D bonding (pixels)
- Bonding done at Geneva University using semi-automatic flip-chip bonder
  - Precise temperature, pressure and alignment control, heating up to 400 °C
- Film based bonding has two steps – lamination and bonding
  - Pressure applied to displace and compress particles
  - Epoxy cures at 150 °C for a few seconds only



SET ACC $\mu$ RA100

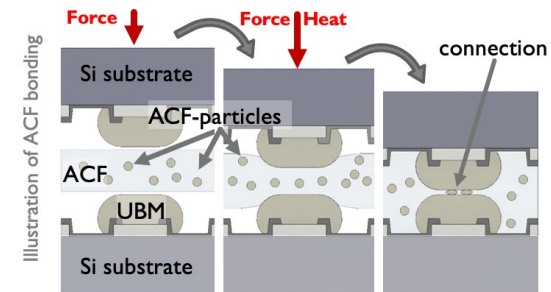
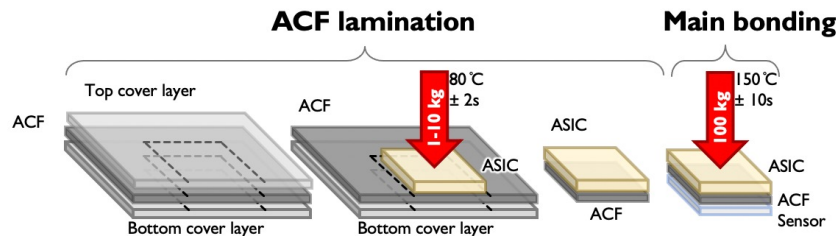
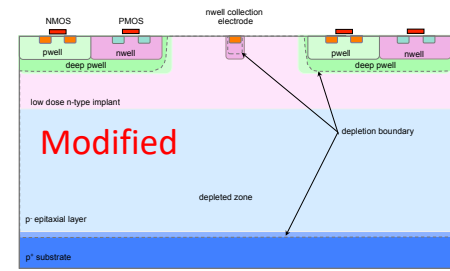
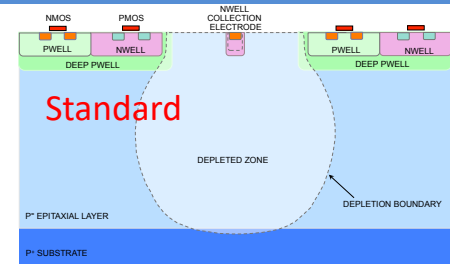


Illustration of ACF bonding

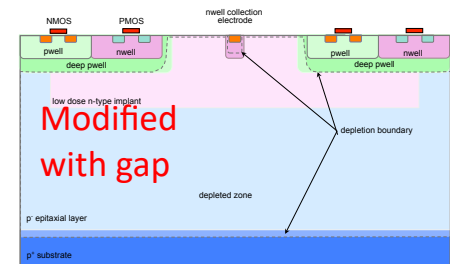
20.04.2023

# Exploring the TPSCo 65 nm

- Benefits : 65 nm vs 180 nm
  - Better spatial resolution due to smaller feature size.
  - Larger wafers : 300 mm vs 200 mm => final sensor : 27x9 cm<sup>2</sup>.
  - Lower power supply : 1.2 V vs 1.8 V => Low power consumption.
  - Lower material budget : thinner sensitive layer (  $\sim 10\mu m$  ).
- Provides 2D stitching
- 7 metal layers
- Process modifications for full depletion:
  - Standard (no modifications)
  - Modified (low dose n-type implant)
  - Modified with gap (low dose n-type implant with gaps)



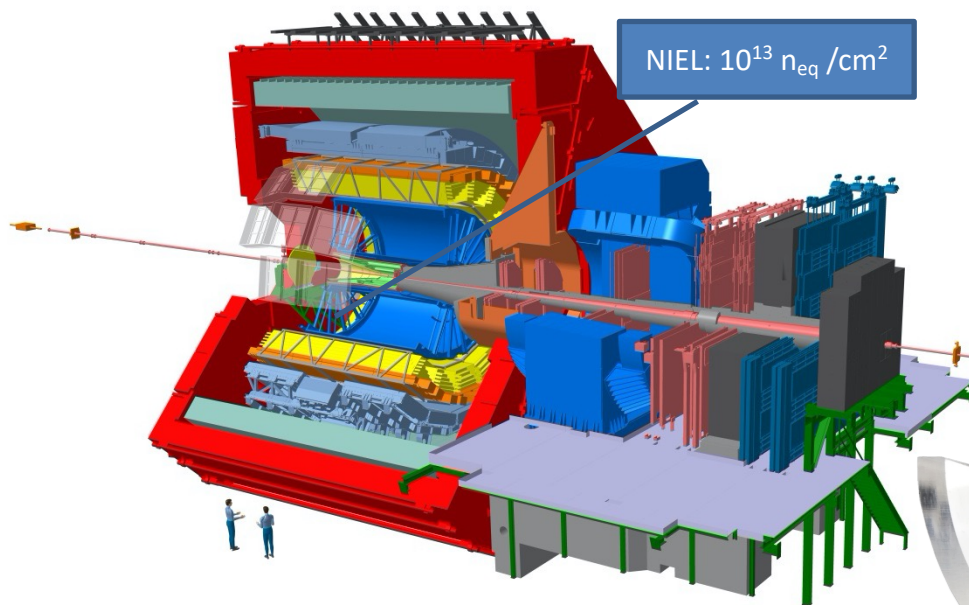
<https://doi.org/10.1016/j.nima.2017.07.046>



<https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013>

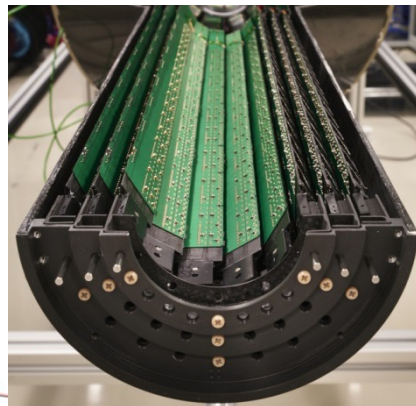
# Alice detector LS3 upgrade: ITS2 (180 nm) → ITS3 (65nm)

[R. Ricci, PSD 2023](#)



ALICE – general purpose detector at LHC:

- Tracking (100 MeV/c – 100 GeV/c)
- Particle identification:  $\pi$ , K, p, e (0.1 – 50 GeV/c)



## ITS2:

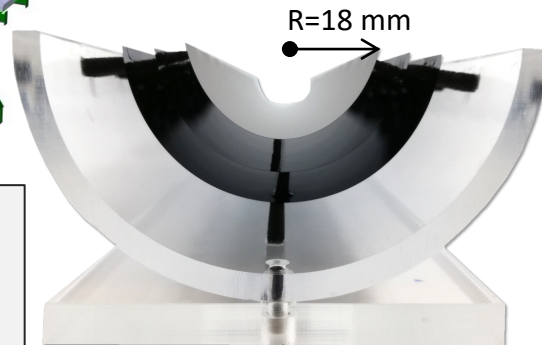
[\(S.Beol , iWoRiD 2022\)](#)

- 7 layers of MAPS
- TJ 180 nm CMOS
- 12.5 Giga pixels
- Pixel size:  $27 \times 29 \mu\text{m}^2$
- Water cooling
- **0.3 %  $X_0$  / inner layer**

## ITS3

[\(M.  ulji , iWoRiD 2023\)](#)

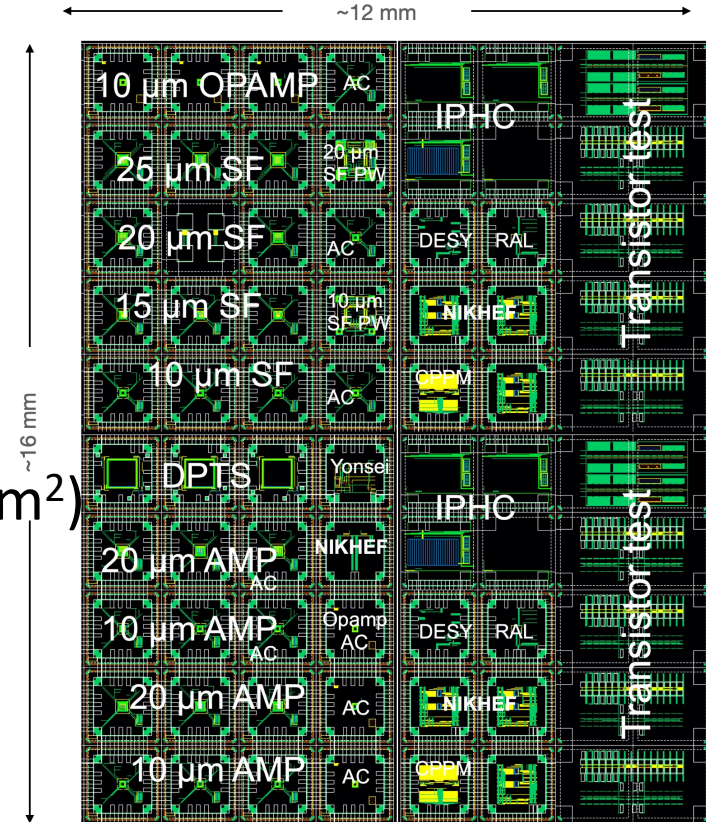
- 4 outer layers of ITS2
- 3 new fully cylindrical inner layers
  - Sensor size up to  $27 \times 9 \text{ cm}$
  - Thickness 30-40  $\mu\text{m}$
  - No FPCs
  - Air cooling in active area
- **0.05 %  $X_0$  / inner layer**





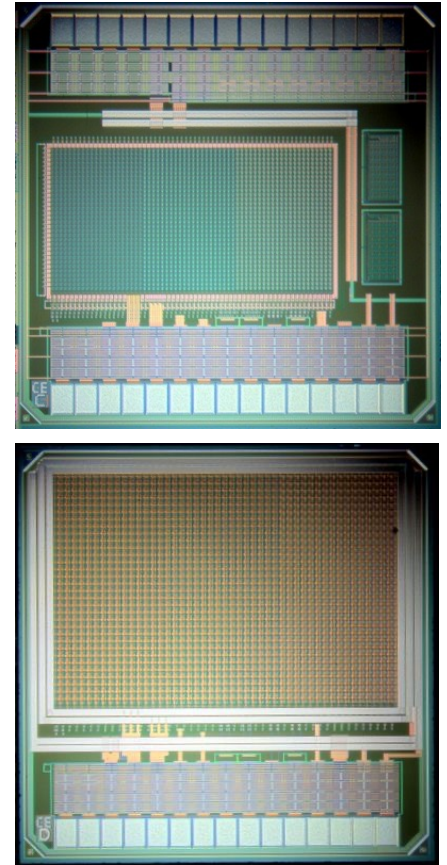
# First Test Submission : MLR1

- Submitted in December 2020
- Main goals:
  - Learn technology features
  - Characterize charge collection
  - Validate radiation tolerance
- Each reticle ( $12 \times 16 \text{ mm}^2$ ):
  - 10 transistor test structures ( $3 \times 1.5 \text{ mm}^2$ )
  - 60 chips ( $1.5 \times 1.5 \text{ mm}^2$ )
    - Analogue blocks
    - Digital blocks
    - **Pixel prototype chips: APTS, CE65, DPTS**



# CE65 : Circuit Exploratoire 65 nm

- 2 matrix sizes
  - 64×32 with 15  $\mu\text{m}$  pitch
  - 48×32 matrix with 25  $\mu\text{m}$  pitch
- Rolling shutter readout (50  $\mu\text{s}$  integration time)
- 3 in-pixel architectures:
  - AC-coupled amplifier
  - DC-coupled amplifier
  - Source follower
- 4 chip variants:
  - **Standard process 15  $\mu\text{m}$  pitch**
  - Modified process 15  $\mu\text{m}$  pitch
  - **Modified process with gaps 15  $\mu\text{m}$  pitch**
  - Standard process 25  $\mu\text{m}$  pitch
- Fabrication in September 2021
- Presented results from CERN PS beam test : May 2022

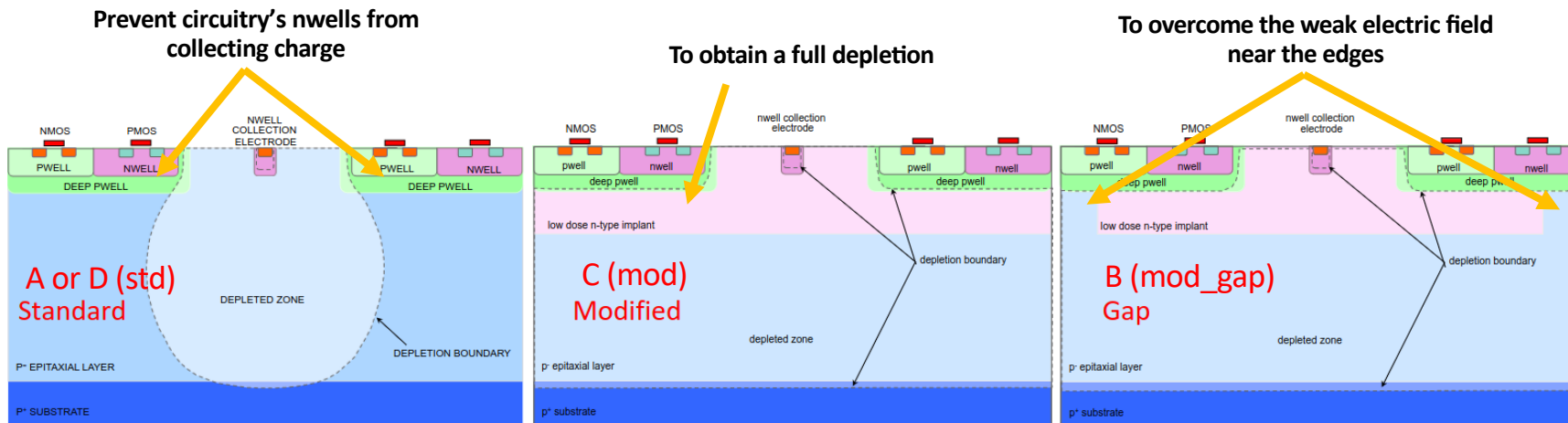


1.5×1.5 mm<sup>2</sup> 18

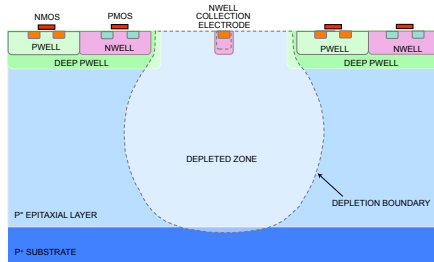
# CE65 variants

Variant	Process	Pitch	Matrix	Sub-matrix
CE65-A	std	15 $\mu$ m	64 $\times$ 32	AC/21, DC/21, SF/22
CE65-B	mod_gap	15 $\mu$ m	64 $\times$ 32	AC/21, DC/21, SF/22
CE65-C	mod	15 $\mu$ m	64 $\times$ 32	AC/21, DC/21, SF/22
CE65-D	std	25 $\mu$ m	48 $\times$ 32	AC/16, DC/16, SF/16

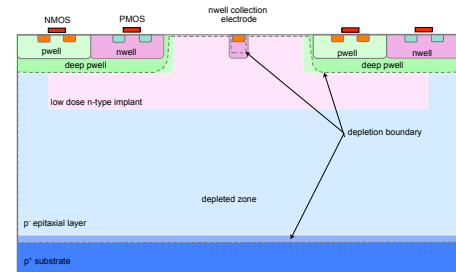
Pixel pitch impact was evaluated on standard process only



# Process modification impact



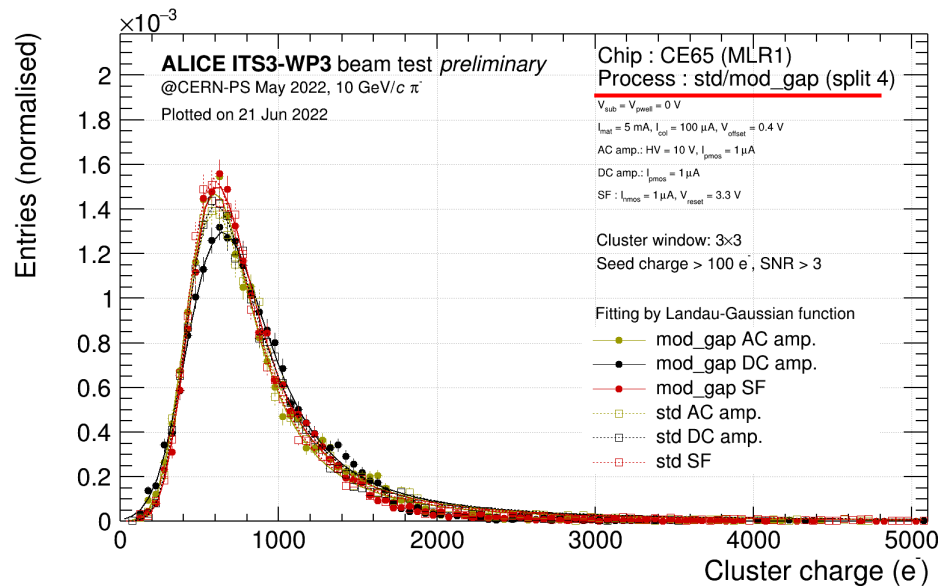
Standard



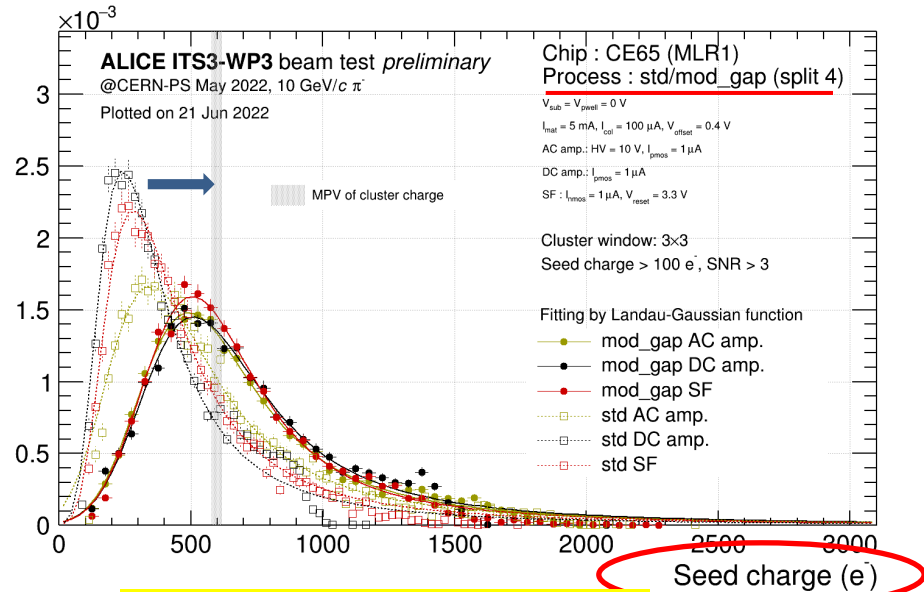
Modified with gap



# Modified process effective for depletion...

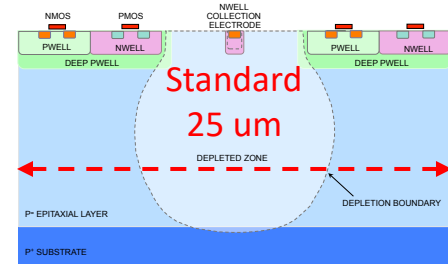
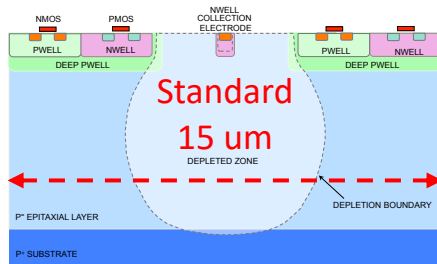


Cluster charge is not affected by process modification



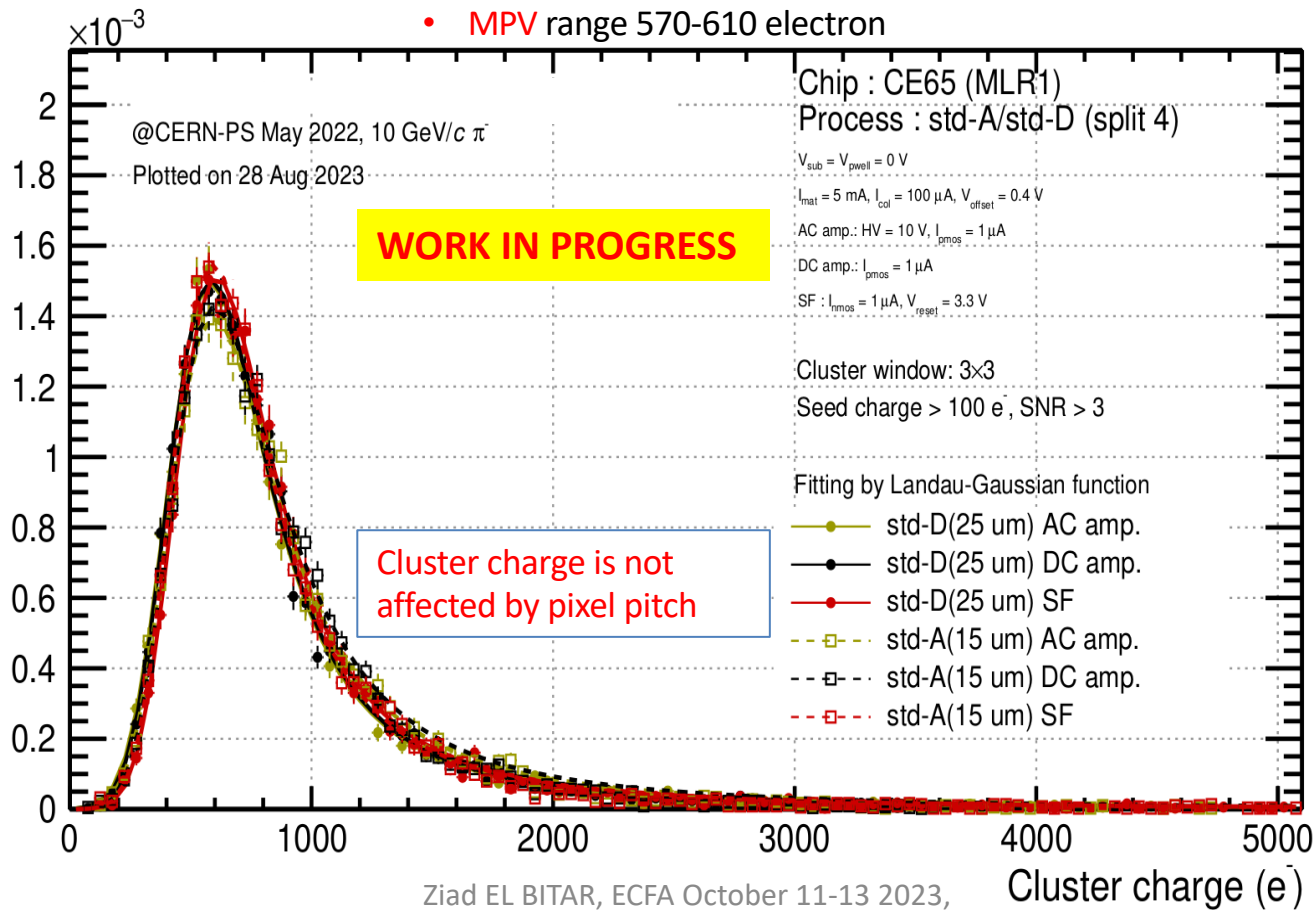
Seed charge is affected by process modification

# Pixel pitch impact



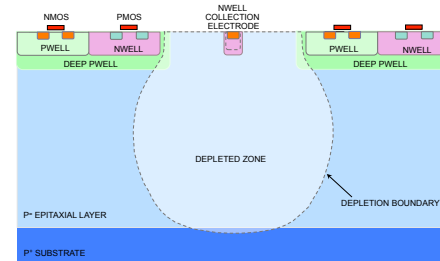
# Cluster charge

Entries (normalised)



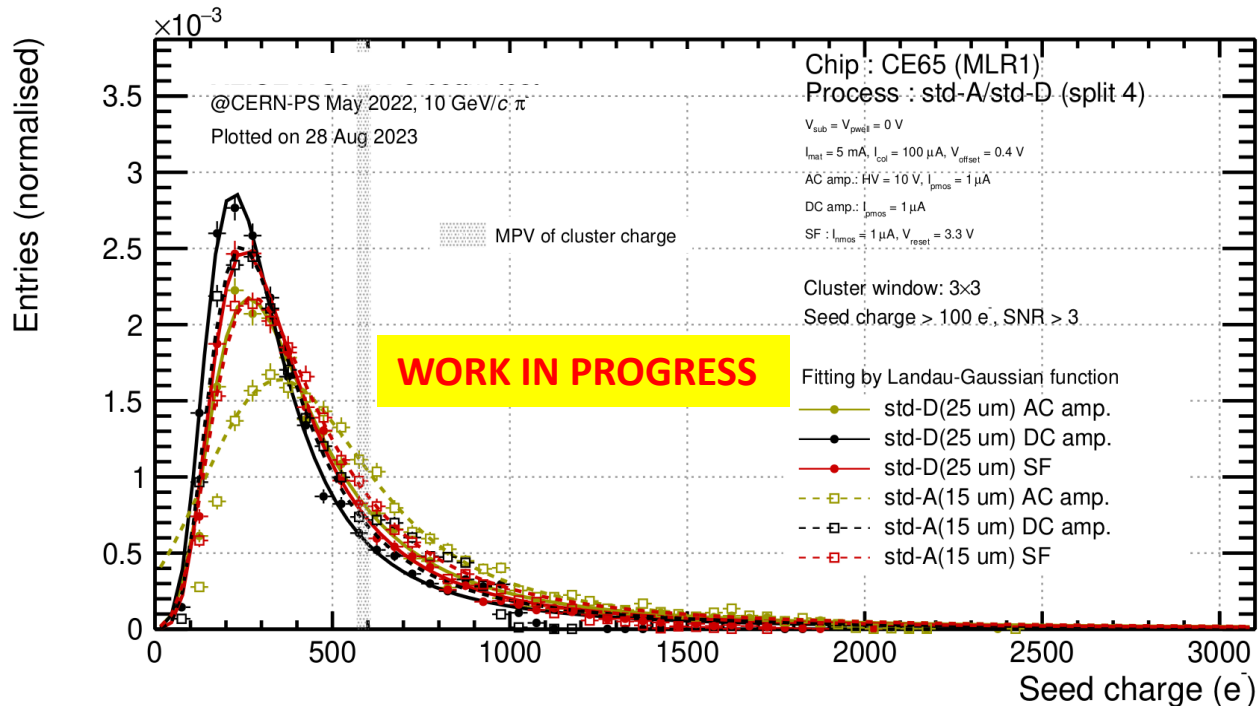
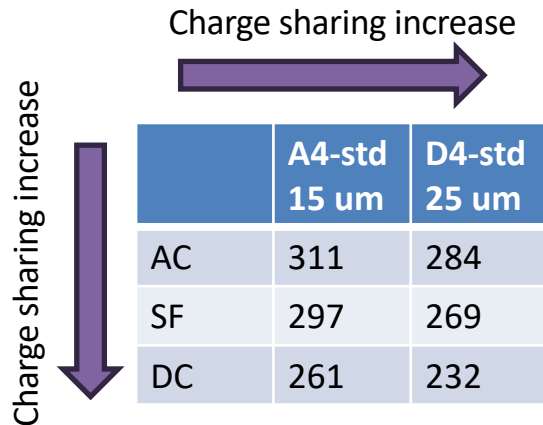
Ziad EL BITAR, ECFA October 11-13 2023,  
Paestum

Pixel pitch evaluation for  
standard process only



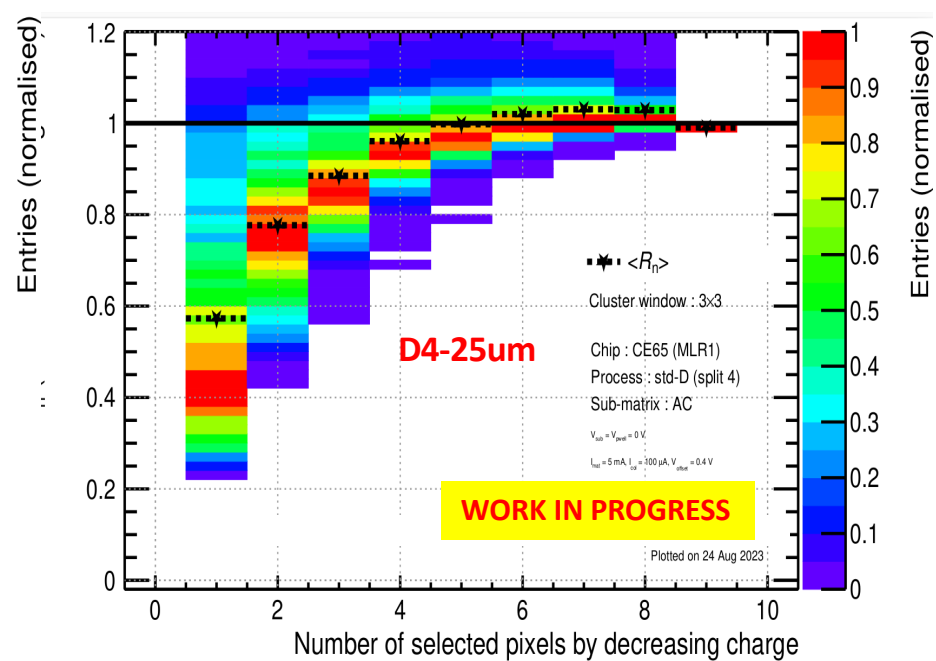
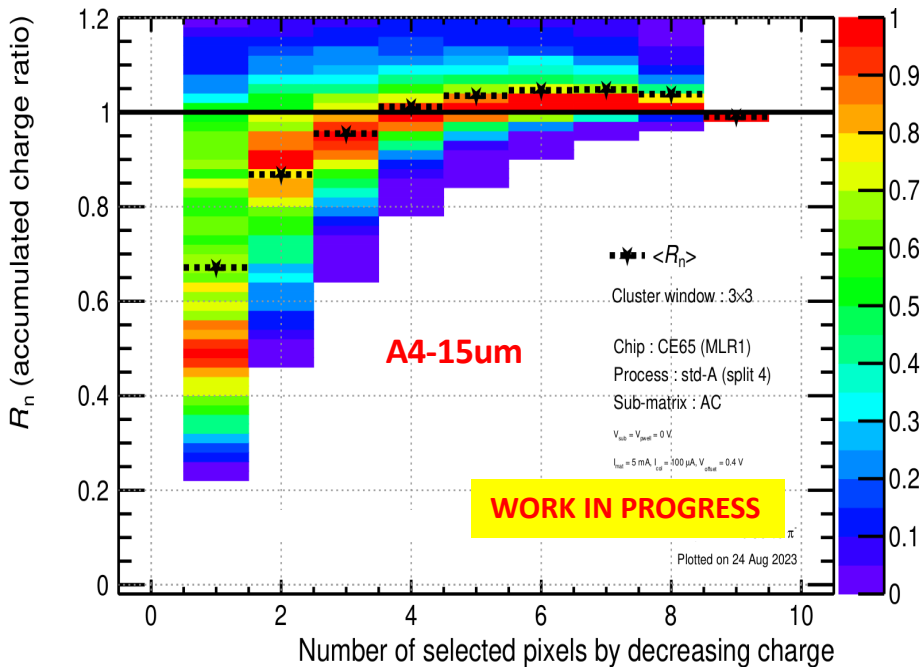
# Seed charge

- Seed peaks



# Charge sharing

- 4 pixels contain all cluster charge for AC submatrix in A4-15um where it needs 5-6 pixels for D4-25um.
- Seed pixel contains: **more** than 60% in average for A4  
a little bit **less** than 60% in average for D4



# Simulations: ALLPix + TCAD

C. Ferrero et al., TREDI, 2023

## ARCADIA fully-depleted monolithic active pixel sensors optimised for sub-nano second timing

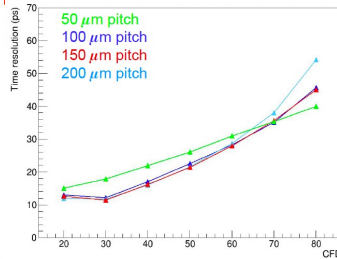
### TCAD

- Numerical simulation tool for sensor modeling
- Describes carriers motion and electromagnetic fields
- Very demanding on computing time

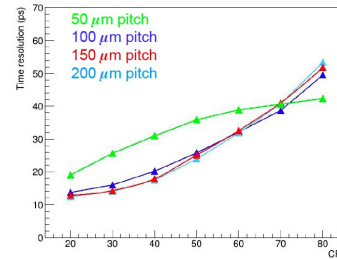


### ALLPIX<sup>2</sup>

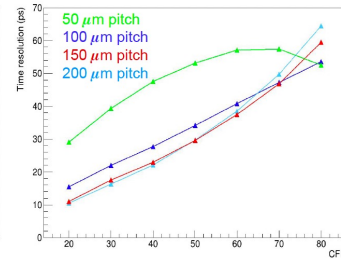
- Monte Carlo simulations
- High statistics
- Geant4 for energy deposition
- Telescope and complex detector geometries



Thickness 25  $\mu\text{m}$



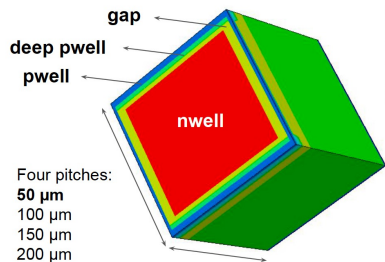
Thickness 35  $\mu\text{m}$



Thickness 50  $\mu\text{m}$

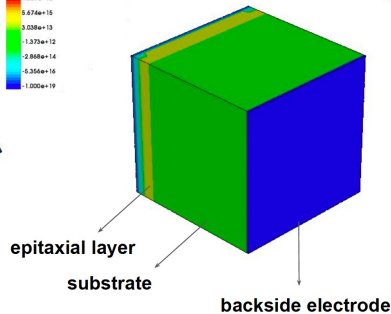
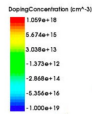
## ARCADIA pad diode monolithic sensor

TCAD single pixel simulation domain:  $(50 \times 50 \times 50) \mu\text{m}^3$

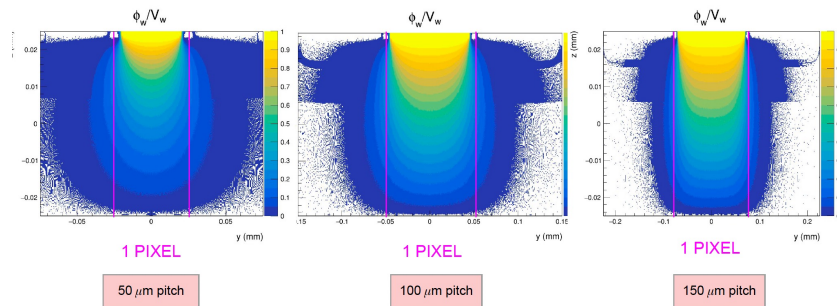


Four pitches:  
50  $\mu\text{m}$   
100  $\mu\text{m}$   
150  $\mu\text{m}$   
200  $\mu\text{m}$

Three thicknesses:  
25  $\mu\text{m}$   
35  $\mu\text{m}$   
50  $\mu\text{m}$



## Weighting Potential - 3x3 simulation domain 50 / 100 / 150 $\mu\text{m}$ pitch

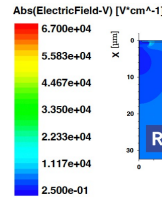
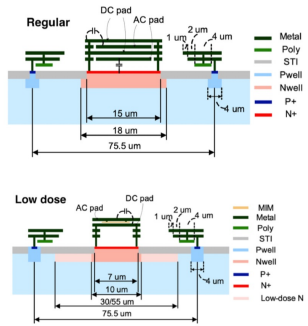
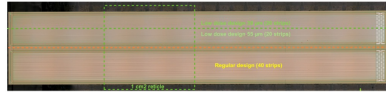


# Stitching passive strip CMOS

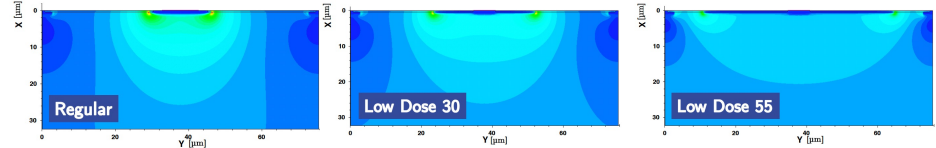
I. Zatocilova et al., iWoRiD 2023

## Passive CMOS Strips

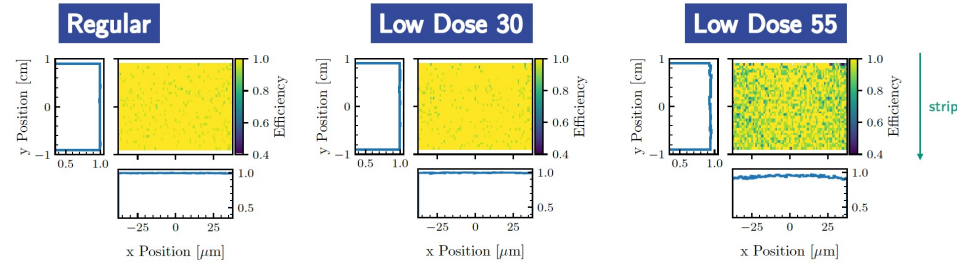
- Sensors fabricated in LFoundry in a 150 nm process
- Passive → no electronics included
- 150 μm thick silicon wafer
- Two lengths of strips 2.1 and 4.1 cm
  - 1 cm<sup>2</sup> reticle used → strips had to be stitched
  - Up to five stitches in each sensor
- Three different designs
  - Regular – similar to the ATLAS strip design
  - Low dose 30 & 55 – low dose implant and NIM capacitor



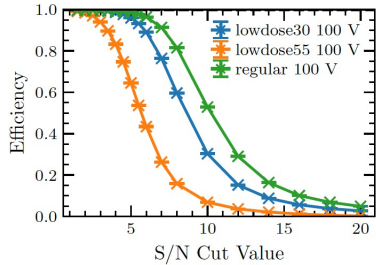
## Electric Field @ 100 V, Sentaurus TCAD simulation



## Test Beam, Unirradiated

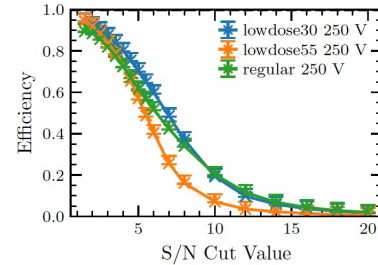


## Unirradiated

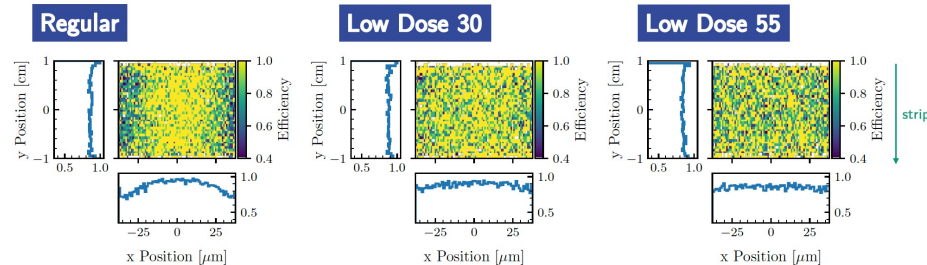


## Irradiated

by 23 MeV neutrons  
 $\Phi_{eq} = 3 \cdot 10^{14} \text{ n}_{eq}/\text{cm}^2$



## Test Beam, irradiated







# Stitching active pixel CMOS

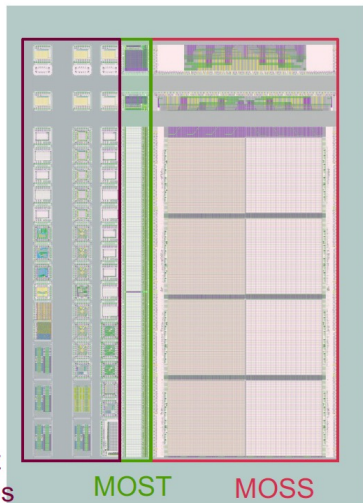
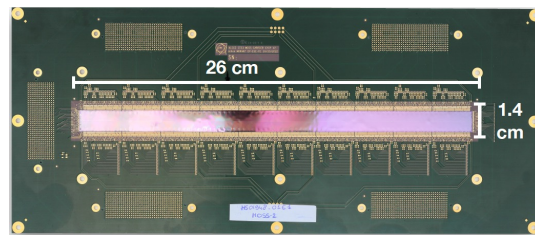
• First MAPS for HEP using stitching - one order of magnitude larger than previous chips

• **“MOSS”** : 14 x 259 mm, 6.72 MPixel (22.5 x 22.5 and 18 x 18  $\mu\text{m}^2$ )  
- conservative design, different pitches

• **“MOST”** : 2.5 x 259 mm, 0.9 MPixel (18 x 18  $\mu\text{m}^2$ )  
- more dense design

• Plenty of small chips (like MLR1)

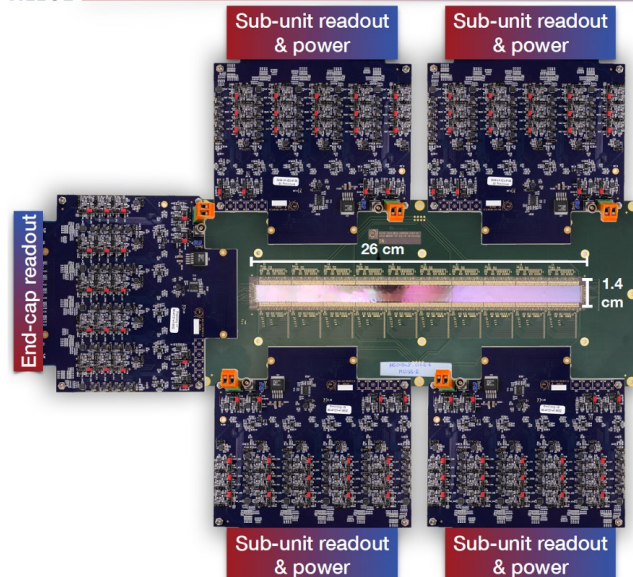
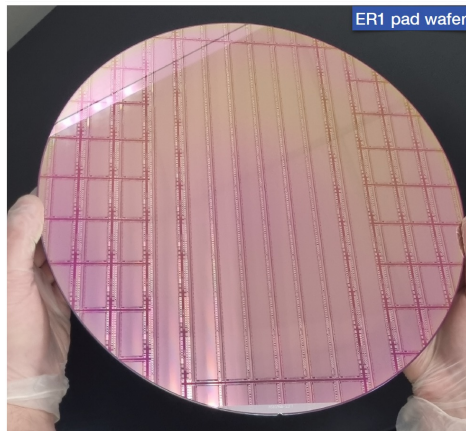
reticle



Test chips

MOST

MOSS

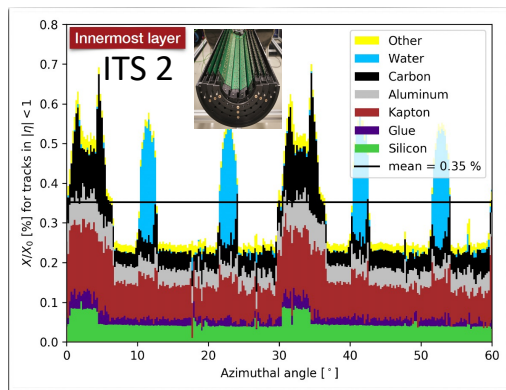


[W. Snoeys, PSD 2023](#)

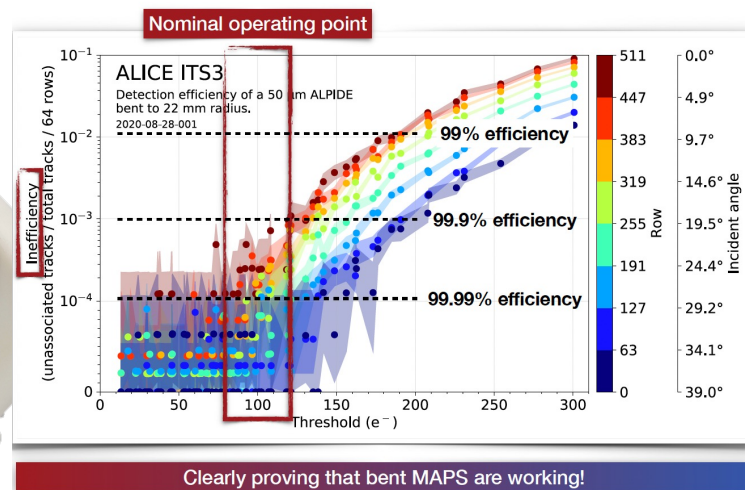
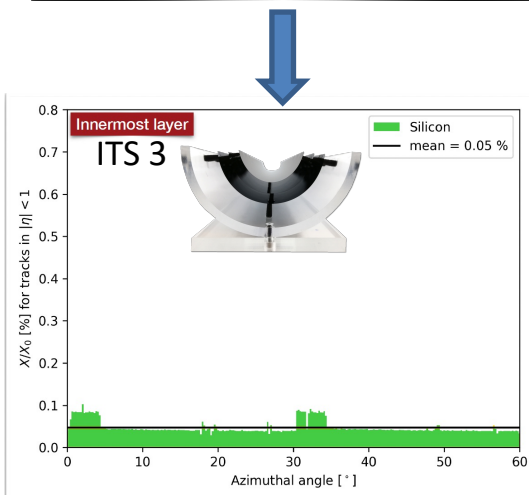
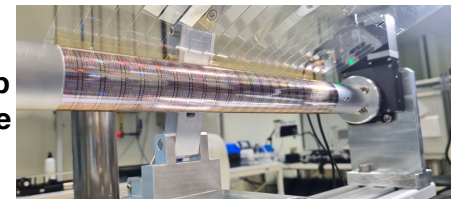


# Bent sensor: reducing material budget

[M. Suljic et al., iWoRiD 2023](#)



- Observations: - Si makes only 1/7-th of total material budget - Non-uniformity due to support, cooling & overlaps
- Removal of water cooling: - If **power consumption < 20 mW/cm<sup>2</sup>**
- Removal of the circuit board for power & data: - If **integrated on chip**
- Removal of mechanical support: - **Self-supporting arched structure**



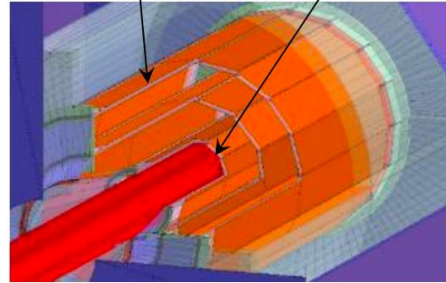
Clearly proving that bent MAPS are working!

# VXD Prototype - CEPC

S. Li et al., BTTB 2023

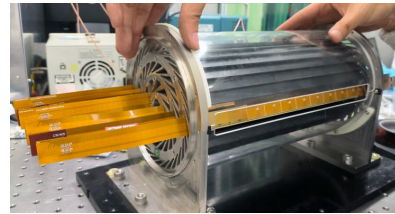
T. Wu et al., PSD 2023

2 layers / ladder  $R_{in} \sim 16$  mm

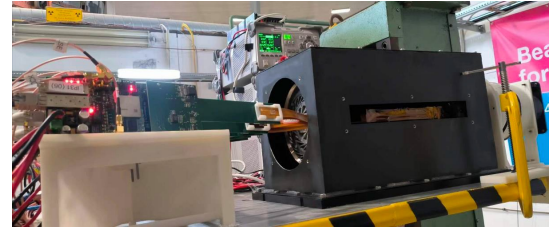


FPGA board

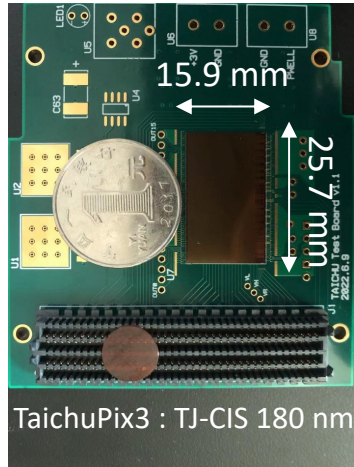
FPGA board



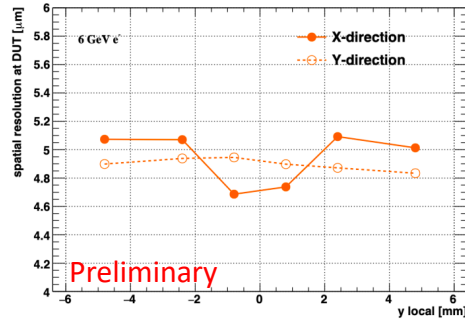
Vertex Prototype



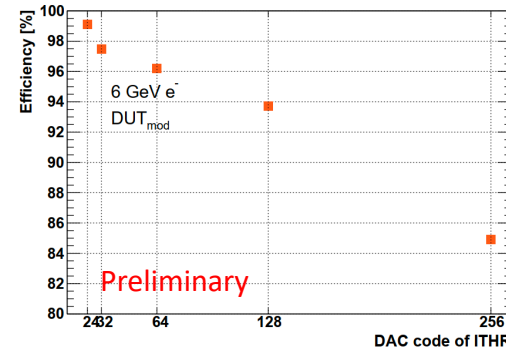
Test Beam @ DESY



Pixel size: 25  $\mu$ m x 25  $\mu$ m



Preliminary



Preliminary

<https://doi.org/10.1016/j.nima.2018.11.133>

# Summary

- Plenty of R&D to follow carefully.
- Exploring new technologies is very promising (TPSco65 nm).
- Some detector requirements are achieved: spatial resolution ( $\sim 5$   $\mu\text{m}$ ).
- Material budget is drastically reduced (bent sensors).
- Stitching sensors is very well advanced.

THANK YOU