Future MAPS Development Scenario

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SuperB Meeting

La Biodola, Elba, May 30 – June 3, 2008

Status of MAPS

- After several years of R&D, monolithic active pixel sensors for particle detection are reaching a good maturity level, but there is still room for substantial improvements

- The performance of standard MAPS needs to be upgraded if they have to fulfill specifications of experiments at ILC or SuperB

- MAPS can benefit from technological advances; the scenario of microelectronics processes and performance typically changes in a time scale of 1-2 years.

MAPS R&D strategies

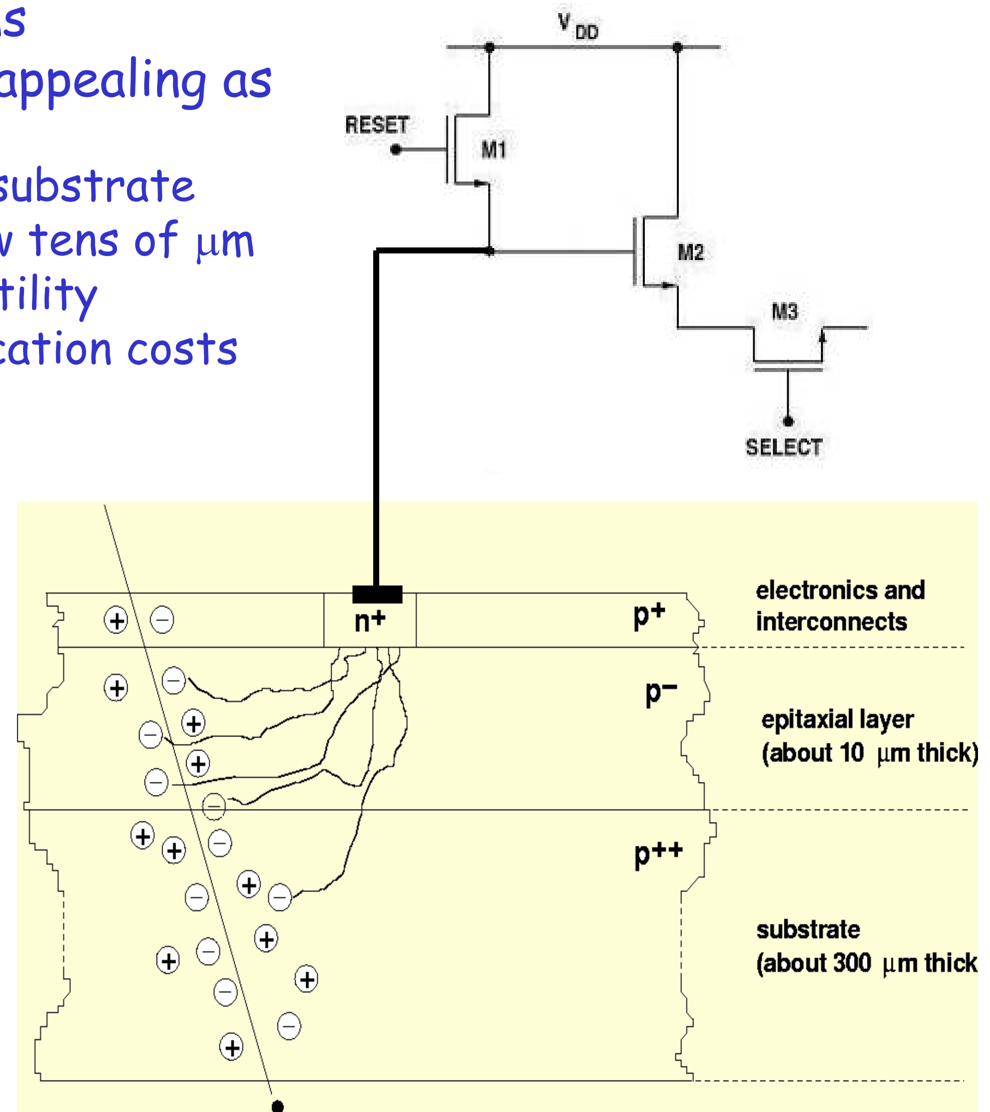
Two main development lines are followed by the HEP MAPS community:

- Improve electronics performance:
  ➔ put more intelligence on the chip, and possibly on the pixel itself
  (handling of high data rates, analog-to digital conversion, sparsification,…)

- Improve sensor performance:
  ➔ improve the quality of the sensor substrate and the charge collecting properties of sensing electrodes
  (increase efficiency, collected charge and signal-to-noise ratio, improve radiation tolerance,…)

The standard reference: 3T CMOS MAPS

- Developed for imaging applications
- Several reasons make them very appealing as tracking devices :
  - detector & readout on the same substrate
  - wafer can be thinned down to few tens of μm
  - high functional density and versatility
  - low power consumption and fabrication costs



Principle of operation

- The undepleted epitaxial layer (or a non-epi substrate) acts as a potential well for electrons
- Signal (~1000 e-) collected through diffusion by the n-well contact
- Charge-to-voltage conversion provided by the sensor capacitance
  → small collecting electrode
- Simple in-pixel readout (PMOS not allowed)
  → sequential readout

Put more intelligence on chip

MIMOSA sensors (Strasbourg, LBNL)

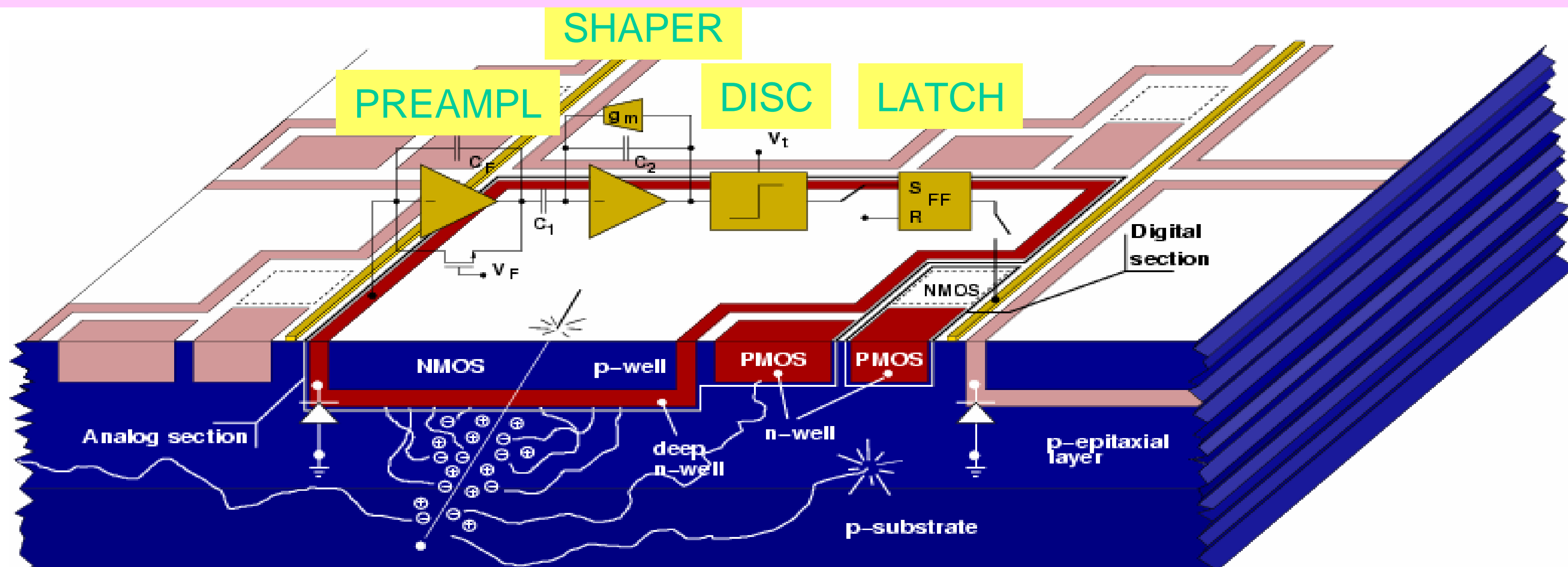
- Natural development of standard imaging MAPS, mostly in 0.35 μm CMOS – Opto process (~ 10 μm epitaxial layer)
- Achieved impressive performance with analog output sensors (slow, serial readout)
- Now developing more advanced devices with fast column-parallel readout, with Correlated Double Sampling on pixel (MIMOSA16, MIMOSA22), 4-5 bit ADCs at end of columns, zero suppression (next generation)

DNW MAPS (INFN)

- SuperB (APSEL chips) and ILC sensors in 130nm bulk CMOS (non-epi) with on-pixel sparsification, binary readout with time stamping (see talk by Giuliana Rizzo)

Deep N-Well (DNW) sensor concept

New approach in CMOS MAPS design compatible with data sparsification architecture to improve the readout speed potential



Classical optimum signal processing chain for capacitive detector can be implemented at pixel level:

- Charge-to-Voltage conversion done by the charge preamplifier
- The collecting electrode (Deep N-Well) can be extended to obtain higher single pixel collected charge (the gain does NOT depend on the sensor capacitance), reducing charge loss to competitive N-wells where PMOSFETs are located
- Fill factor = DNW/total n-well area ~90% in the prototype test structures

Improve sensor performance

CMOS MAPS

Quadruple well CMOS process

Deep P-wells to shield competitive N-wells with PMOS, fill factor ~ 100%

Graded epitaxial substrate

Field shaping using doping gradient: faster charge collection (reduce effect of bulk damage), smaller charge spread (ideal for binary readout)

SOI MAPS, 3D APS

Fully depleted, high resistivity substrate

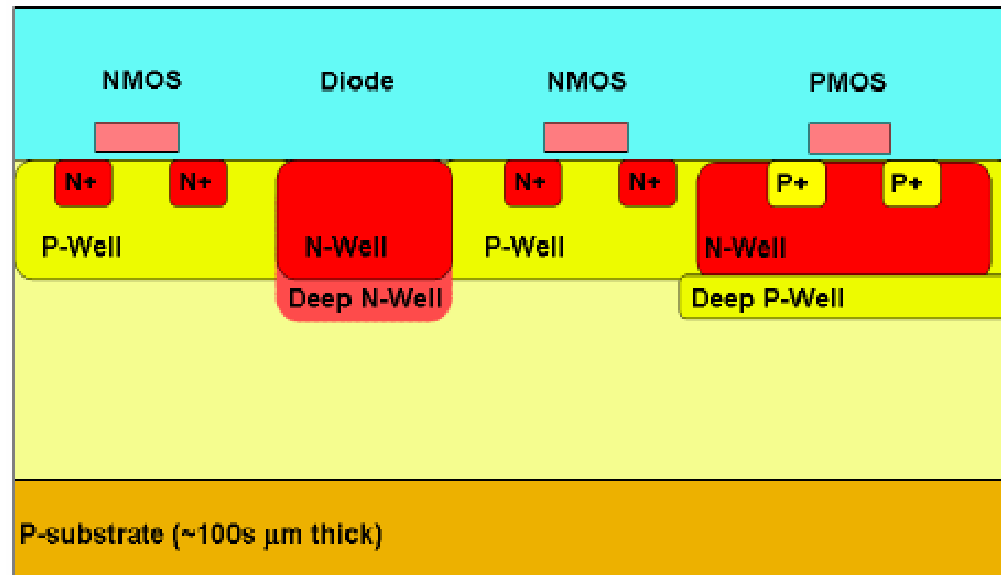
Large signal, minimum charge spreading

Not available with bulk CMOS

Quadruple well CMOS process

- Standard 0.18 μm image sensor process, not (yet?) available to all users, with additional deep P-well implant
- Full CMOS without degrading charge collection with competitive N-wells

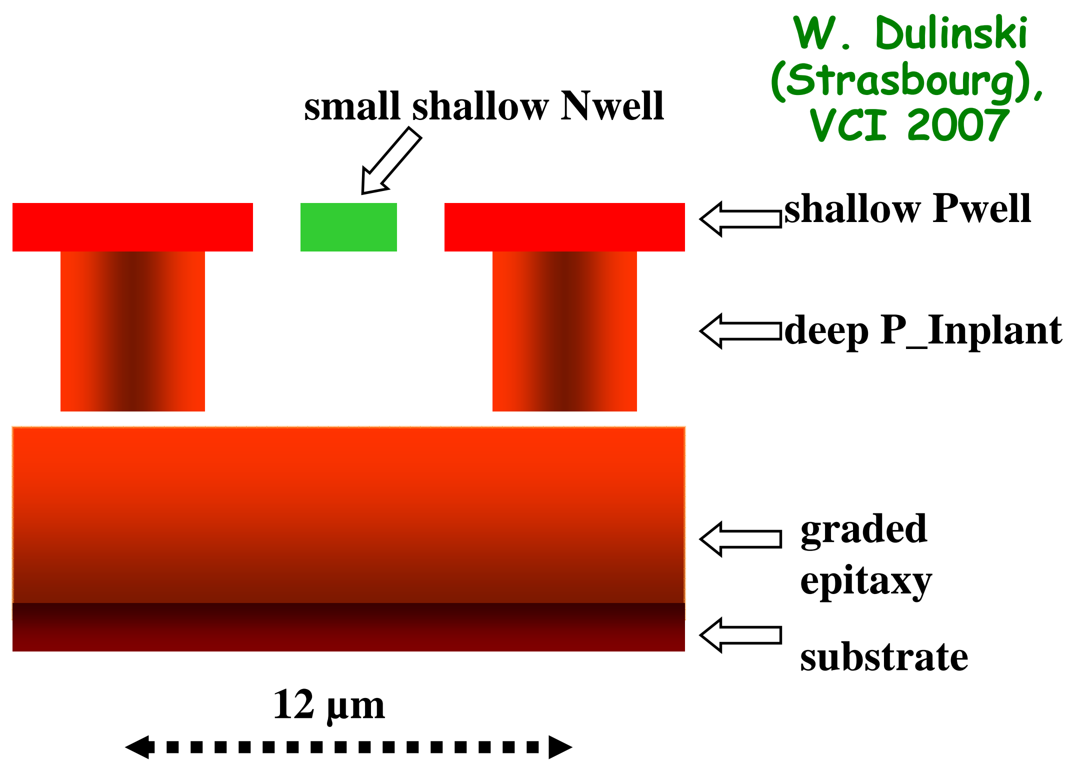
RAL, ILC CALICE collaboration



Graded epitaxial substrate

- Selected CMOS foundries agree to process custom silicon wafers
- Doping gradient generates an electric field in the substrate, helping charge collection

W. Dulinski (Strasbourg), VCI 2007



Example from our simulation of novel MAPS structure (ISE TCAD, realistic doping profiles). In parentheses, typical standard structure.

-Charge collection time: < 10 ns (~100ns)

-Charge spread suppression:

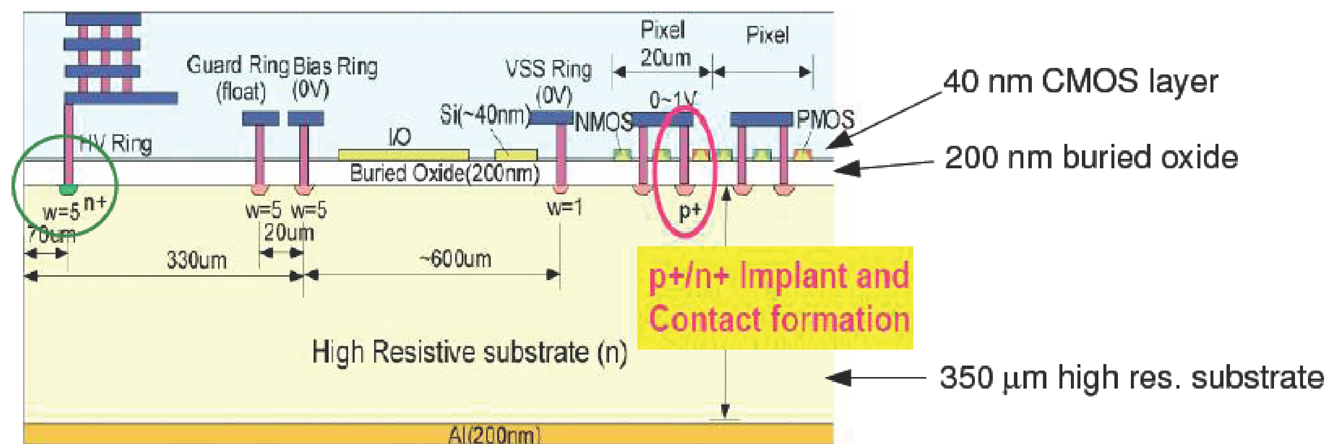
> 60% (<30%) of charge in central pixel,
all charge inside < 4 pixels (>9 pixels)

Prototypes in construction!

Fully depleted sensors: SOI

0.15 μm, 0.20 μm OKI technology
(LBNL, FNAL, Japan,...)

- integration of readout electronics isolated by the buried oxide layer (BOX) from a high resistivity substrate where fully-depleted detector elements can be located



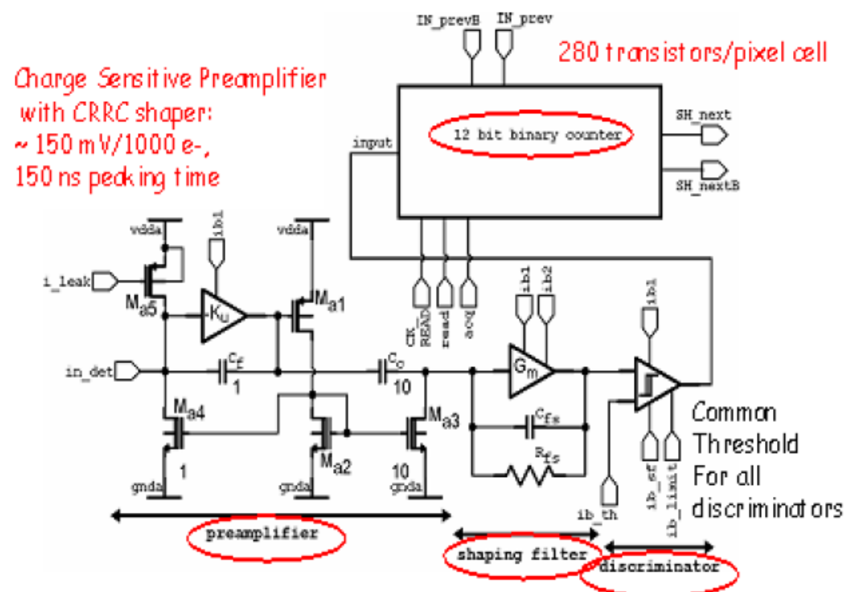
[NIM A 582 (2007) 861]

Examples of SOI MAPS

Fermilab: MAMBO chip

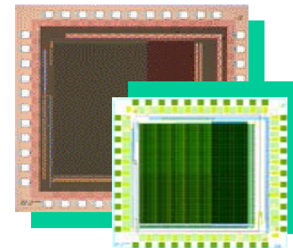
- Imaging detector with binary output for soft X-rays and electron microscopy

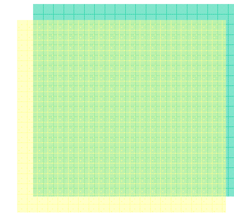
  (counting applications)

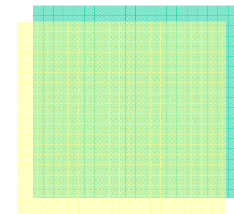


R. Yarema, FNAL, Vertex 2007

LBNL: LDRD-SOI







<u>**OKI 0.15μm FD-SOI**</u>
LDRD-SOI-1 (2007): 10μm pixels, analog & binary pixels

<u>**OKI 0.20μm FD-SOI**</u>
LDRD-SOI-2 (2008): 10μm pixels, analog & binary pixels (in-pixel time stamp)

M. Battaglia, ILC VXD Review, 2007

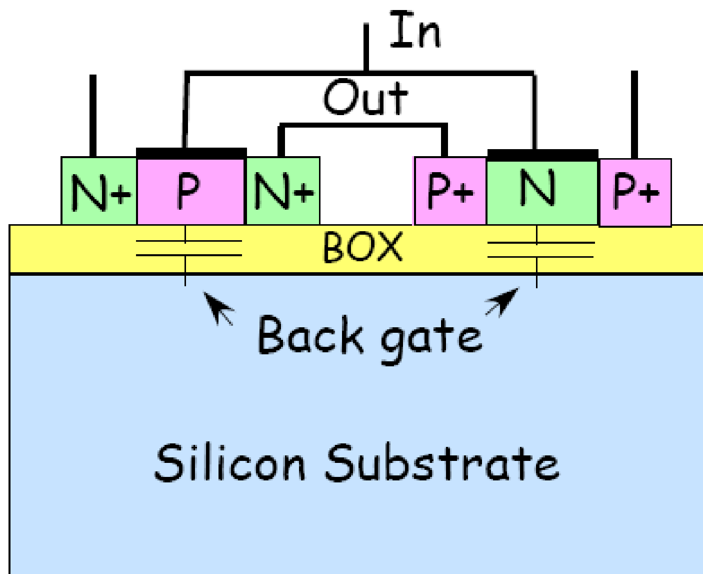
Potential problems in SOI detectors

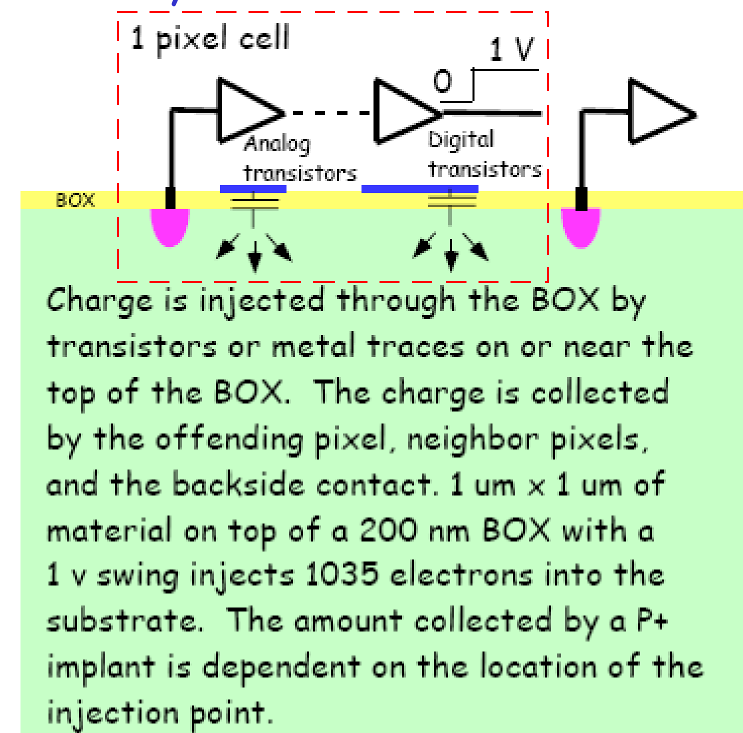
- Backgating effects

  Buried oxide acts as a back gate for MOSFETs

  ⇒ signal coupling, threshold voltage affected by substrate depletion voltage,...

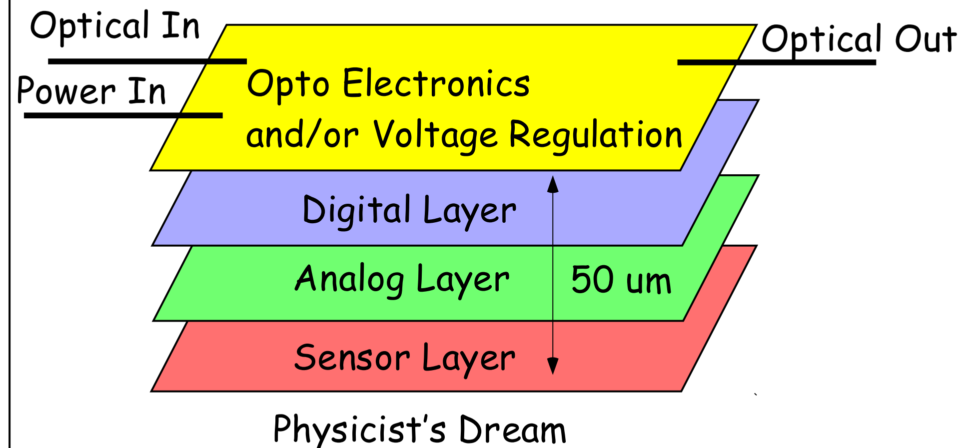
  ⇒ could be minimized by acting on device layout, by having no active circuitry during signal acquisition,....



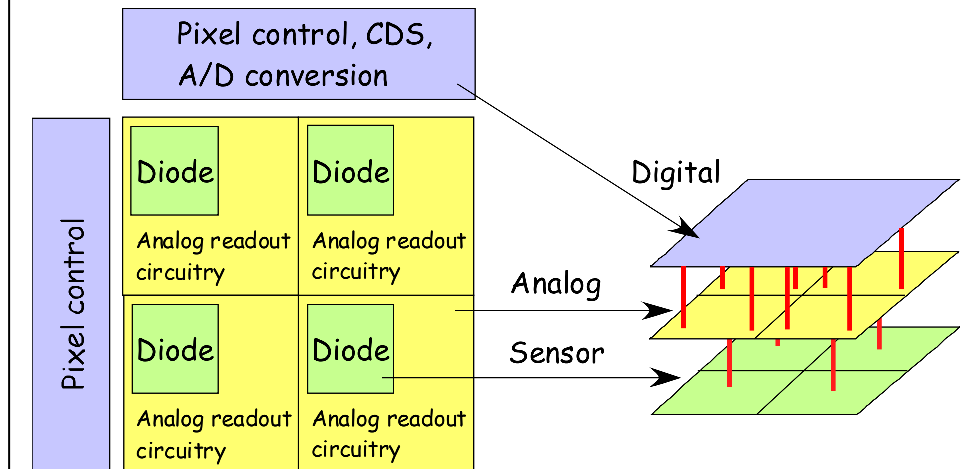


Vertical integration technologies

- A 3D chip is generally referred to as a chip comprised of 2 or more layers of active semiconductor devices that have been thinned, bonded and interconnected to form a "monolithic" circuit.
- Often the layers (sometimes called tiers) are fabricated in different processes.
- Industry is moving toward 3D to improve circuit performance.
  - Reduce R, L, C for higher speed
  - Reduce chip I/O pads
  - Provide increased functionality
  - Reduce interconnect power and crosstalk
- This is a major direction for the semiconductor industry.



Physicist's Dream



Conventional MAPS 4 Pixel Layout

3D 4 Pixel Layout

Active Pixel Sensors and Vertical Integration Technologies

- The very crowded zoo of vertical integration processes can be reduced to two different basic approaches (and technical problems):

1. Interconnection between a CMOS readout electronics chip (2D or 3D) and a fully-depleted high resistivity sensor

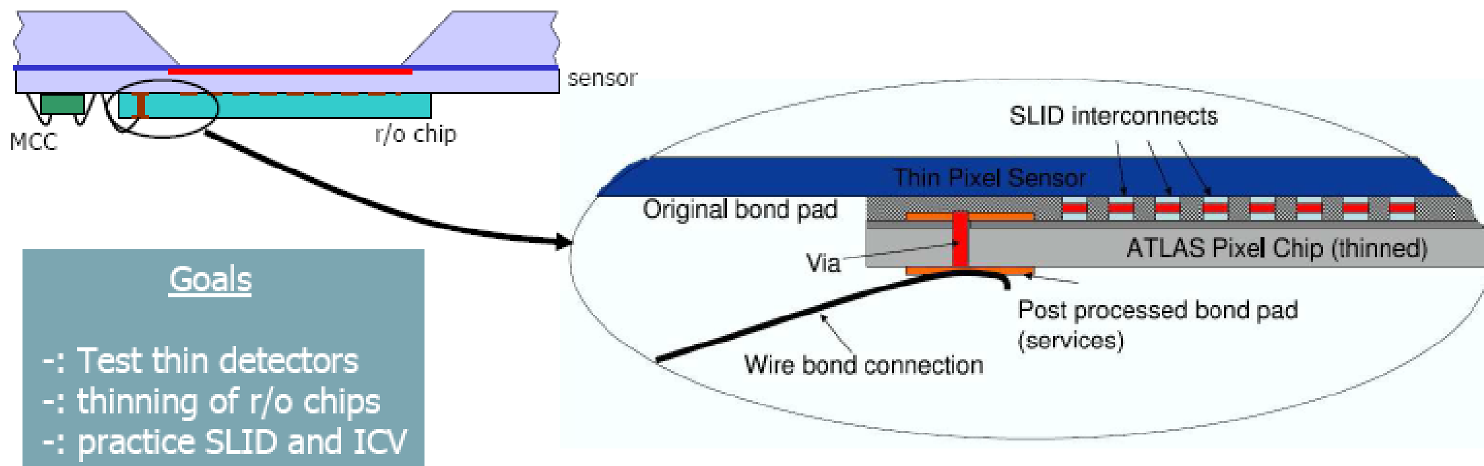
2. Interconnection between 2 (or more) layers, one with a MAPS (DNW) device and analog front-end, and the other layer(s) with the digital readout

Vertical integration between readout chip and fully depleted sensor

- Example: ICV-SLID technology developed by Fraunhofer-IZM and MPI-HLL

- sLHC: R&D Program 2007 - 2009 → Demonstrator

Existing ATLAS Pixel chip (FE-I3) face-to-face attached to a thin sensor!



Goals

-: Test thin detectors
-: thinning of r/o chips
-: practice SLID and ICV

MAPS and Vertical Integration

- Vertical integration between two layers of 130nm CMOS chips.

  The first layer may include a MAPS device with analog readout, and the second layer the digital readout circuits

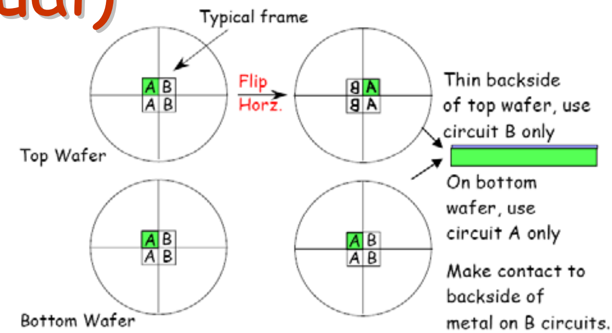
  (from an idea of Ray Yarema)

- Overcome limitations typically associated to "conventional" and DNW CMOS MAPS:
  - Reduced pixel pitch
  - 100 % fill factor (few or no PMOS in the sensor layer)
  - Better S/N vs power dissipation performance (smaller sensor capacitance)
  - Reduction of possible analog-to-digital interferences
  - Increased pixel functionalities (multiple hit handling, analog information)

3D vertical integration based on DNW MAPS (conceptual)

Use vertical integration technology to interconnect two 130nm CMOS layers

(R. Yarema)

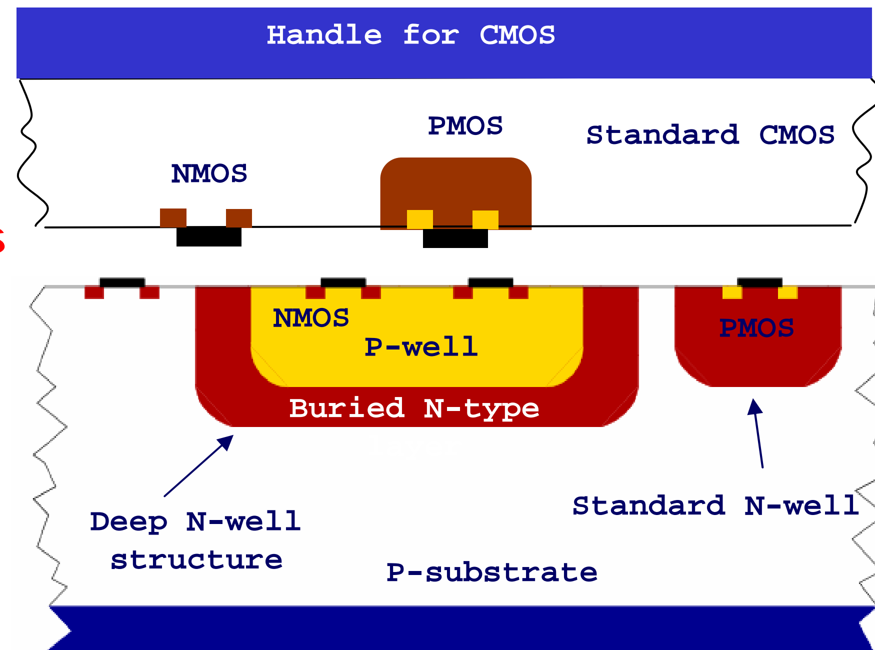


Face to Face Bonding

Mostly digital CMOS tier

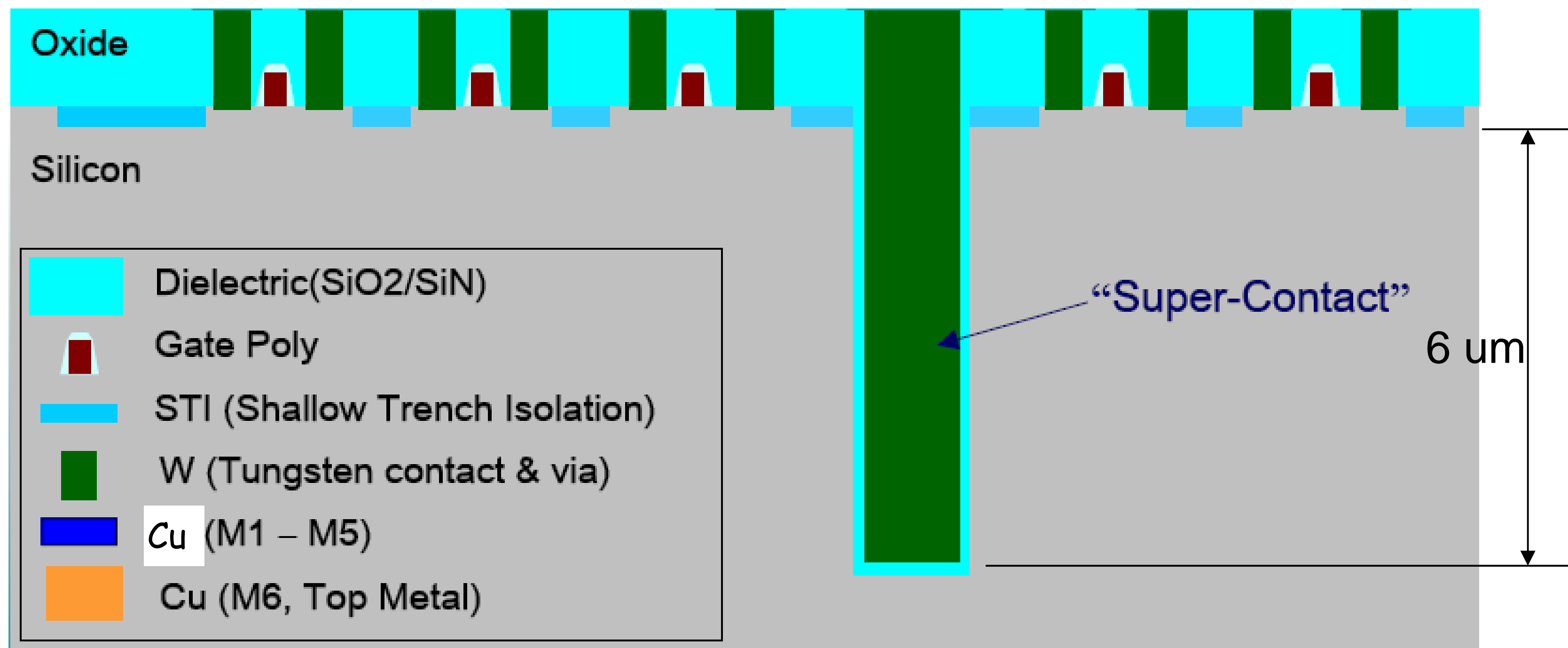
Tier interconnection and vias with industrial technique

Analog and sensor CMOS (mostly NMOS) tier



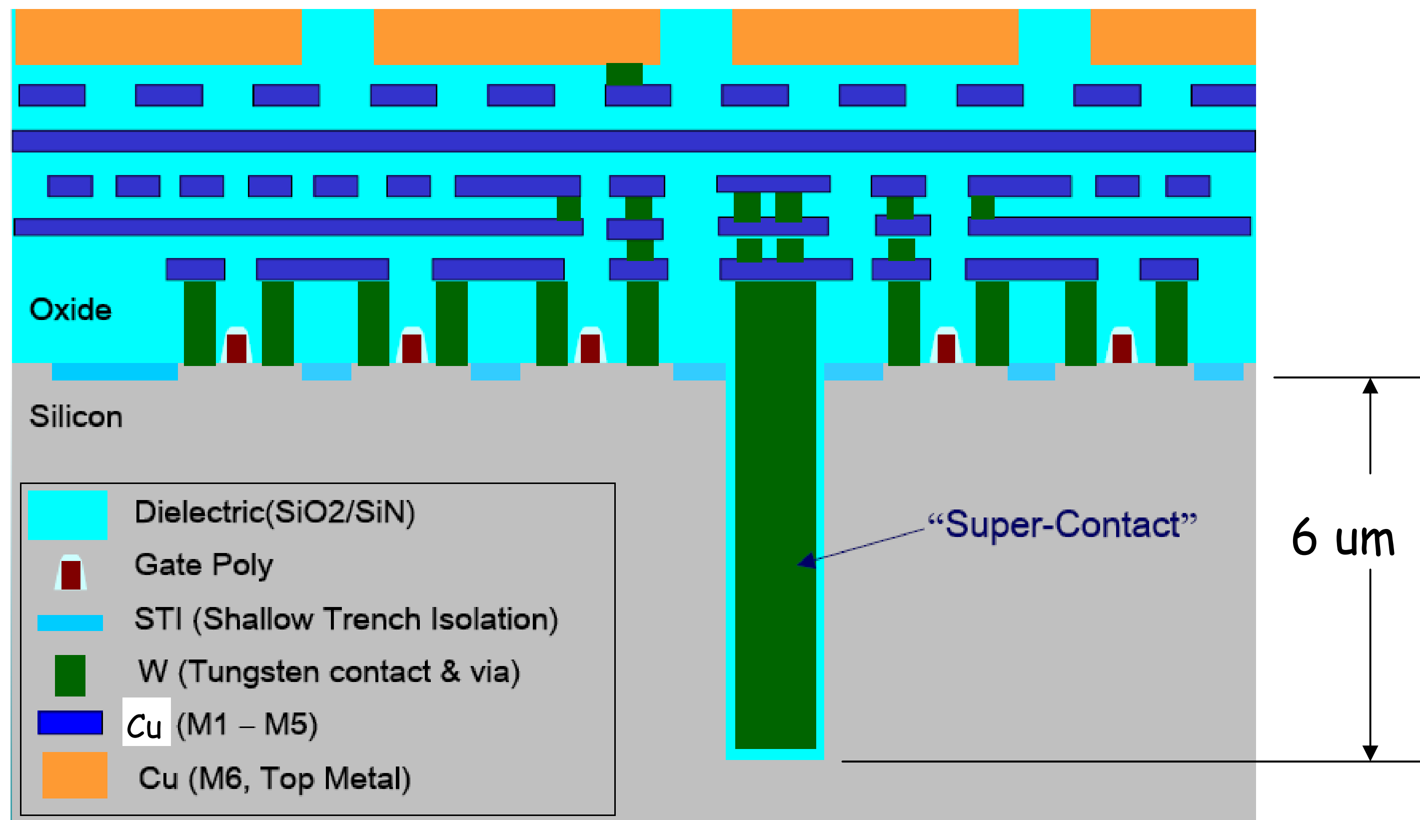
Tezzaron 3D Process

- Complete transistor fabrication on all wafers to be stacked
- Form super via on all wafers to be stacked
- Fill super via at same time connections are made to transistors



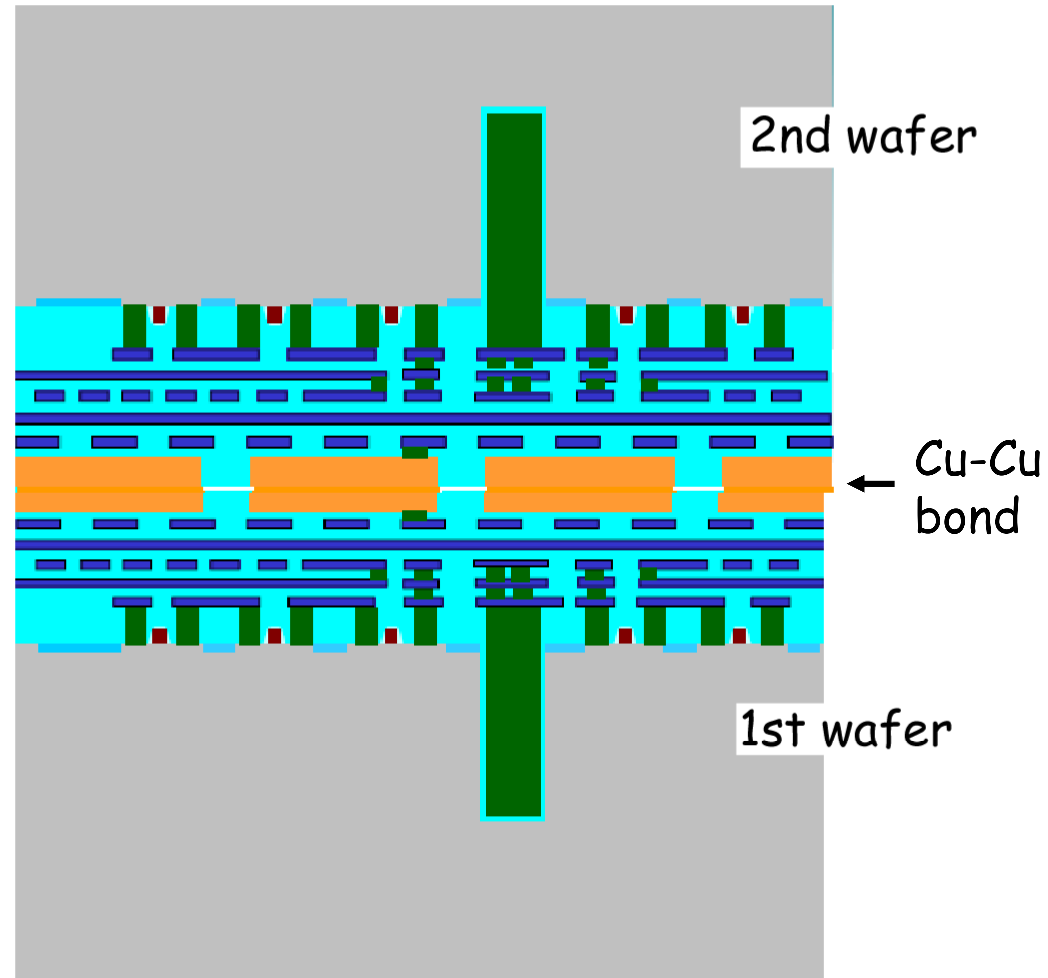
Tezzaron 3D Process

- Complete back end of line (BEOL) processing by adding Cu metal layers and top Cu metal (0.8 um)



Tezzaron 3D Process

- Bond second wafer to first wafer using Cu-Cu thermo-compression bond

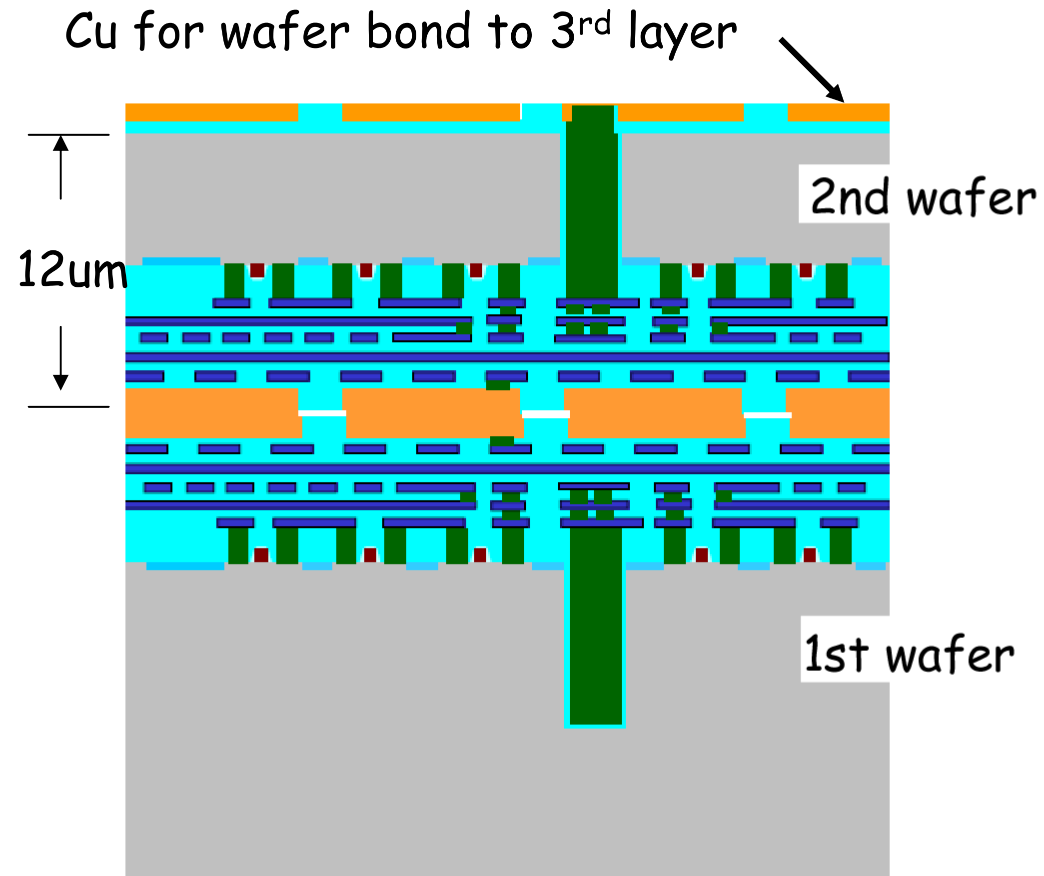


Tezzaron 3D Process

- Thin the second wafer to about 12 um total thickness to expose super via.
- Add Cu to back of 2nd wafer to bond 2nd wafer to 3rd wafer

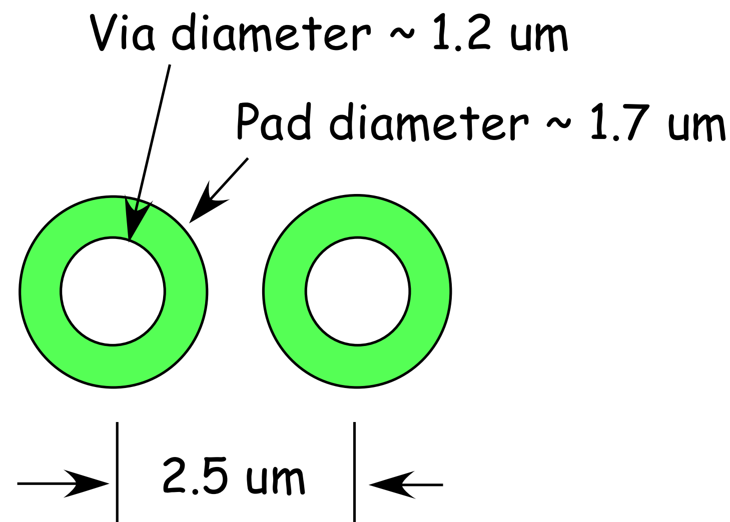
  OR

  add metallization on back of 2nd wafer for bump bond or wire bond.



Tezzaron vias

- Via size plays an important role in high density pixel arrays
- Tezzaron can place vias very close together



Wafer Bonding

- Bonding performed at 40 PSI and about 375 degrees C.
- Bonding done with improved EVG chuck
  - 3 sigma alignment = 1 um
- Missing bond connections = 0.1 PPM
- Temp cycling of bonds from -65 to + 150 C
  - 100 devices, 1500 cycles, 2 lots, no failures

3D MPW run

- Minimal material added with bond process
  - 35% coverage with 1.6 um of Cu gives Xo=0.0056%
  - No material budget problem associated with wafer bonding.
- Process supported by commercial tools and vendors
- Fast assembly and lower cost
- Fermilab will be the broker of a 3D multi project run using Tezzaron.
- There will be only 2 layers of electronics fabricated in the Chartered 0.13 um process, using only one set of masks. (Useful reticule size 16 x 24 mm)
- The wafers will be bonded face to face.
- INFN will join the run in the frame of a collaboration between microelectronics groups in U.S.A. and France

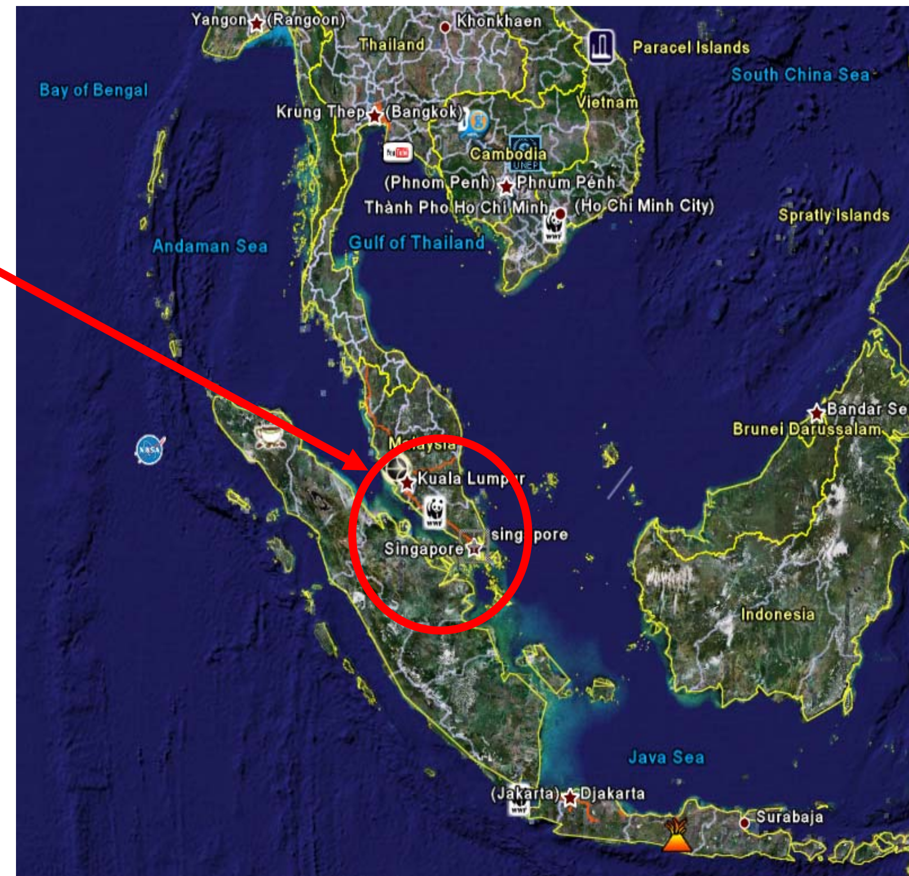
Conclusions

- **130 nm 3D Active Pixel Sensors have the potential for a big performance breakthrough targeting SuperB**
- Advanced microelectronic technologies provide exciting opportunities for high performance MAPS
- A lot of work is needed to qualify these technologies for the next generation of HEP experiments

Backup slides

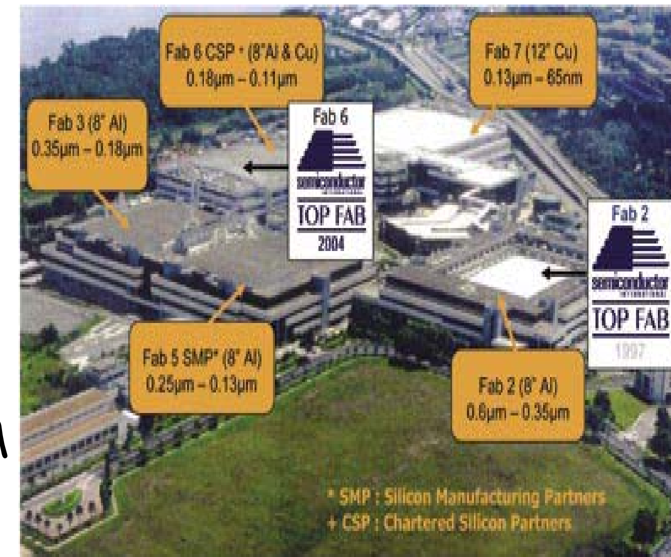
Tezzaron Background

- Founded in 2000, located in Naperville, Illinois
- Has fabricated a number of 3D chips for commercial customers
- Tezzaron uses the "Via First" process
- Wafers with "vias first" are made at Chartered Semiconductor in Singapore.
- Wafers are bonded in Singapore by Tezzaron.
  - Facility can handle up to 1000 wafers/month
- Bonded wafers are finished by Tezzaron
  - Bond pads
  - Bump bond pads
- Potential Advantages
  - Lower cost
  - Faster turn around
  - One stop shopping!!
- Process is available to customers from all countries



Chartered Semiconductor

- One of the world's top dedicated semiconductor foundries, located in Singapore, offering an extensive line of CMOS and SOI processes from 0.5 um down to 45 nm.
- Offers Common Chartered-IBM platform for processes at 90 nm and below.
- Chartered 0.13 um mixed signal CMOS process was chosen by Tezzaron for 3D integration
  - Chartered has made nearly 1,000,000 eight inch wafers in the 0.13um process
- Extension to 300mm wafers and 45nm TSVs underway
- Chartered 0.13 um process has different layer arrangement and transistor thresholds than IBM process.
- Commercial tool support for Chartered Semiconductor
  - DRC – Calibre, Hercules, Diva, Assura
  - LVS - Calibre, Hercules, Diva, Assura
  - Simulation – HSPICE. Spectre, ELDO, ADS
  - Libraries – Synopys, ARM, Virage Logic



Chartered Campus

Chartered 0.13 um Process

- 8 inch wafers
- Large reticule – 24 mm x 32 mm
- Features
  - Deep N-well
  - MiM capacitors – 1 fF/um^2
  - Reticule size 24 x 32 mm
  - Single poly
  - 8 levels of metal
  - Zero Vt (Native NMOS) available
  - A variety of transistor options with multiple threshold voltages can be used simultaneously
    - Nominal
    - Low voltage
    - High performance
    - Low power

Eight inches

Circuit Performance

- Circuits tested with full substrate thickness and then after bonding and thinning to 12 um
  - No change in performance between thinned and bonded devices and unthinned/unbonded devices.
    - Bandgap circuit
    - Sense Amplifier
    - Charge pump
  - No change in performance between thinned and bonded devices before and after temperature cycling.
- Transistor measurements on same devices before and after thinning and bonding are shown on the next slide.
  - No noticeable difference in characteristics except small increase in PMOS speed due to strain in silicon as expected