Towards ALCOR-64

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INFN Torino

Giornate Nazionali EIC_NET 2023

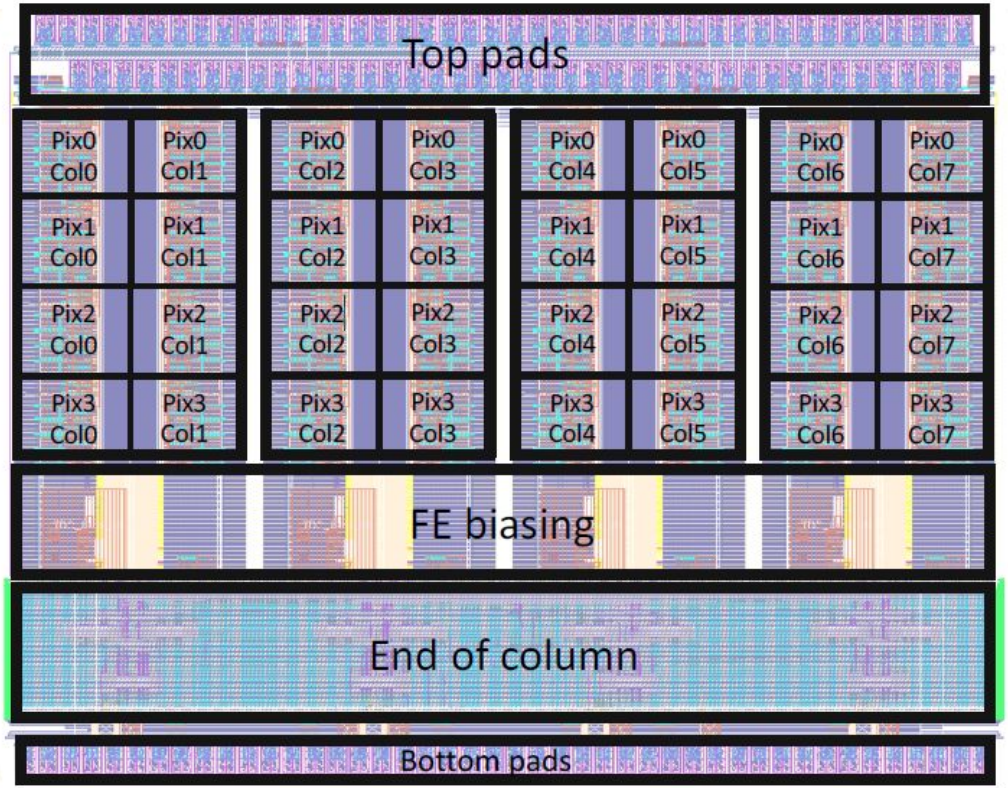
Corigliano-Rossano - 23.06.2023

Outline

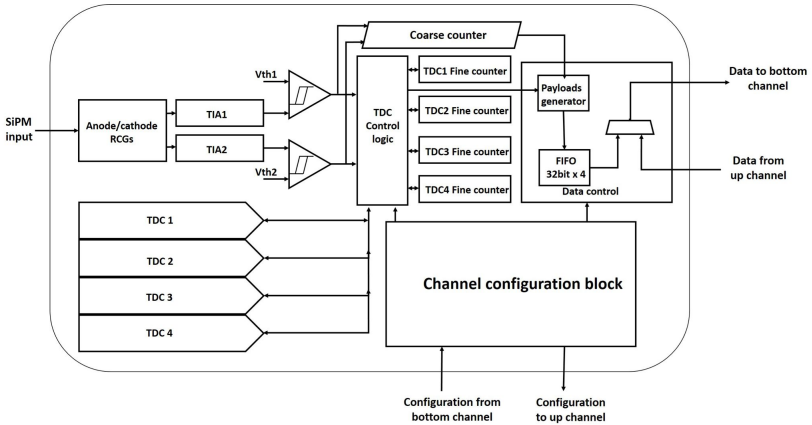
- ALCOR ASIC architecture overview
- ALCOR versions history
- Plans for next version: ALCOR-64
  - ALCOR packaging
  - ALCOR design upgrades
- Conclusions

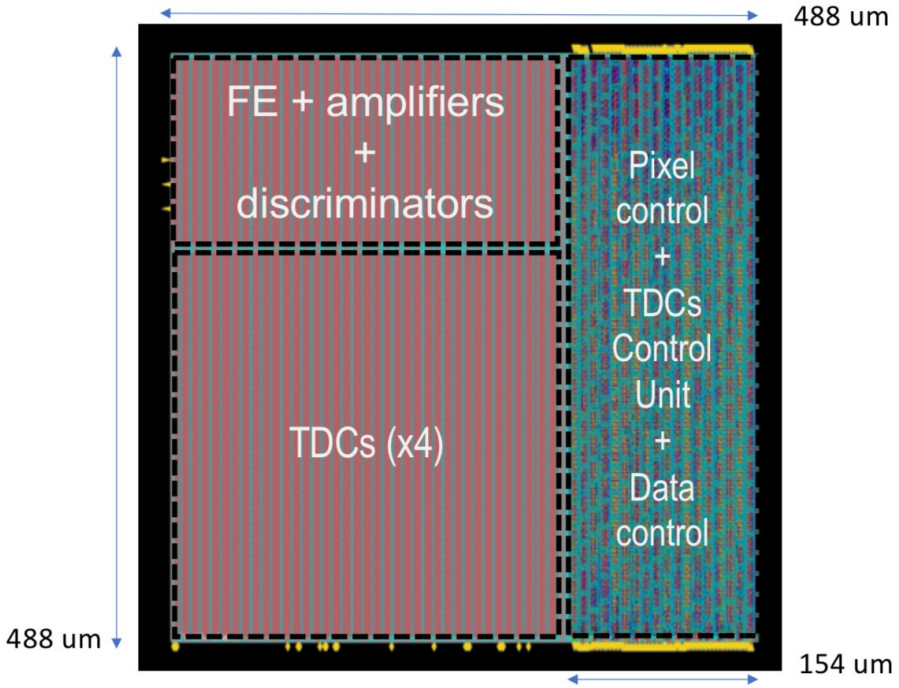
ALCOR ASIC

- Developed for the readout of SiPMs at 77K, in the framework of Darkside
- 32-pixel matrix (8x4) mixed-signal ASIC
- Single-photon time tagging + Time-over-Threshold measurement
- 32-bit (64-bit in ToT mode) event word generated on-pixel and propagated down the column
- Fully digital output: 4 LVDS 320 MHz DDR Tx links



Pixel architecture



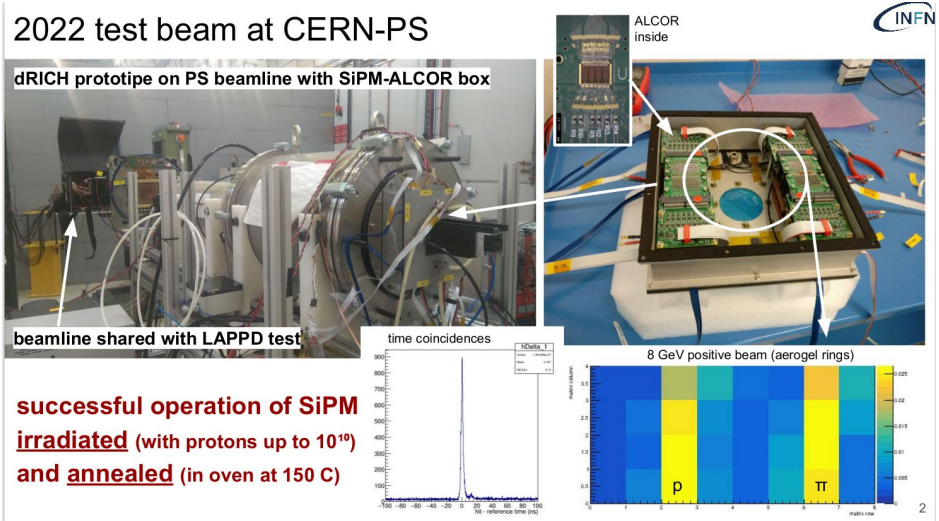


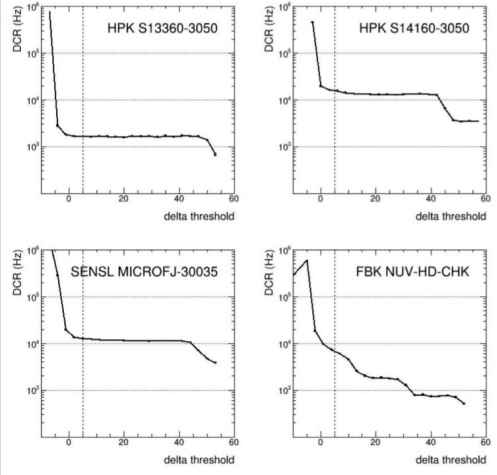
- TIA amplifier with RCG input stage
- 2 independent post-amp branches with 4 gain settings
- 2 leading edge discriminators with independent (and per pixel) threshold settings (6-bit DAC)
- 4 TDCs based on analogue interpolation with 25-50 ps time-bin (at 320 MHz clock frequency)
- Pixel control logic handles TDC operation, pixel configuration and data transmission

ALCOR v1

- MPW, submitted in Dec 2019
- Developed for the readout of SiPMs at 77K, in the framework of Darkside
- Extensively used within the EIC dRICH framework in the last 2 years

Slides from R. Preghenella





1-pe plateau for FBK sensors (large 40 um) SPAD is very short

small amplitude signals seen by ALCOR? why? in principle FBK has similar capacitance / gain as HPK sensors

moreover the 1-pe plateau in FBK is not really a plateau

is ALCOR “more noisy” with FBK sensors? “less gainy” with FBK sensors?

need to better study how we couple ALCOR with the SiPM

ALCOR v2

- MPW, submitted in Dec 2022
- **~50-60 chips, received last week, tests started this week**

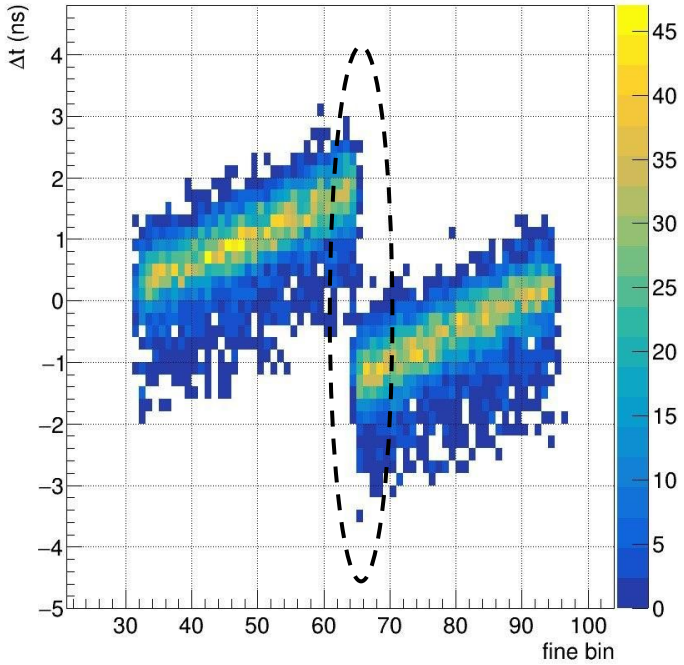
Bug fixes and new features

- TDC logic critical error at high rates almost solved
- Special words from EoC (header, frame, CRC) ok also when status words are disabled
- New FE gain settings more suited for single photon applications
- On-chip test-pulse also for EIC SiPM polarity

ALCOR v2.1

- INFN internal engineering run
- Submitted in Mar 2023, chips expected this Summer
- High number of chips will be available
- Corrected TDC logic bugs:
  - TFine-clock ambiguity
  - TOT orphans due to fake trigger at very low rates

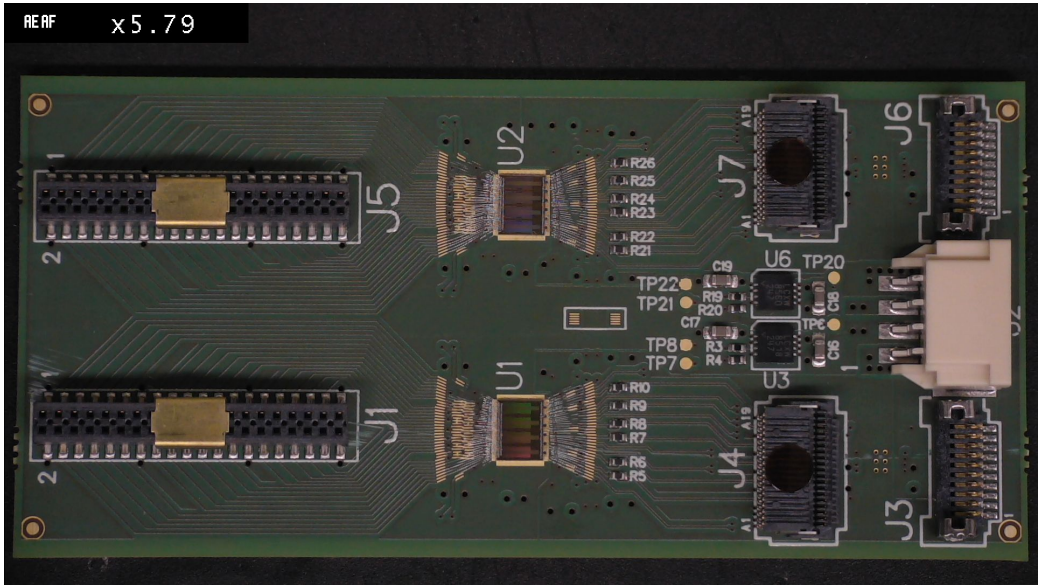
R. Preghenella



ALCOR 2023 readout system

ALCOR-FE-DUAL

- Two 32-channel ALCOR (v1 or v2) ASICs **wire-bonded** on the PCB
- This system will be used for 2023 beam tests



Towards ALCOR-64: ALCORv3

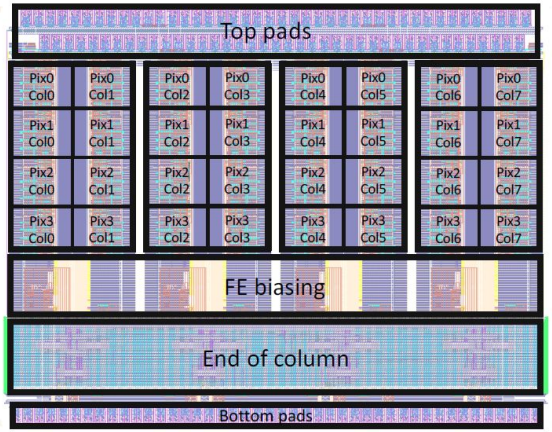
- **64-channel** version with shared digital signals and **BGA package** (~256 IO pins)
- Operation of ALCOR with multiple of EIC clock frequency (98.52 MHz): 295.56 MHz or **394.08 MHz**
  - First tests on ALCORv1 at 390 MHz look promising but more detailed tests and simulations are required, digital implementation must be re-done with new constraints
- Revise **ALCOR FE** design to improve time resolution and rate capability of the SiPM+ALCOR system
  - Studies on SiPM capacitance and optimal coupling with ALCOR (AC coupling inside ALCOR)
  - Increase amplifier bandwidth
  - Improve response for afterpulses and re-triggering (hysteresis discriminator)
- **Digital logic** bug fix and new features
  - TDC logic fix to remove orphans due to re-triggering of events very close in time
  - Increase EoC FIFO size to cope with higher data rates
  - Digital shutter for data reduction
  - Revise data payload format to improve ToT data stream and reconstruction algorithm

ALCOR I/Os

ANALOGUE (top, 44+38=82)

- 16 AVDD + 4 AVDD_IO
- 16 AGND + 4 AGND_IO
- 4 AVSS

- 32 inputs
- 4 debug outputs
- 2 bias Vref



DIGITAL (bottom, 20+24=44)

- 6 DVDD + 2 DVDD_IO
- 6 DGND + 2 DGND_IO
- 4 DVSS

- 8 Tx outputs
- 2 clk, 2 reset, 2 test-pulse
- 8 SPI
- 2 clk_out

ALCOR current version has 32 channels and 126 I/Os

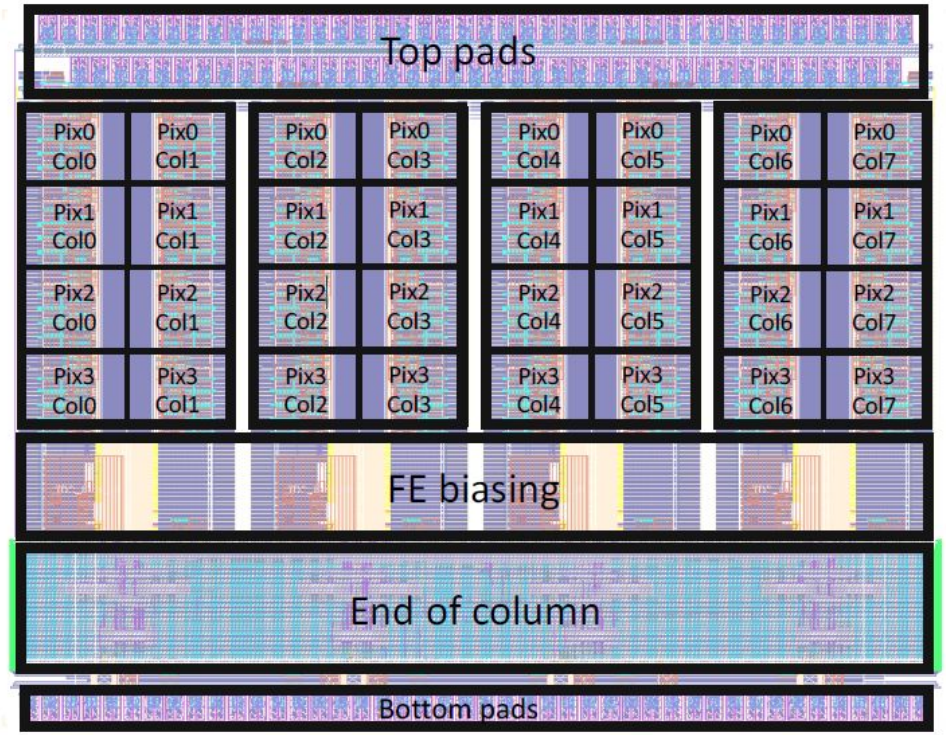
Targeting a 64-channel version with 256 I/Os

ALCOR-64

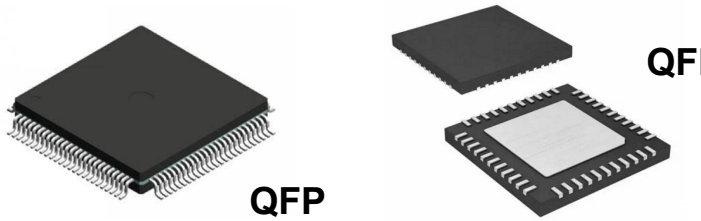
In **ALCOR-32** the space between each sector is used to route the pixels input to the Top pads (SiPMs signal)

ALCOR-64 → 8x8 pixel matrix, 256 IO pins

x2 increase of input channels → no space and pads to do routing from the Top pads

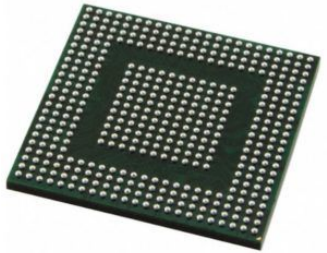


Standard packaging (QFP, QFN) is cheap but provides low number of pins and large area, which is not suitable for a good implementation of the 64-channel ALCOR



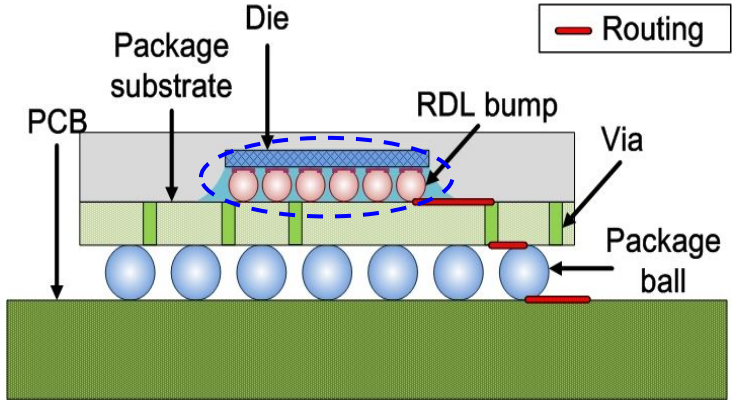
Flip-chip BGA packaging

BGA



Ball grid array package

- The whole bottom surface of the device can be used, not just the perimeter
- More interconnection pins wrt QFP or QFN
- Shorter interconnections reduce inductance, allows high-speed signals, and carrys heat better



Inside the package, the chip is flipped so that the active side of the device can be bump-bonded to the package substrate → each pixel can be directly connected to the outside

256 balls BGA

- 0.8 mm ball pitch → 13x13 mm^2 package
- 1.0 mm ball pitch → 16x16 mm^2 package

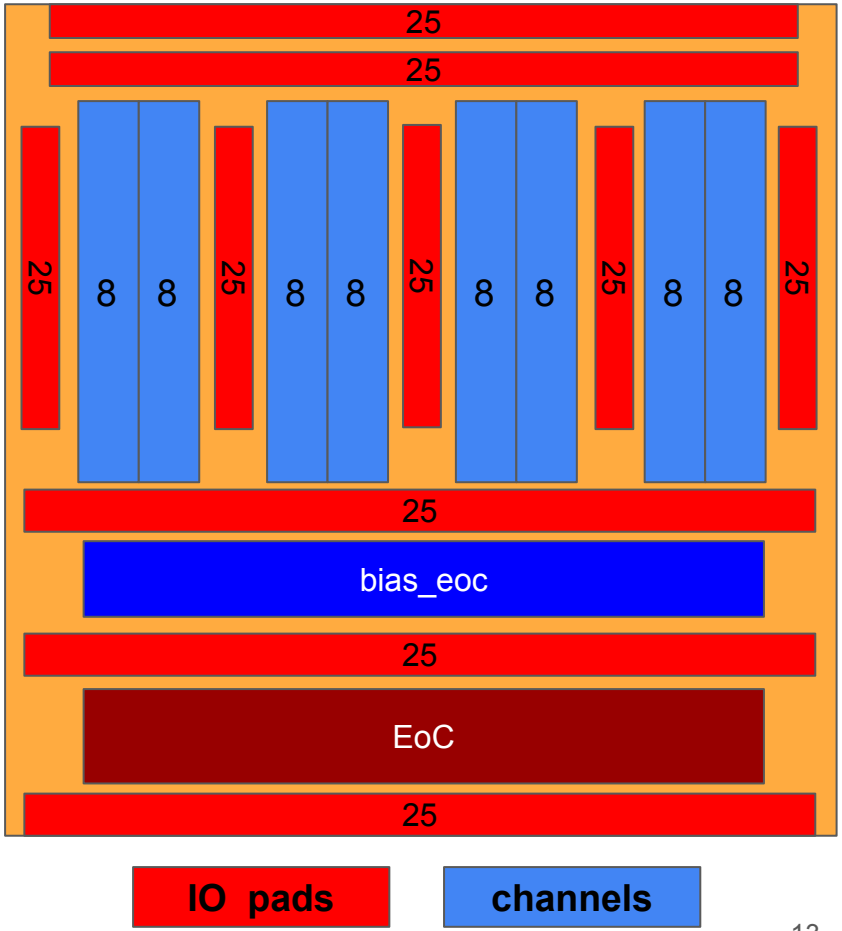
Foundry stopped support to RDL (redistribution layer): special layer for bump bonds interconnections

ALCOR-64 floorplan

Investigations with BGA manufacturers ongoing and they need **detailed floorplan** of the ASIC IOs to define best solution (and cost):

1. Use top metal layer (ME8) as RDL but this can affect power distribution
2. BGA manufacturer adapts package substrate to the bump pads geometry

In any case, having the **bump pads** array **distributed** and **uniform** across the chip (as much as possible) makes the design more feasible (and cheaper)



Digital shutter

ALCOR test pulse can also act as **“inhibit”** of the pixel digital logic and this can help to reduce data throughput

- Successfully used in beam tests to reduce occurrence of ALCORv1 TDC logic critical errors
- In EIC: 10 ns bunch crossing, 250 ps bunch length
- Select 1-2 ns → **5-10x data reduction** before ALCOR TDCs

Current version of ALCOR cannot work with such short shutter time interval

- Inhibit signal is **synchronous** with clock
- Issues if leading/trailing edges of discriminator signal are across the time window

Logic for asynchronous digital shutter implemented in ALCORv3

- Studies ongoing to define **delays** needed to guarantee same time window for all the channels
- Need to evaluate effect due to **time-walk** and **thresholds dispersion**

ALCOR v1 FE

PM5: input transistor (CG)

PM4: CG bias

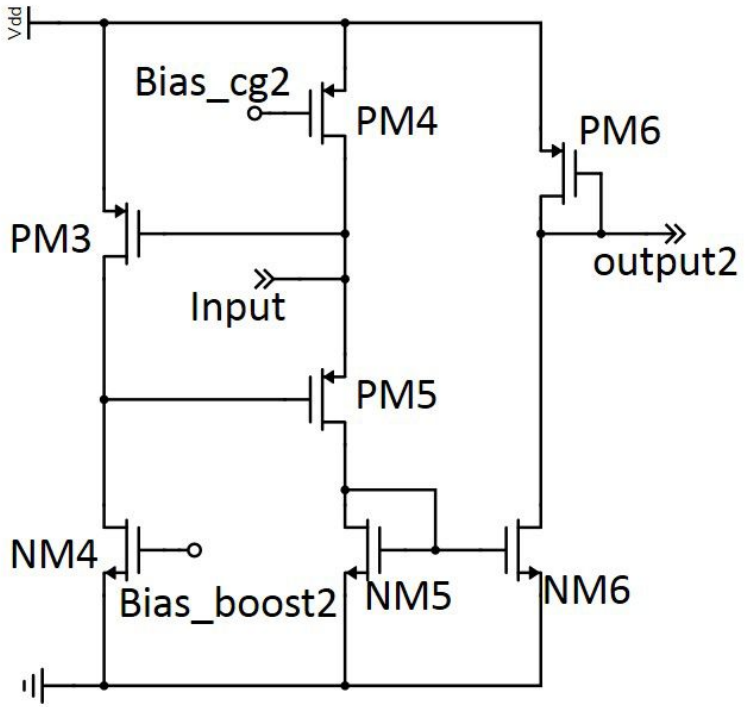
PM3: boost transistor

NM4: boost bias

PM3 + NM4 = CS amplifier

$A = gm_{PM3} \cdot R_p$

$Zin \simeq 1 / (A * gm_{PM5})$



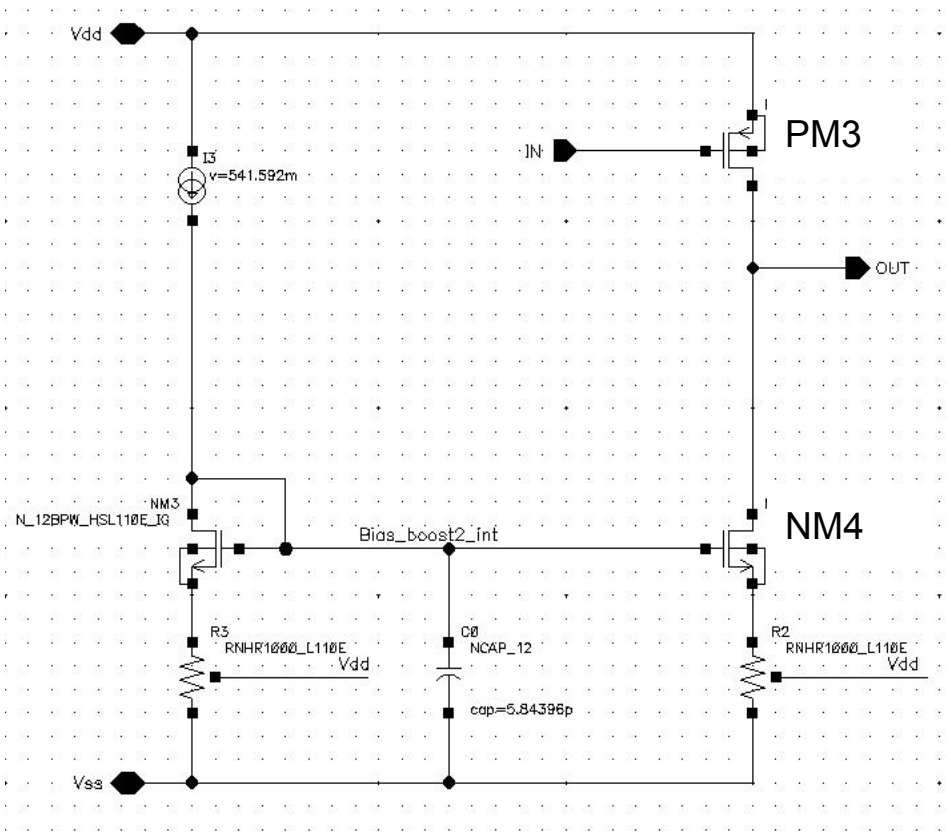
New FE (CS boost stage)

Boost bias transistor (NM4) with source degeneration to reduce its contribution to noise and increase output resistance

Zin ≃ 1 / (A * gm_{PM5})

$A = gm_{PM3} \cdot R_p$

Attention must be paid to small mismatches in the resistors and to the decreased voltage headroom

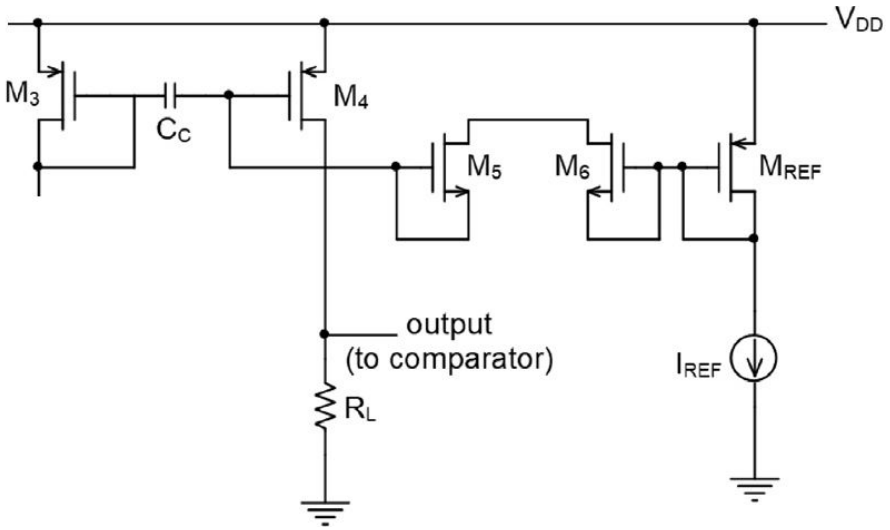


Internal AC-coupling

Input and output stages of ALCOR amplifier are AC-coupled via Cc

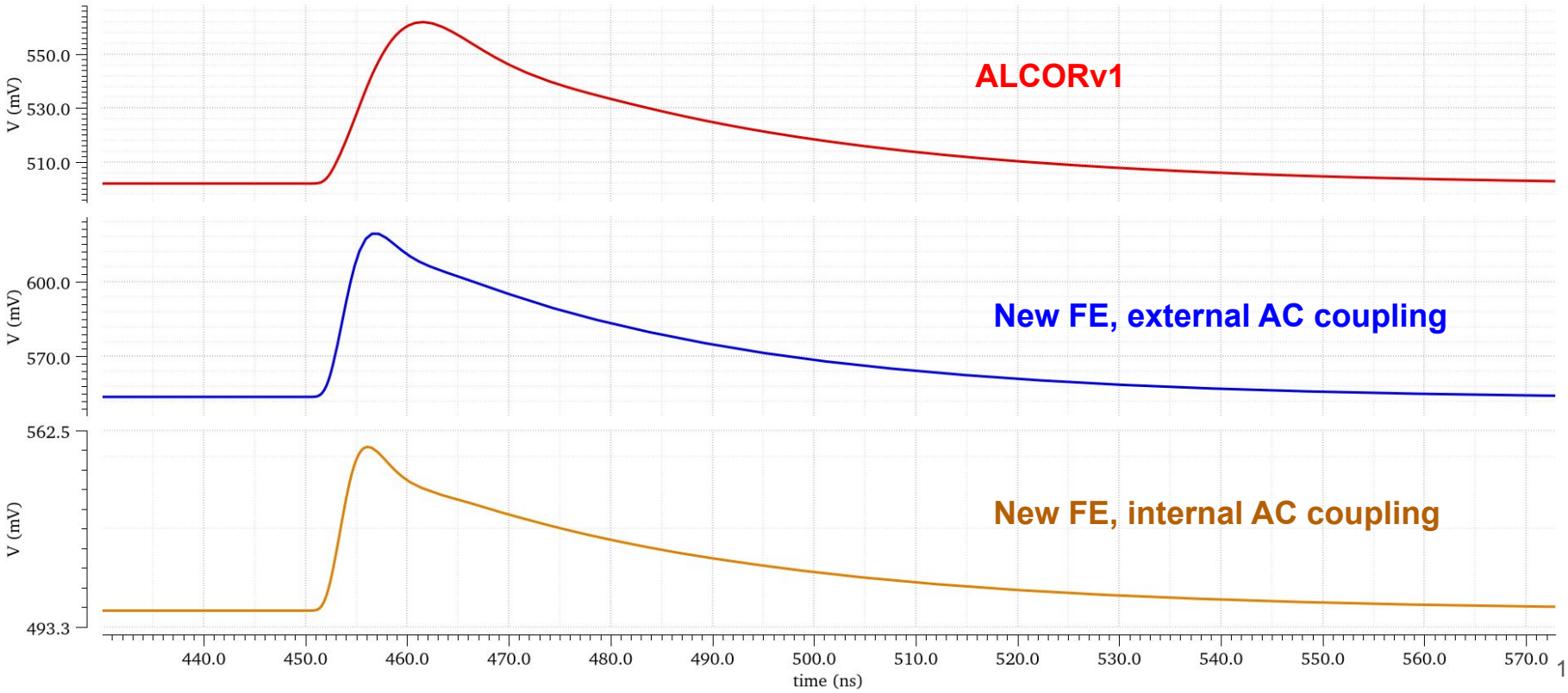
IREF and MREF set DC operating point of M4 via M5 and M6: back-to-back cut-off MOSFETS providing equivalent large resistor (~GΩ)

Baseline can be controlled using I_{REF}, using a simpler architecture w.r.t. the one implemented in ALCOR v1 with DC-coupled output stage

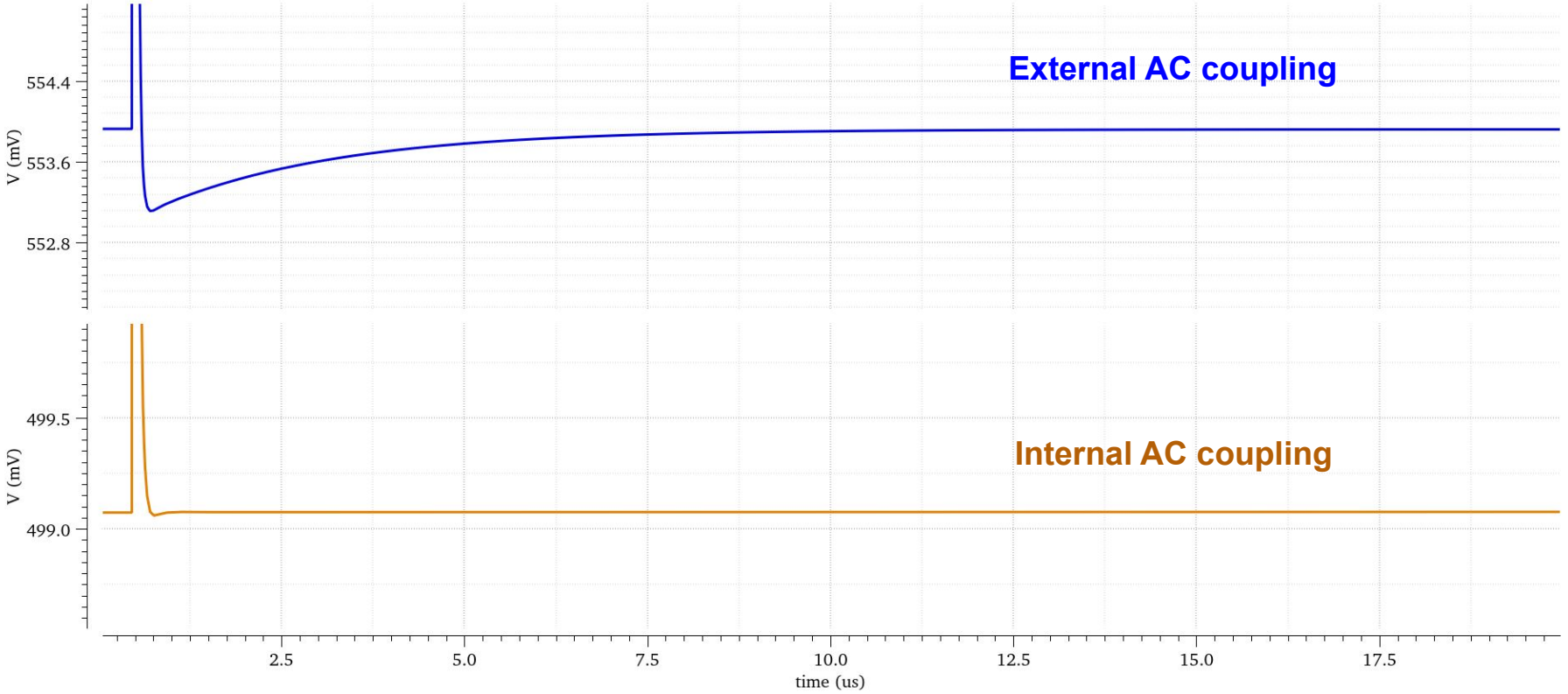


Input stage can be in principle DC-coupled to the SiPM → need to study interplay with annealing MOSFETs and SiPMs HV trim DACs

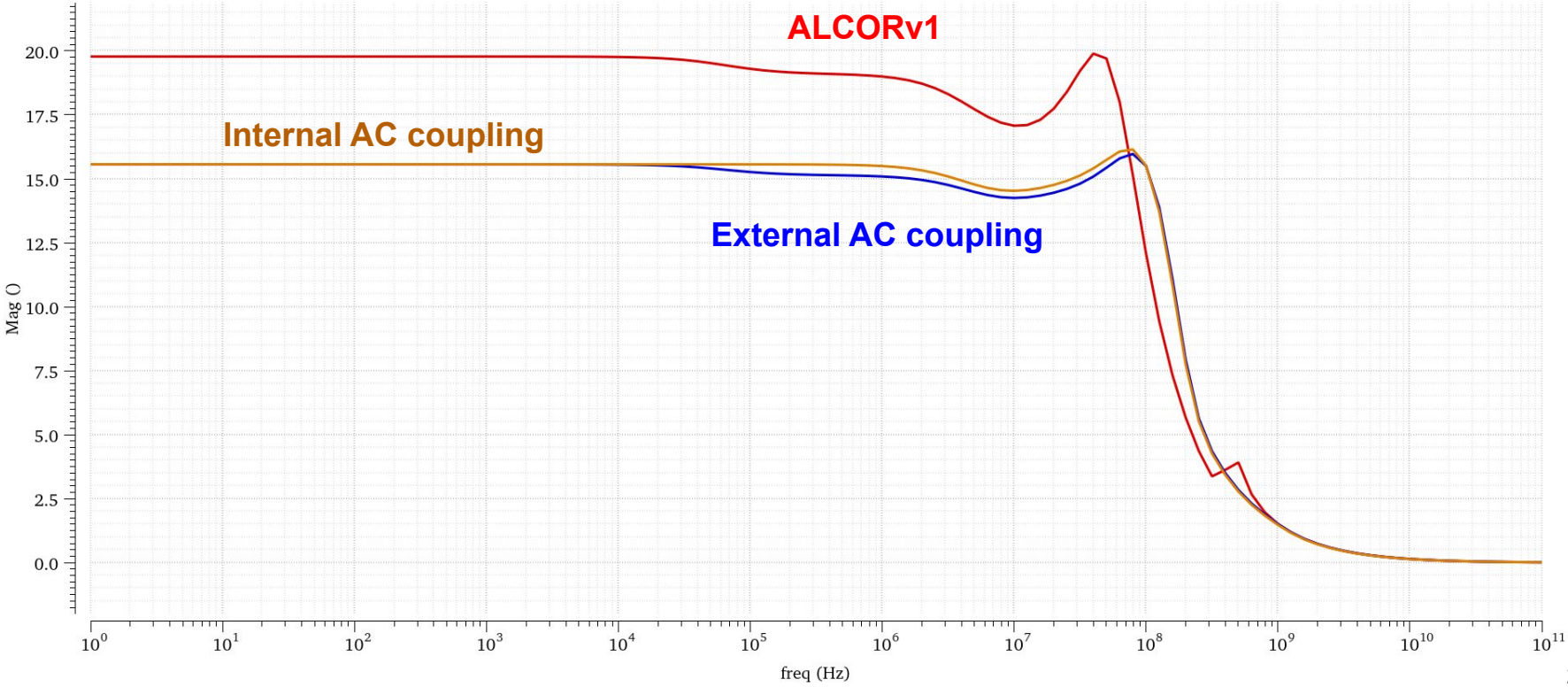
Transient simulation



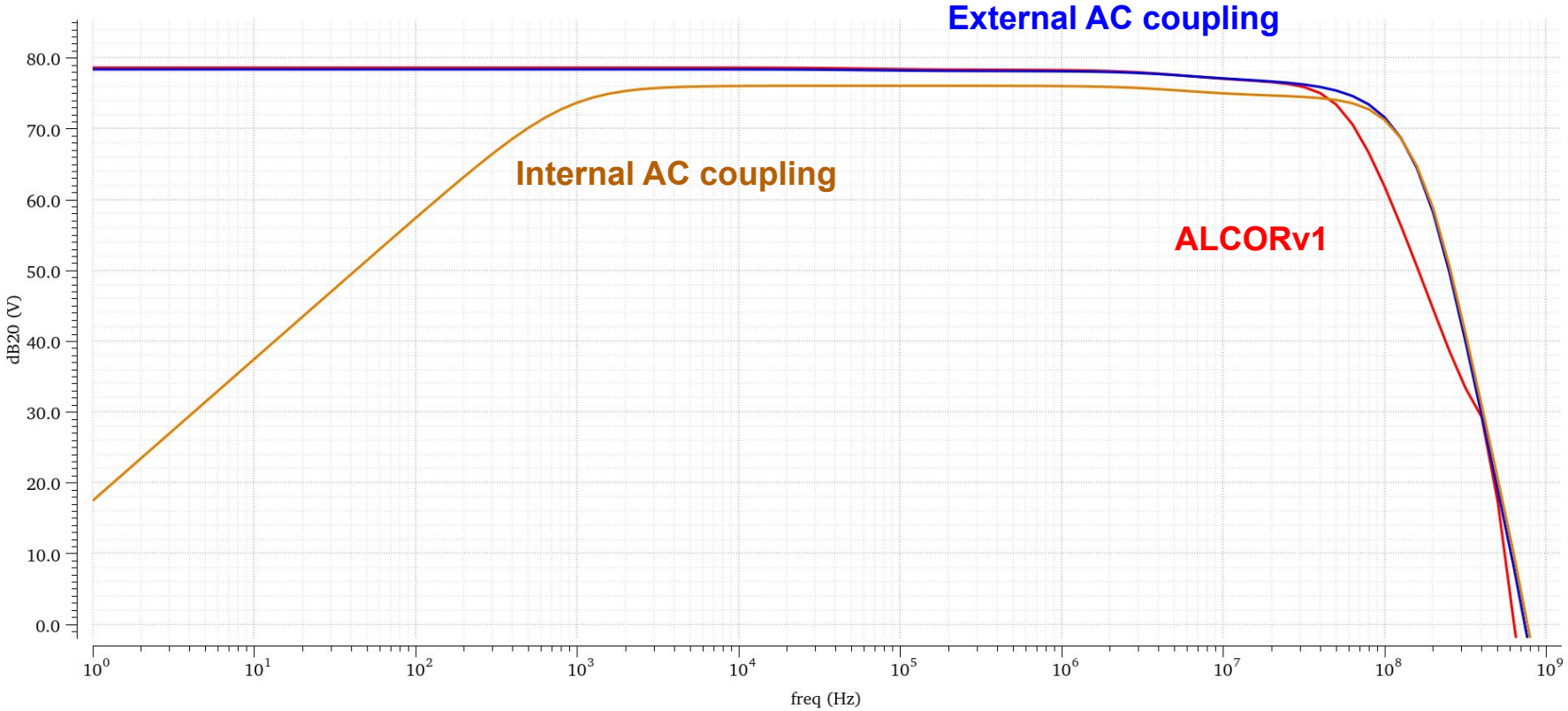
Return to baseline



Input impedance



Frequency response



Specs comparison

Schematic simulations with SiPM model: Hamamatsu S131360-3050, OV = 3 V

ALCORv1

RMSnoise	1.43 mV
SR	9.72 MV/s
jitter	147 ps
gain	221.4 mV/pC
SNR	41.9
rise_time	10.4 ns
Zin_DC	19.8 Ω

External AC coupling

RMSnoise	1.65 mV
SR	20 MV/s
jitter	82.6 ps
gain	243.5 mV/pC
SNR	39.7
rise_time	5.61 ns
Zin_DC	15.6 Ω

Internal AC coupling

RMSnoise	1.54 mV
SR	19.74 MV/s
jitter	77.9 ps
gain	198.9 mV/pC
SNR	37.5
rise_time	5.17 ns
Zin_DC	15.6 Ω

Summary and Outlook

- ALCOR v1 extensively used in the last two years within the EIC dRICH Collaboration
- ALCOR v2 just received: promising first results, start assembly of ALCOR-FE-DUAL for preparation of 2023 beam tests
- Works on ALCOR v3 ongoing
  - Studies and investigations on ALCOR packaging to find a baseline solution
  - Internal design upgrades providing improved performance and new features
- Thanks to EIC colleagues for their massive tests with ALCOR and the fruitful discussions which improved the overall understanding of the ASIC and the upgrades required for the EIC dRICH application

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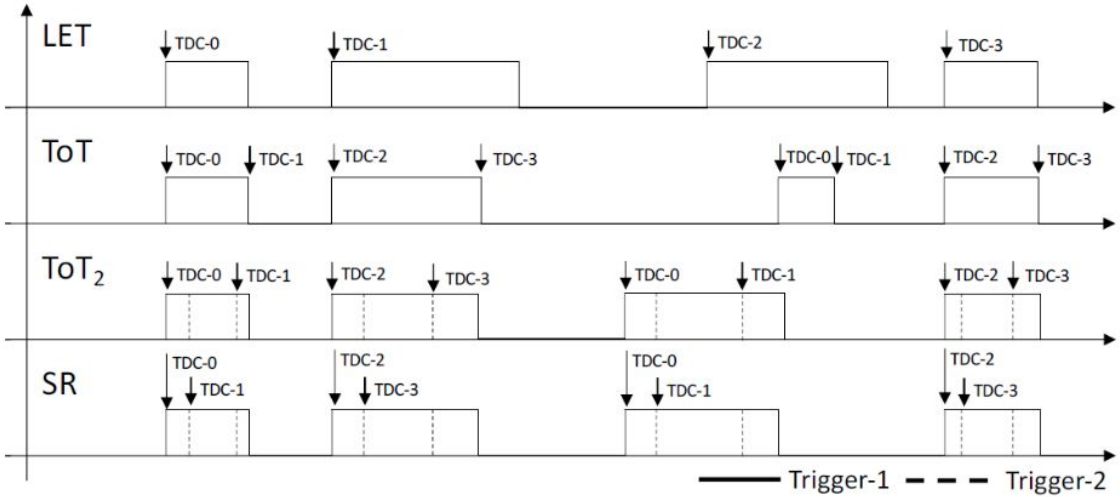
ALCOR pixel operating modes



4 operating modes:

- LET: leading edge measurement
- ToT: Time-over-Threshold measurement using the first discriminator for both edges
- ToT2: Time-over-Threshold measurement using both discriminators
- SR: slew-rate measurement

Each mode can be set to:

- FE: normal operation mode
- FE_TP: send test-pulse to analogue front-end
- TDC_TP: send test-pulse to pixel control logic to test and calibrate TDCs (bypass front-end)

Each pixel can also be disabled

Towards ALCOR-64

All sizes must be scaled by 0.9

Max size = 5.5 mm → 4.95 mm (0.9x scale factor)

ALCOR-32 dimensions (4.95 mm × 3.78 mm)

- **Pixel size**: 488.89 µm x 488.89 µm
- **Horizontal pixel pitch**: 1350/2 µm = 675 µm
- **Vertical pixel pitch**: 488.89 µm
- **EoC_bias height**: ~555 µm
- **EoC height**: ~800 µm
- **Serializer height**: ~120 µm
- **Padframe height**: 165 µm (ESD → 90 µm)
- **Padframe pitch**: 120 µm

➢ **8 columns pixel height** = 488.89 µm x 8 = 3911.12 µm

➢ **pixel column + EoC** = 3911.12 µm + 555 µm + 800 µm + 120 µm = **5386.12 µm**

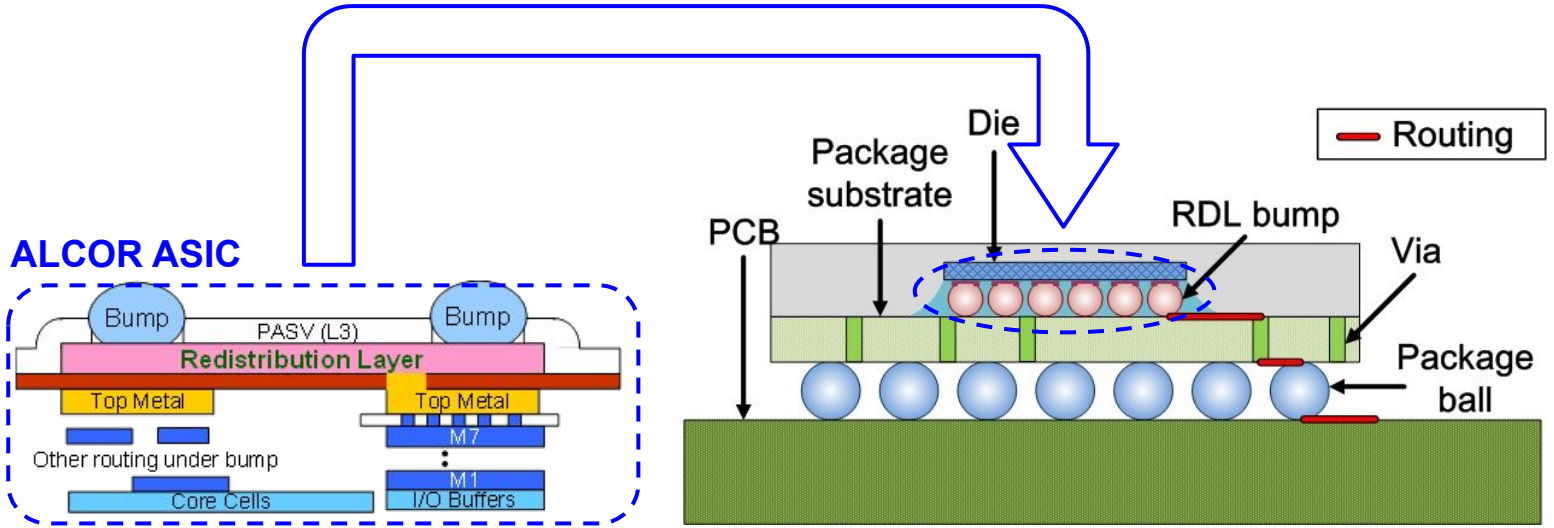
★ No space for padframe → we need to increase chip height above 5 mm


1
42
43
82
ALCOR
version 1
4.95 mm × 3.78 mm
(before optical scaling: 5.4942 mm x 4.1944 mm)
http://personalpages.to.infn.it/~fcossio/projects/ALCOR/ALCOR_user_guide.pdf
83
126

Flip-chip BGA packaging

Inside the package, the chip is flipped so that the active side of the device faces the package substrate to which it can be bump-bonded

→ Each pixel can be directly connected to the outside

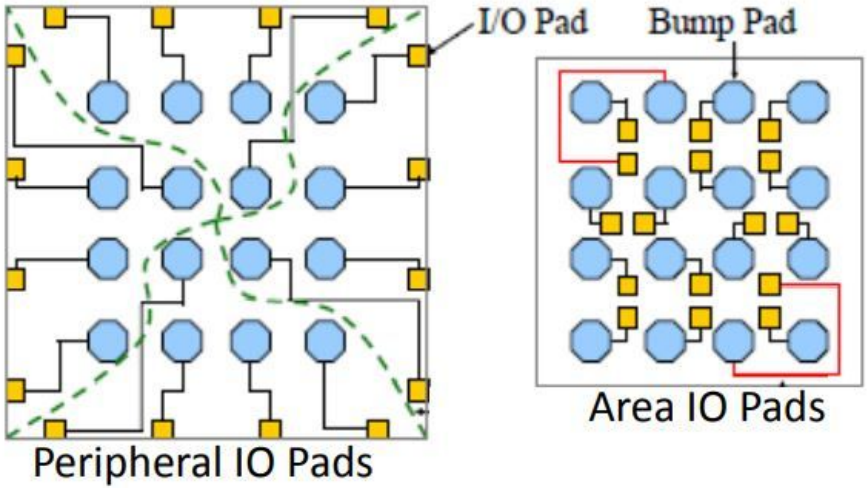


Flip-chip BGA packaging

Bump pads: pads to be connected to package interposer, usually placed in a grid pattern

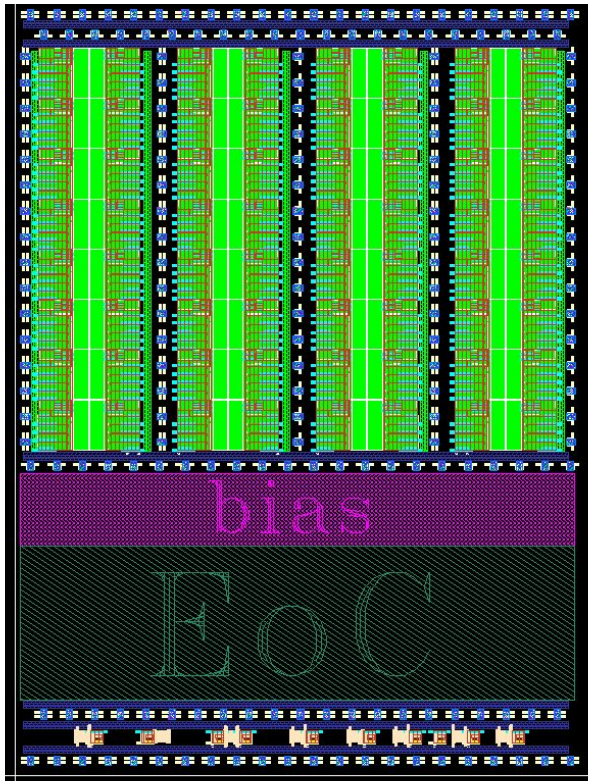
IO pads: pads providing connection to core cells of the chip, provide also ESD protection, geometry can be *peripheral* (wire-bond like) or *area*

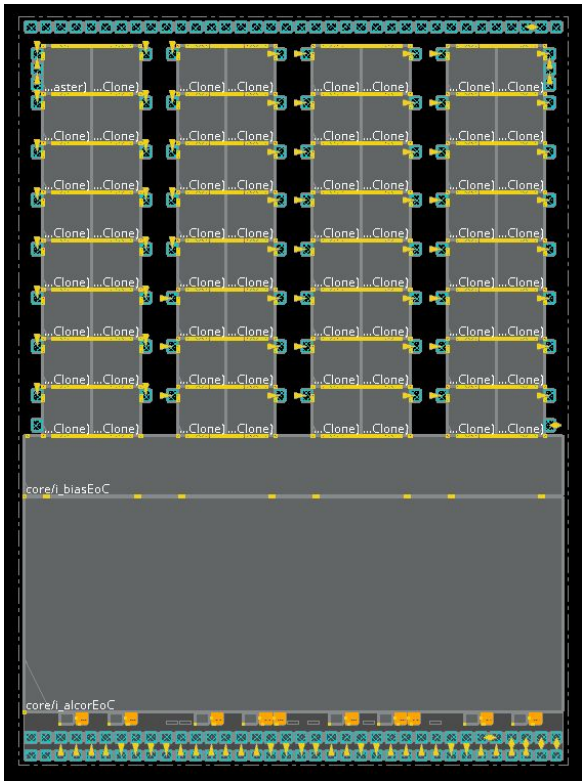
RDL (redistribution layer): extra metal layer connecting IO pads and bump pads



Support to RDL stopped by UMC, only METAL8 can be used to do the redistribution (no special layer)

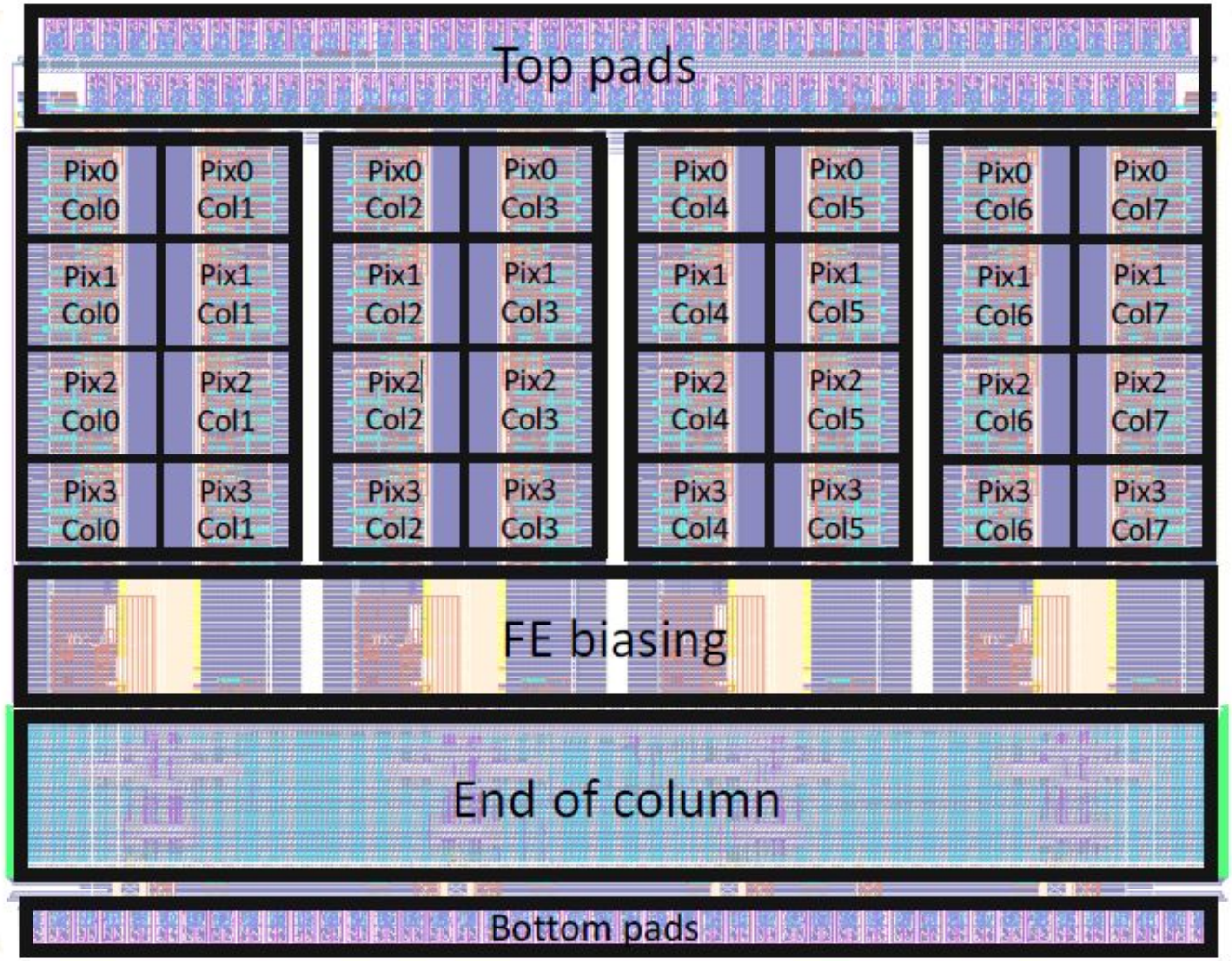
ALCOR-64 floorplan





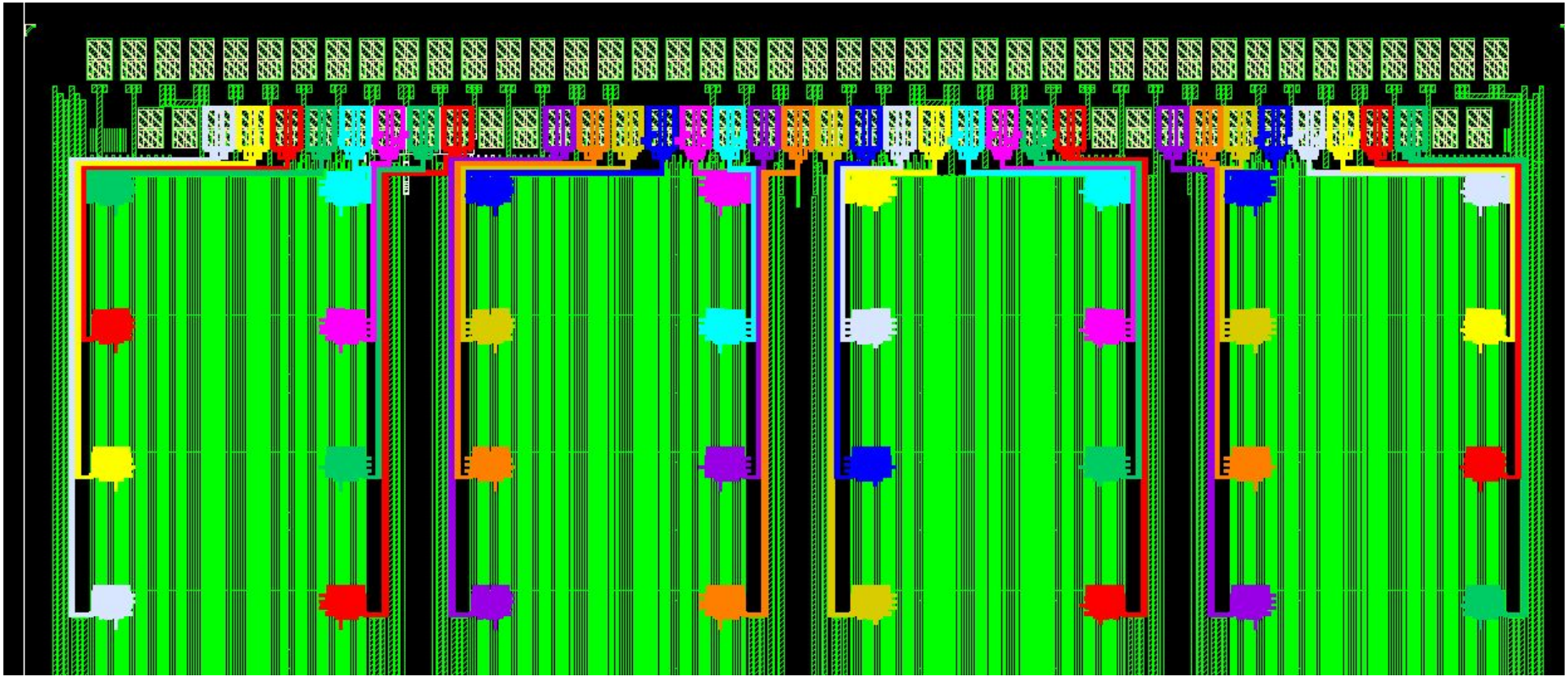
ALCOR-32

Space between each sector is used to route the pixels input to the Top pads and for decap capacitance



ALCOR-32

In ALCOR-32 the space between each sector is used to route the pixels input to the Top pads (going to the SiPMs)



ALCOR-64 I/Os

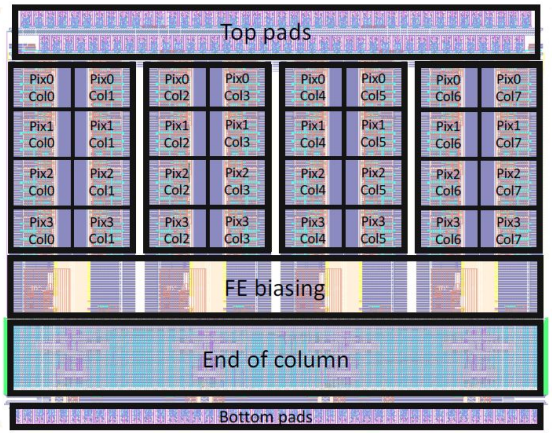
ANALOGUE (top)

- 32 AVDD + 8 AVDD_IO
- 32 AGND + 8 AGND_IO
- 8 AVSS

- 64 inputs
- 4 debug outputs
- 2 bias Vref

TOTAL = 88 + 70 = 158

2x



DIGITAL (bottom)

- 12 DVDD + 4 DVDD_IO
- 12 DGND + 4 DGND_IO
- 8 DVSS

- 16 Tx outputs
- 2 clk, 2 reset, 2 test-pulse
- 8 SPI
- 2 clk_out

TOTAL = 40 + 32 = 72

ALCORv3 64-channel version with 230 I/Os

ALCOR-64 wire-bond version (8x8 matrix)

Top side padframe is already staggered (2 rows)

- ❏ need to find where to put extra inputs and P/G pads
- ❏ need to to route input pads to input pixels

Only way seems to place padframe also on both sides of ALCOR to provide extra pads for:

- external columns pixel inputs (8 + 8)
- Power and Ground

★ <u>This implies that also the chip width will be > 5 mm</u>

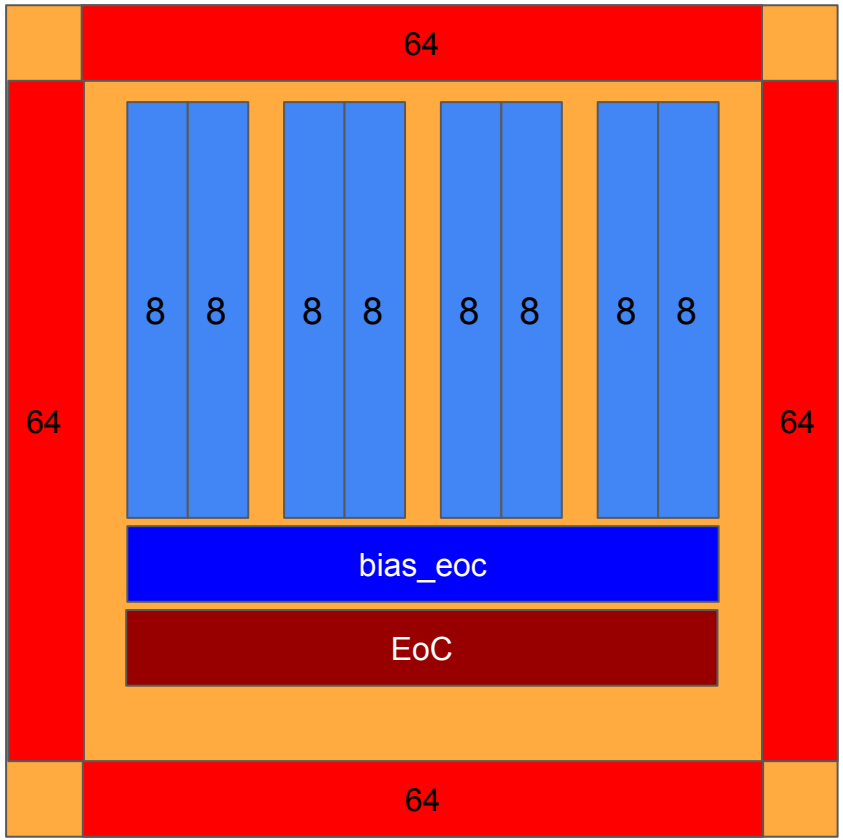
ALCOR-64 wire-bond version (8x8 matrix)

TOP (64)

- 48 inputs
- 8 AVDD
- 8 AGND

EAST/WEST (51)

- 8 inputs
- 12 AVDD
- 12 AGND
- 4 AVDD_IO
- 4 AGND_IO
- 4 AVSS
- 2 debug outputs
- 1 bias Vref
- ----------
- 2 DVDD
- 2 DGND



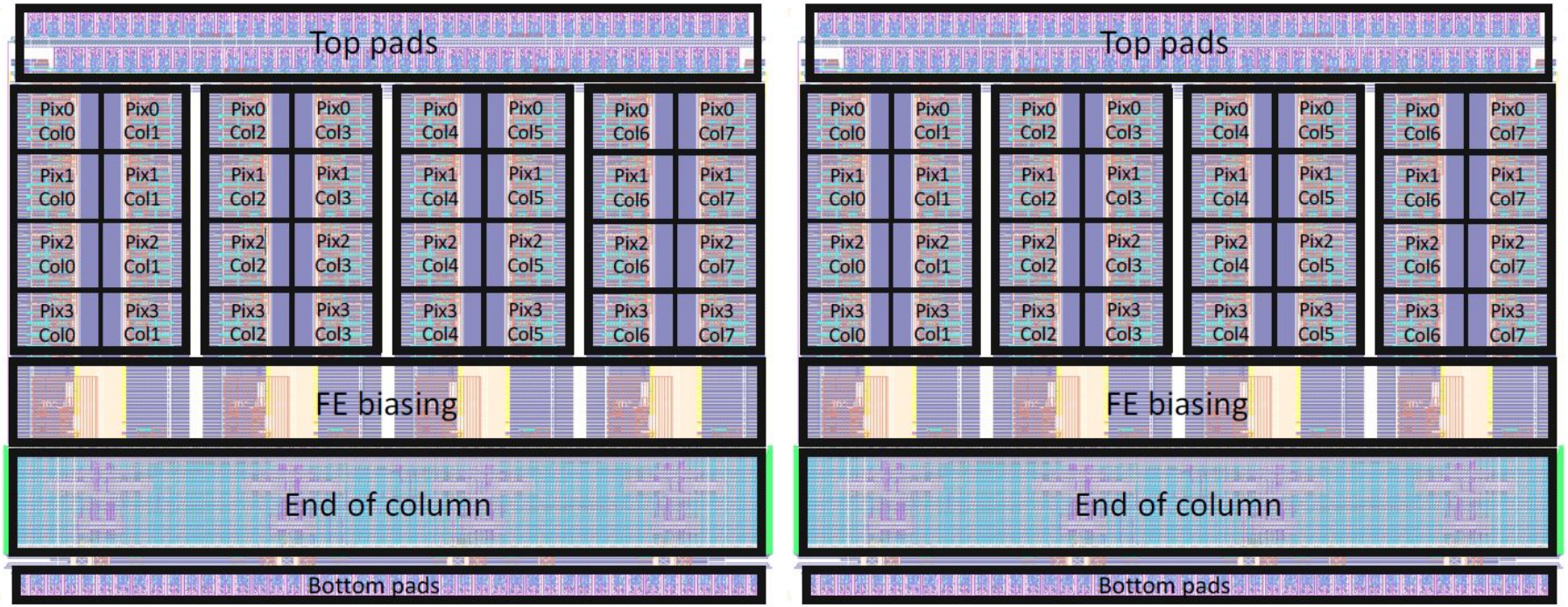
BOTTOM (64)

- 8 DVDD
- 8 DGND
- 8 DVSS
- 4 DVDD_IO
- 4 DGND_IO
- 16 Tx outputs
- 2 clk, 2 reset, 2 test-pulse
- 8 SPI
- 2 clk_out

Y > 5 mm due to increased number of pixels per column

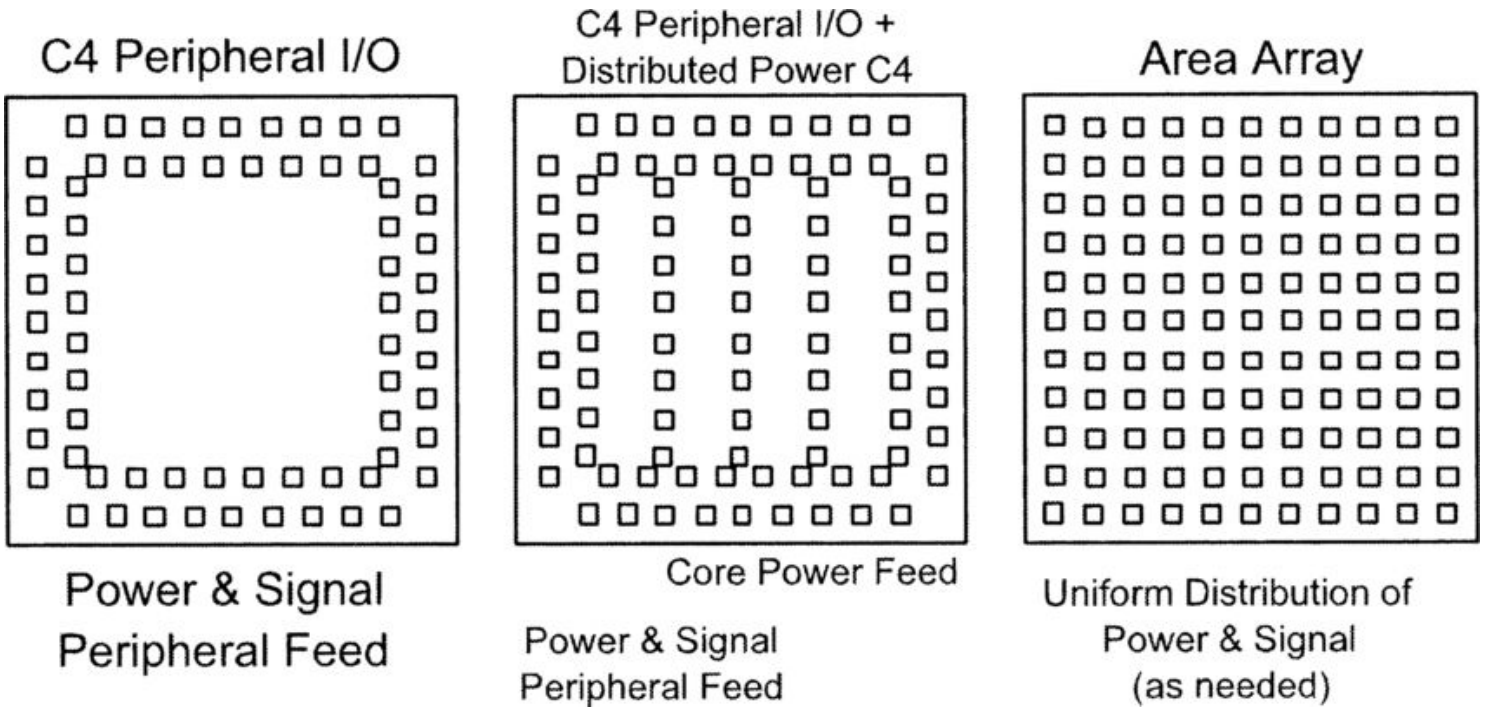
X > 5 mm due to added padframe (and higher number of input interconnections)

ALCOR-64 wire-bond version (4x16 matrix)



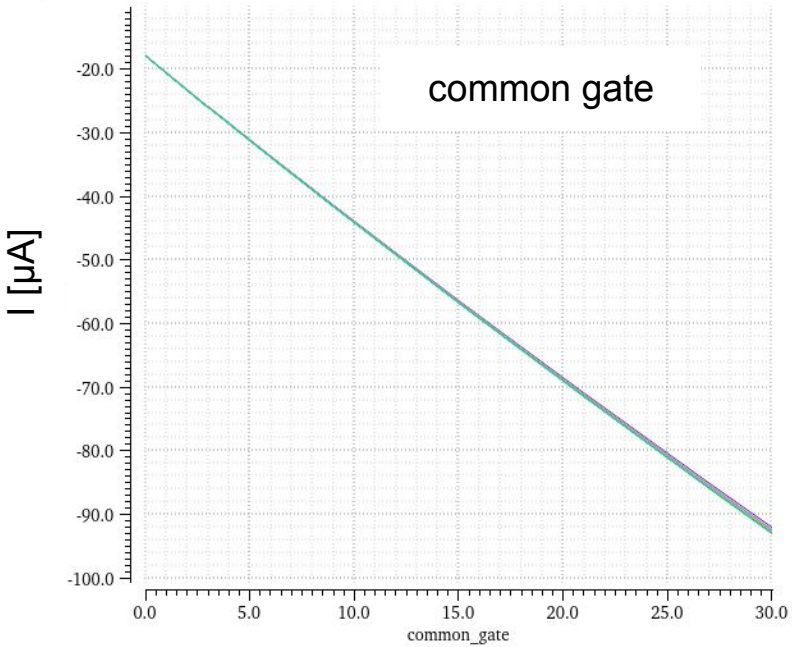
X ~ 10 mm *vs* Y < 4 mm

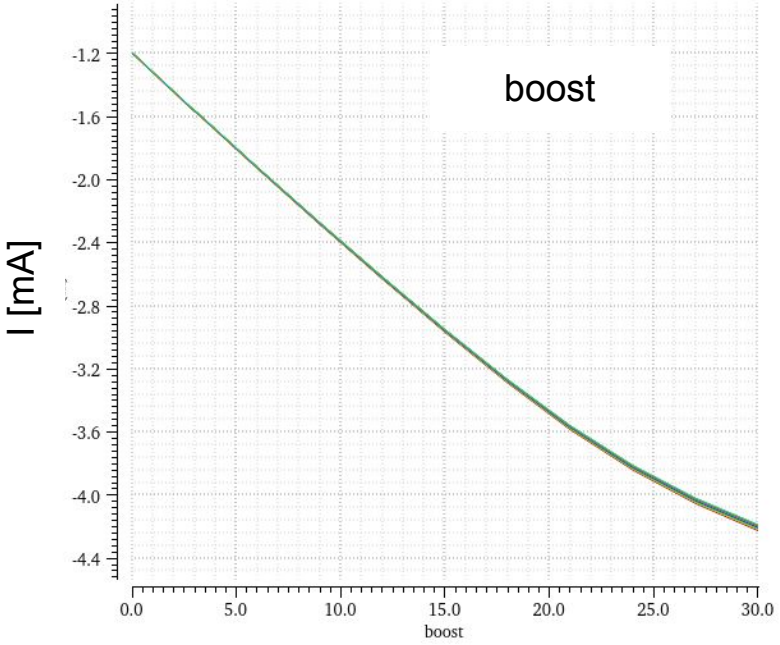
Flip-chip BGA packaging



ALCOR v1 jitter simulations

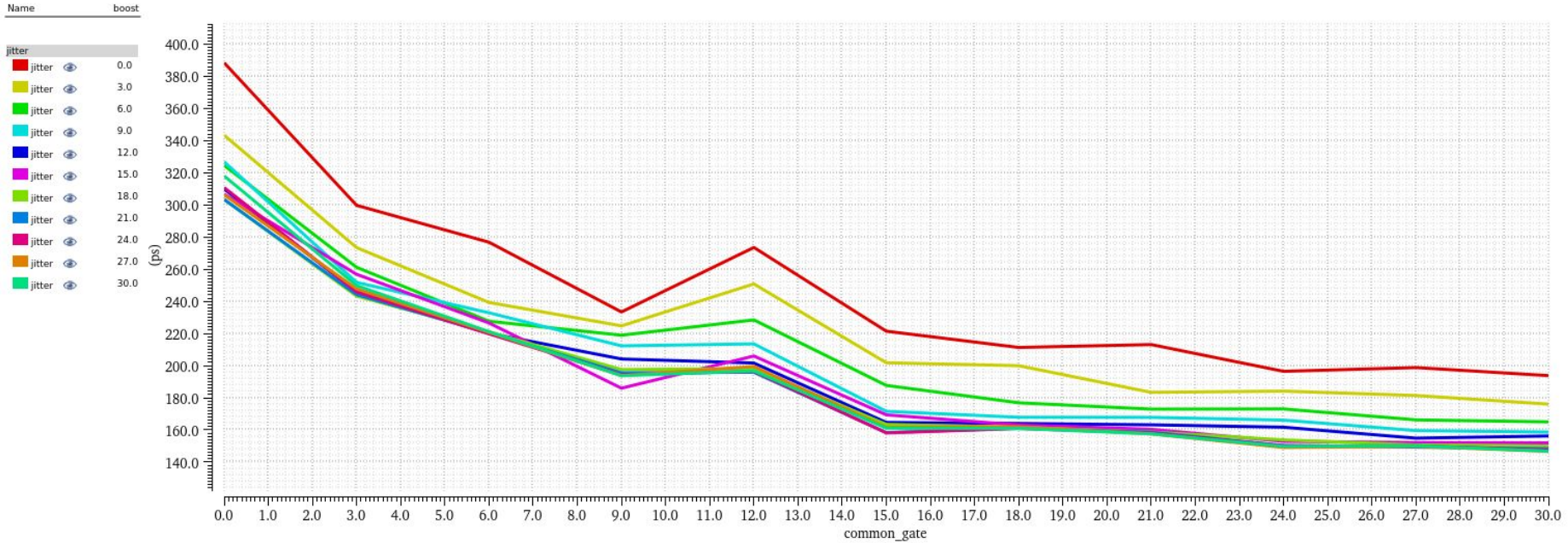
Common gate and Boost bias scan



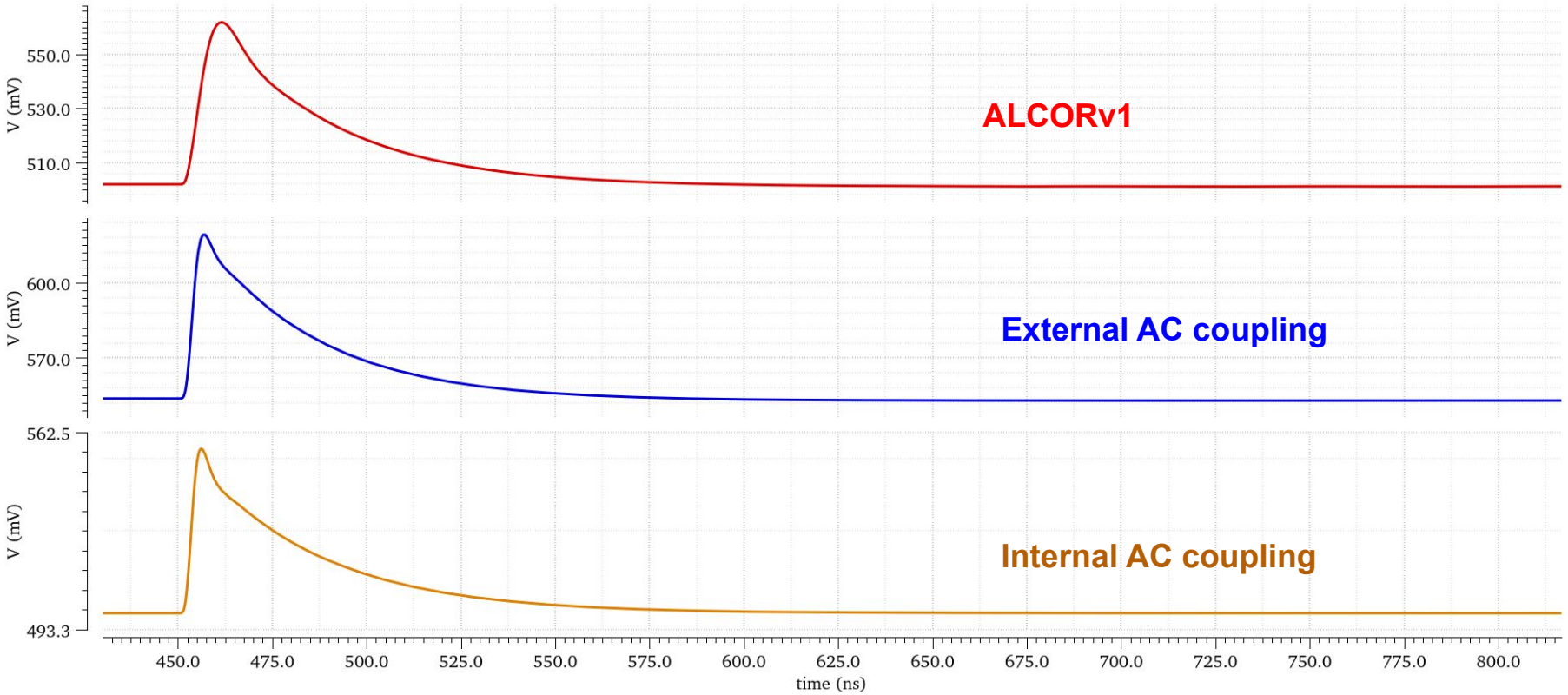


ALCOR v1 jitter simulations

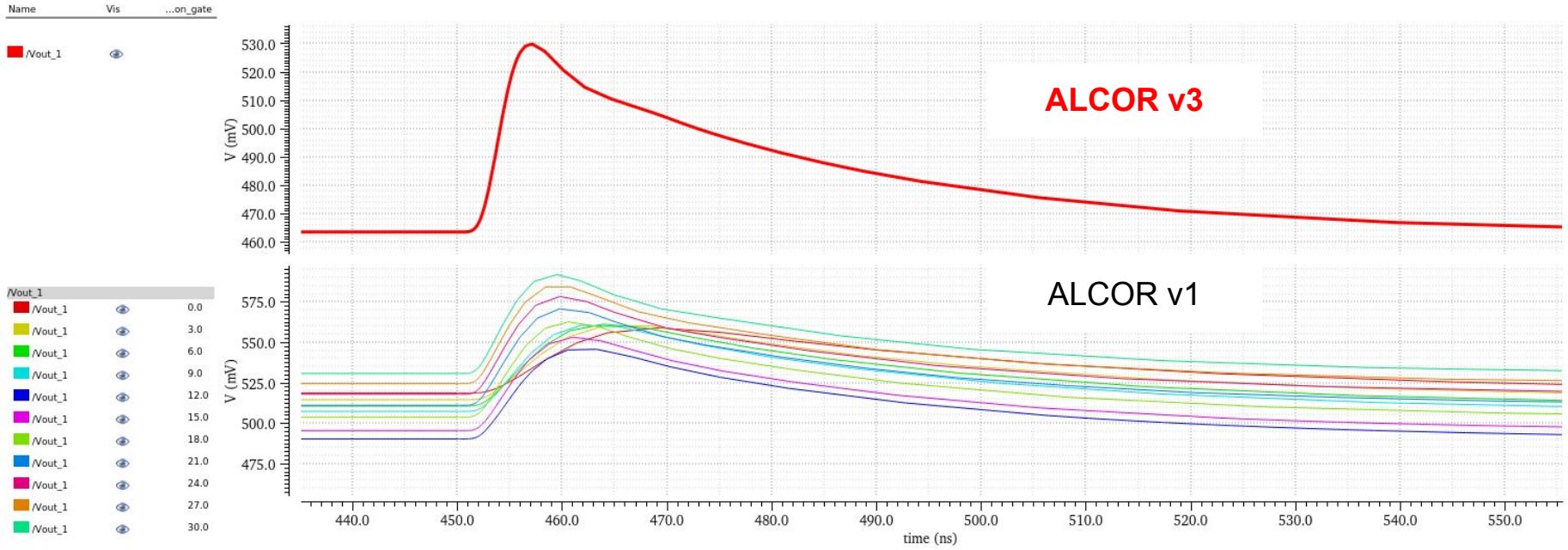
Common gate and Boost scan



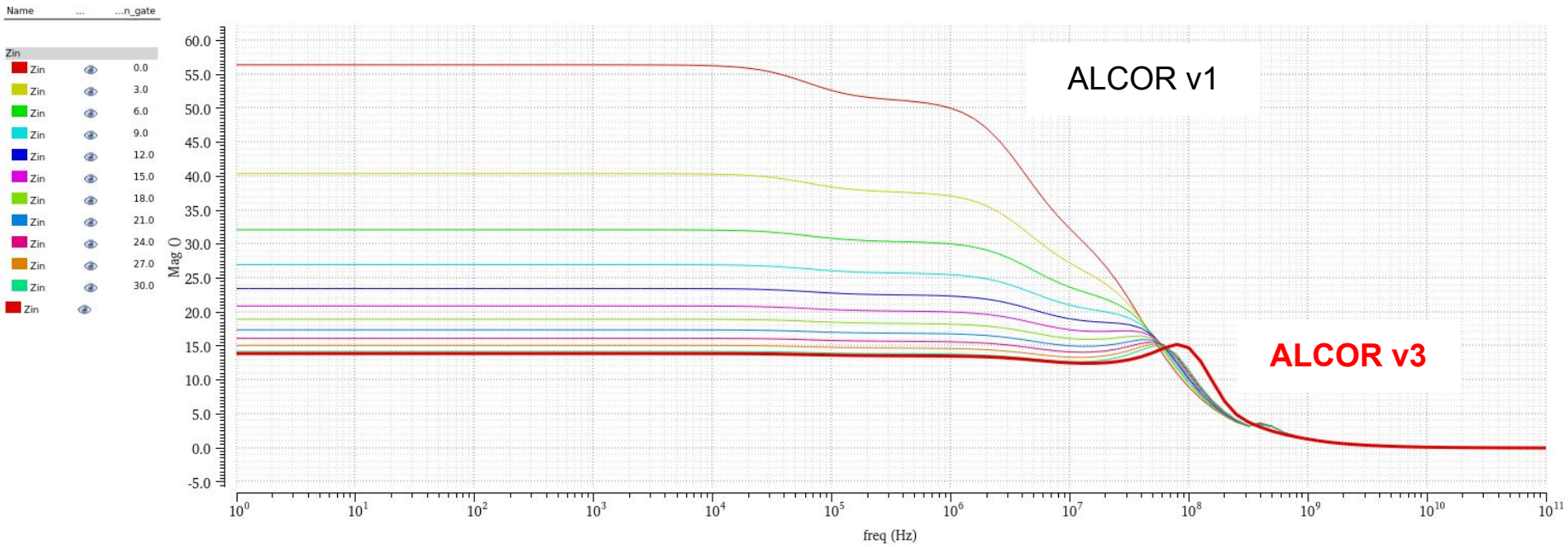
Time response



Time response



Zin


Name ... ...n_gate
Zin
Zin 0.0
Zin 3.0
Zin 6.0
Zin 9.0
Zin 12.0
Zin 15.0
Zin 18.0
Zin 21.0
Zin 24.0
Zin 27.0
Zin 30.0
Zin
60.0
55.0
50.0
45.0
40.0
35.0
30.0
25.0
20.0
15.0
10.0
5.0
0.0
-5.0
Mag ()
10^0 10^1 10^2 10^3 10^4 10^5 10^6 10^7 10^8 10^9 10^{10} 10^{11}
freq (Hz)
ALCOR v1
ALCOR v3

Frequency response