BENDING, TESTING, CHARACTERIZATION: ACTIVITIES IN PADOVA AND TRIESTE FOR THE ePIC TRACKER

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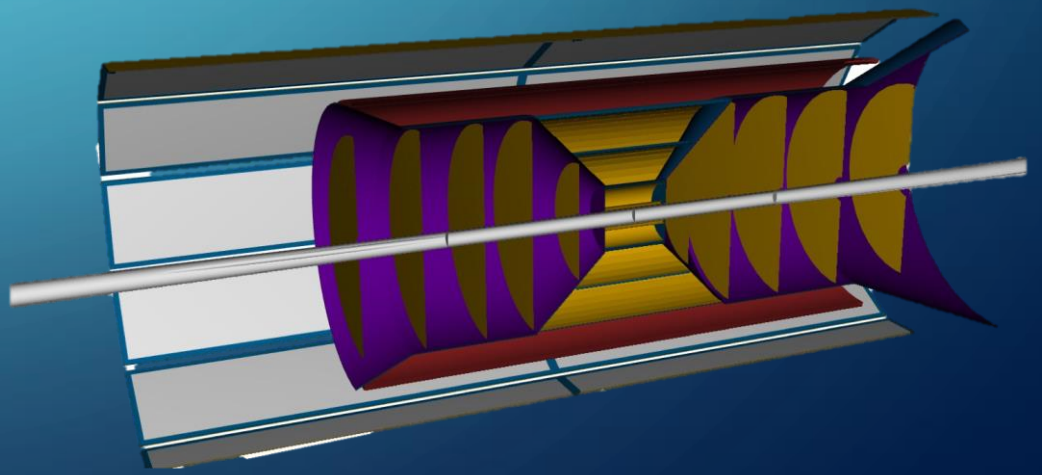


For the slides about the activity in Trieste: thanks to G. Contin and M. Verdoglia!

EIC_NET TEAMS

- Padova
  - Staff: P. Giubilato, S. Mattiazzo, G. Meng, A. Rossi, R. Turrisi
  - PhD/PostDoc: C. Bonini + phd to be hired in next call, co-funded by DoE
  - Activity on chips: test and characterization of bent/flat APTS SF, next step under discussion
- Trieste
  - Staff: A. Bressan, G. Contin, S. Dalla Torre, S. Levorato, A. Martin, F. Tessarotto
  - PhD/PostDoc: D. S. Bhattacharya, C. Chatterjee, R. Rai + post-doc to bi hired co-funded by DoE
  - Activity on chips: bending, test and characterization of flat and bent DPTS, preparation of bent APTS SF samples

NB: these are the names who have % of FTE in EIC, the work has also to be credited to local ALICE ITS3 people!

SHORT RECAP 1

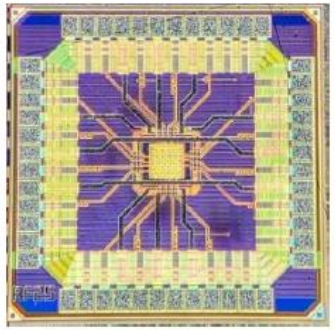
- "Next thing" for physics performance needed
  - Granularity, coverage, resolution → small pixels, large fraction of sensitive area, low material budget, high S/N and efficiency...and reach a lower radius, and cost Is also a parameter!
- Development of sensor/electronics for ITS3 upgrade, big leap from ITS2/ALPIDE chip
- There are three main fields the ITS3 project relies on and develops/pioneers

1. Large area (wafer-scale) Monolithic Active Pixel Sensors
   - use of single stitched sensors (up to ~28×9 cm^2 in size cut from a 300 mm wafer)
   - no tiling of modules by chips
   - no support circuit board
2. **Bending** of Monolithic Active Pixel Sensors
   - truly cylindrical "barrel" geometry (radius of innermost layer: 18 mm)
   - very close to beam pipe, low material budget
3. Monolitic Active Pixel Sensors in **65 nm technology** node
   - larger wafers, possibly thinner sensors (<50 µm), possibly a total material budget per layer < 0.05% X/X_0
   - higher integration density
   - low power consumption (<40 mW/cm^2) that can be achieved with MAPS makes air cooling sufficient to operate the detector.

SHORT RECAP 2 – TEST STRUCTURES PRODUCTION

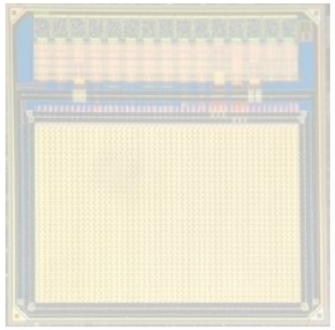
- Few modifications tested on ALPIDE (180 nm TowerJazz technology), then go for 65 nm technology at the now TPSCo
- Multi-Layer-perReticle (MLR)1: production of prototype circuits, complete functional blocks, prototypes of pixel arrays to develop know-how about the technology
  - Analog Pixel Test Structure: 4×4 arrays of pixels, pitches between 10 and 25 µm with direct full analogue readout → test also analog front-end
  - Digital Pixel Test Structure: 32 × 32 pixels,15 µm pitch with in-pixel fast discrimination, encoding of Time Over Threshold and data-driven asynchronous binary readout
  - CircuiteExploratoire65(nm) chips: 32 × 32 pixels, 15 µm pitch with three variants of front-ends and analog readout

Exploratory chips: APTS, CE65 and DPTS



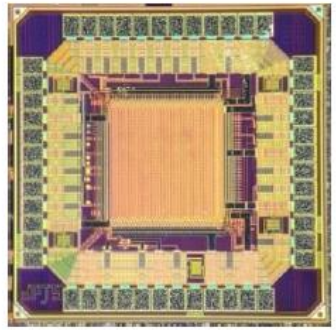
APTS
(Analogue Pixel Test Structure)

- Matrix: 6×6 pixels
- Pitch: 10, 15, 20, 25 µm
- Direct analogue readout of central 4×4 submatrix
- Two types of output drivers:
  - Source follower (APTS-SF)
  - Very fast OpAmp (APTS-OA)
- AC/DC coupling
- 3 process modifications



CE65
(Circuit Exploratoire 65 nm)

- Matrix: 64×32 or 48×32
- Pitch: 15 µm or 25 µm
- Rolling shutter readout (down to 50 µs integration time)
- 3 in-pixel architectures:
  - AC-coupled amplifier
  - DC-coupled amplifier
  - Source follower
- 4 chip variants:
  - Standard process 15 µm pitch
  - Modified process 15 µm pitch
  - Modified process with gap 15 µm pitch
  - Standard process 25 µm pitch



DPTS
(Digital Pixel Test Structure)

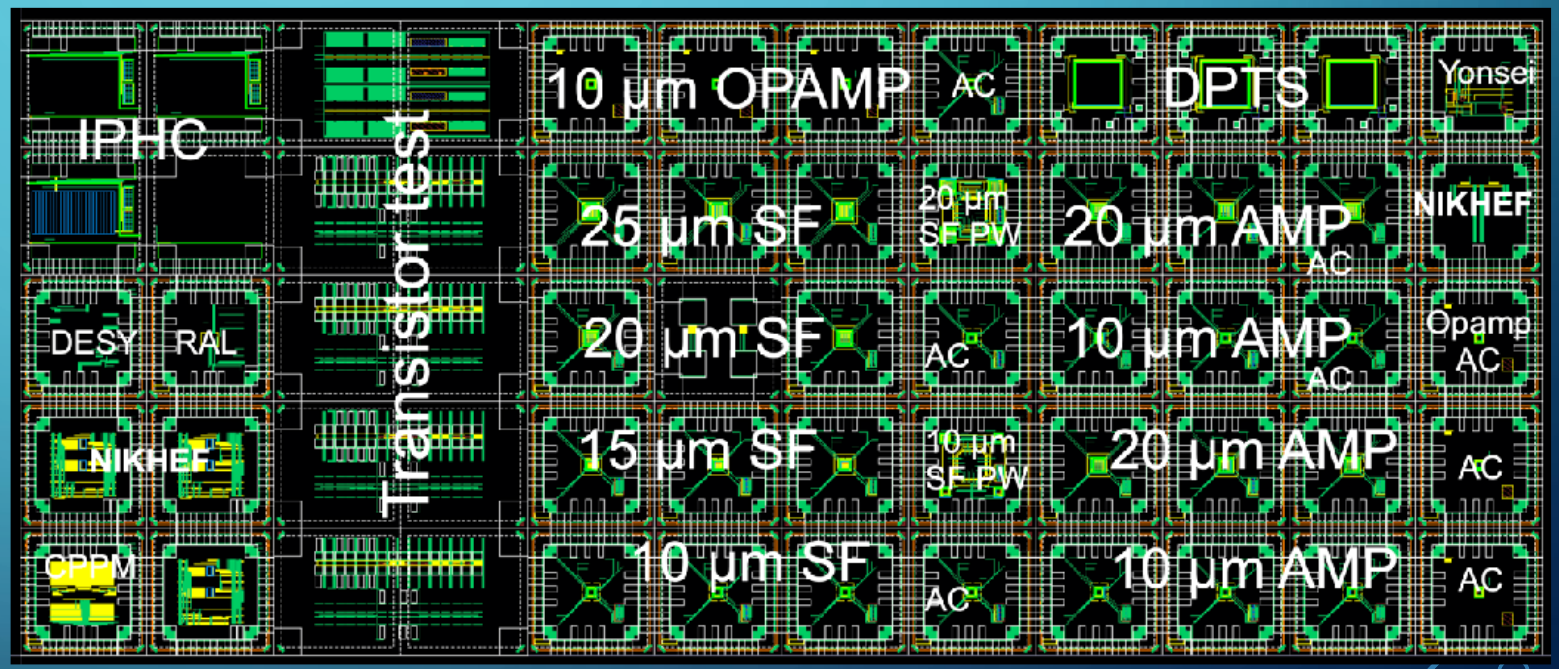
- Matrix: 32×32 pixels
- Pitch: 15 µm
- Asynchronous digital readout
- Time-over-Threshold information
- Only “modified with gap” process modification

S. Senyukov, ALICE Upgrade Week 2023

FIRST SUBMISSION IN TOWERJAZZ 65NM

- Contained several test chips
  - radiation test structures
  - pixel test structures
  - pixel matrices
  - analog building blocks

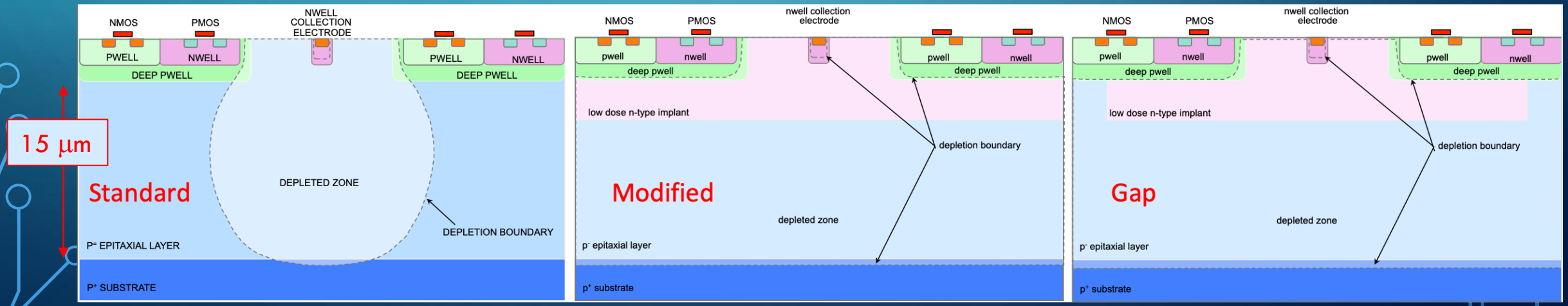
  (band gaps, LVDS drivers, etc)



CMOS VERSIONS

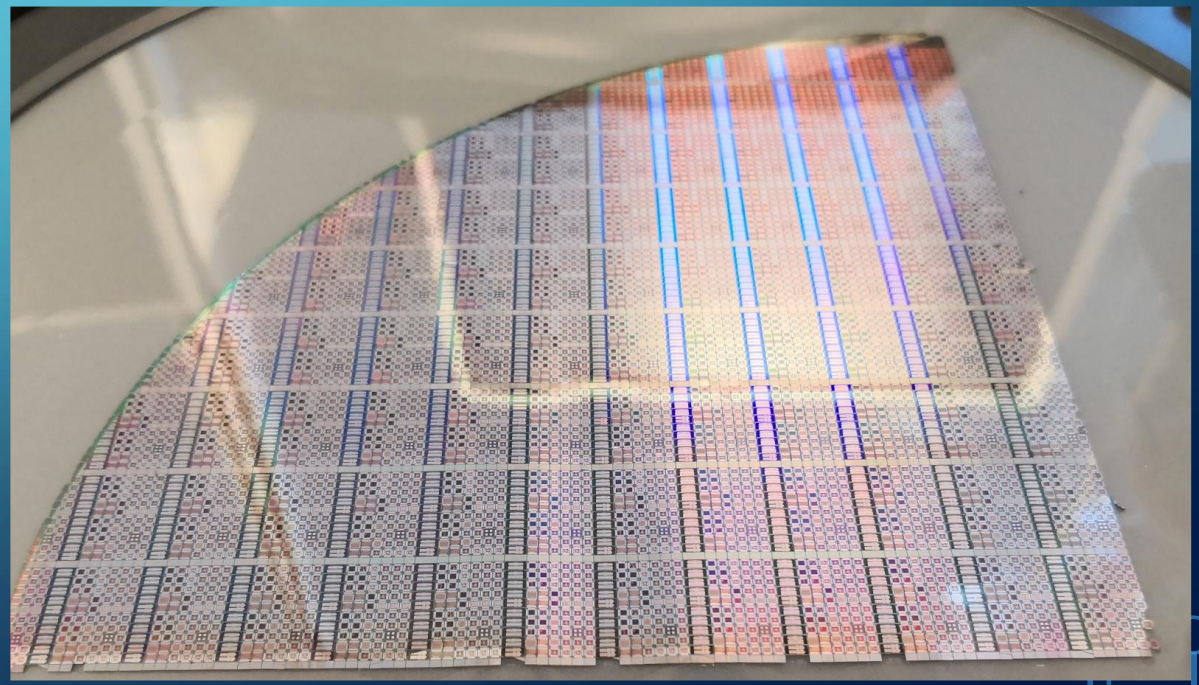
- Split 1: Standard process without modifications
- Split 2: First modification of the deep pwell to improve isolation between circuitry and sensor and prevent punch-through between deep nwell and circuitry
- Split 3: Adding to split 2 the deep nwell adjustment in the pixel to allow full depletion
- Split 4: Adding to split 3 an additional deep pwell modification to prevent potential wells created by the additional in-pixel circuitry

These four *splits* have been produced with the three ''variations'' below (where appropriate):



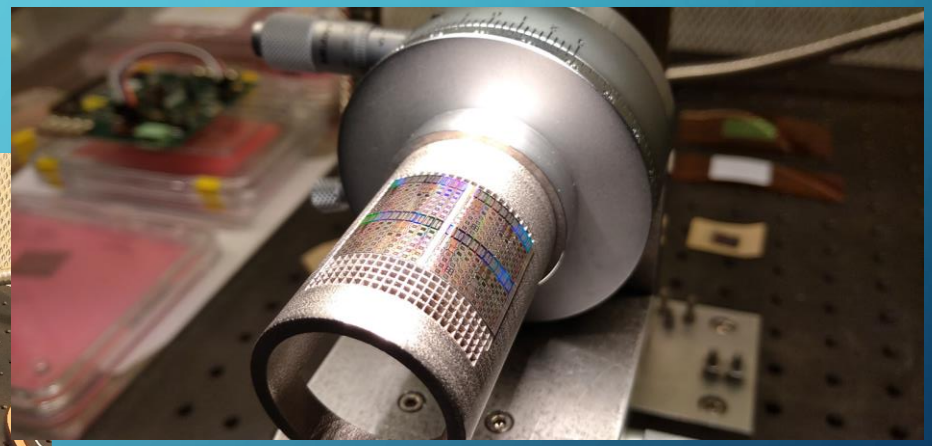
FLAVORS OF CHIPS PRODUCED

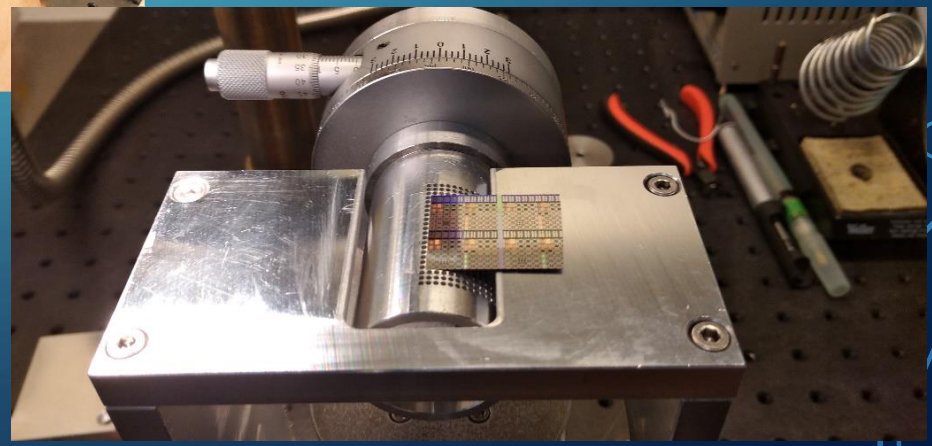
- APTS: analog pixel test structures, source follower based (AC and DC coupled) and with special in-pixel amplifier
- DPTS: digital pixel test structures, source follower based
- OPAMP: analog pixel test structures, op-amp based
- Pixel pitches: 10,15,20,25 microns



BENDING IN TRIESTE

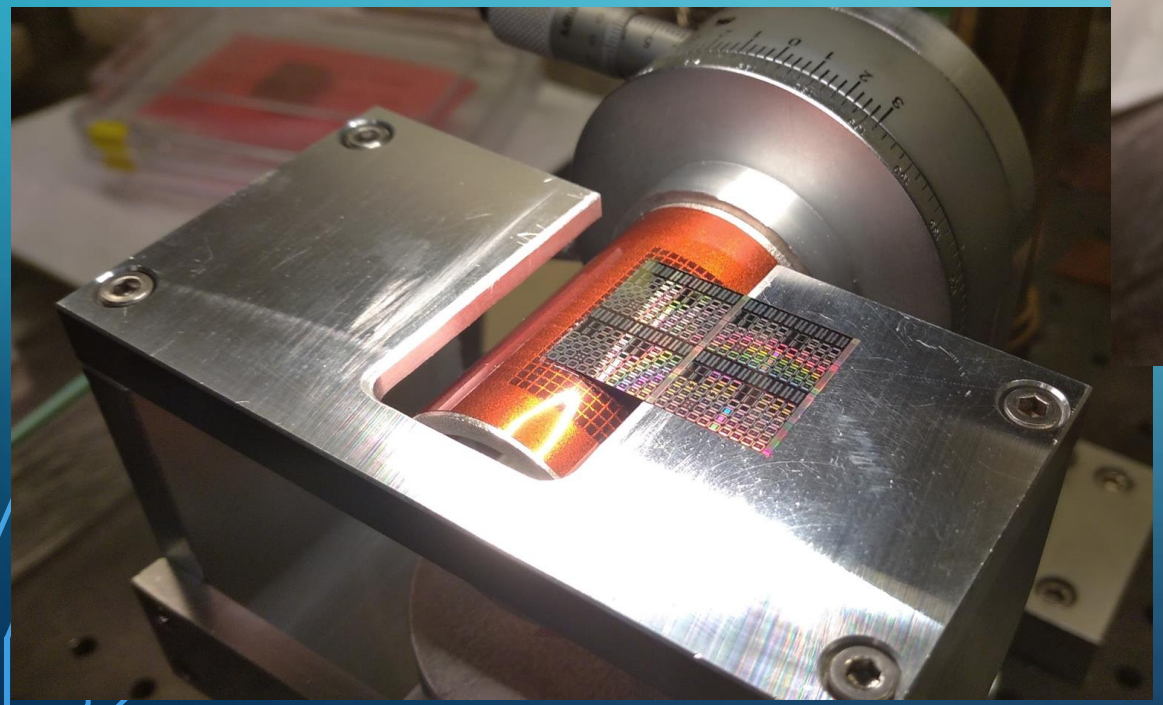
- Manual bending done manually, fixing one end with tape
- "Vacuum" technique to be implemented
- Bending executed with chip oriented in both directions (i.e. columns parallel or orthogonal to bending direction)

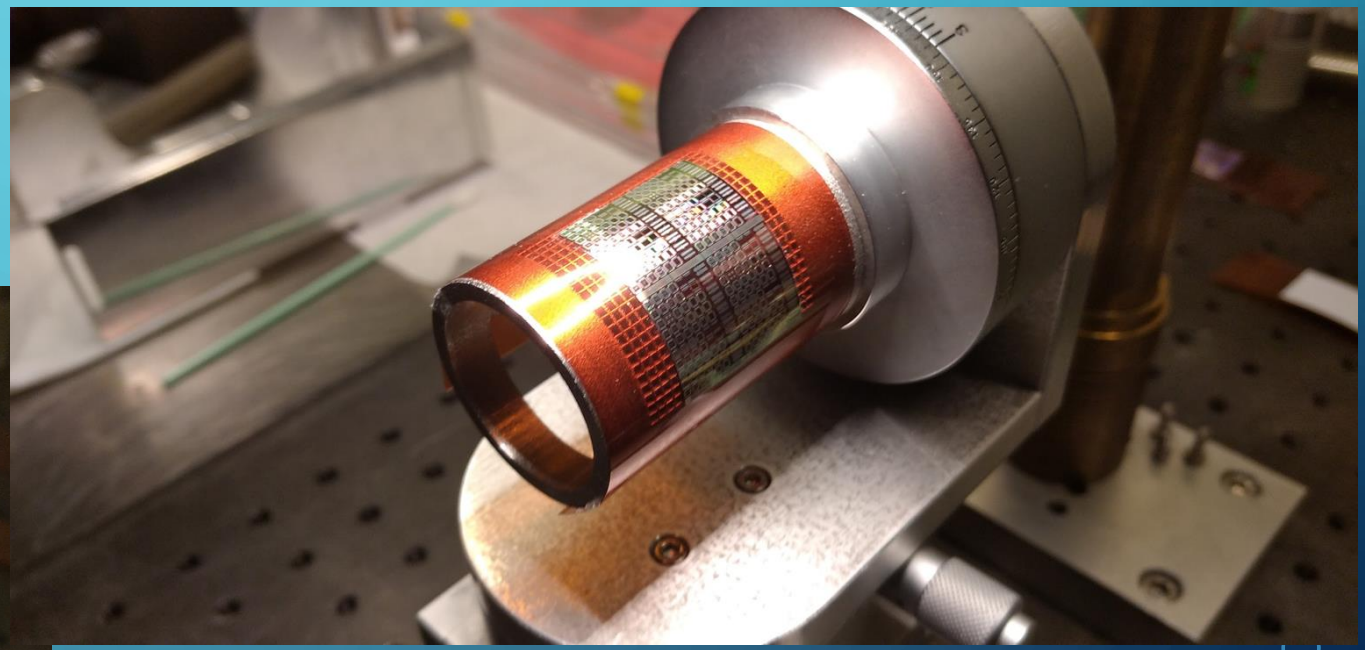




STRESS TEST WITH KAPTON SUPPORT - 1

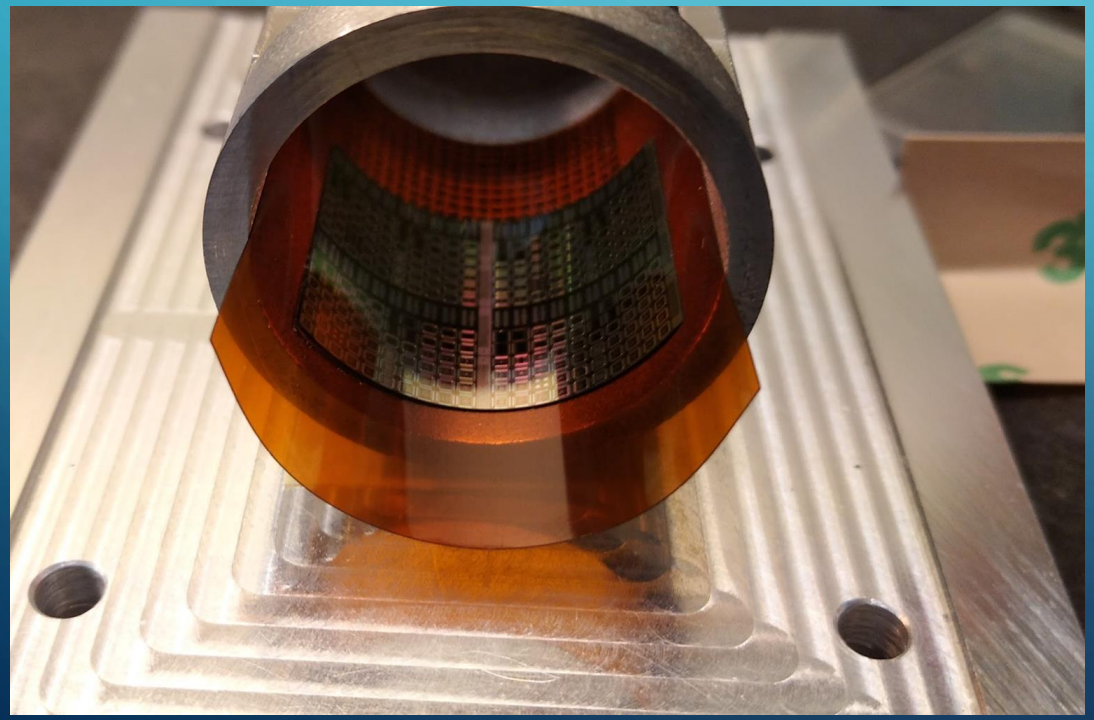
- Kapton tape used as backing to bend/reposition the chip

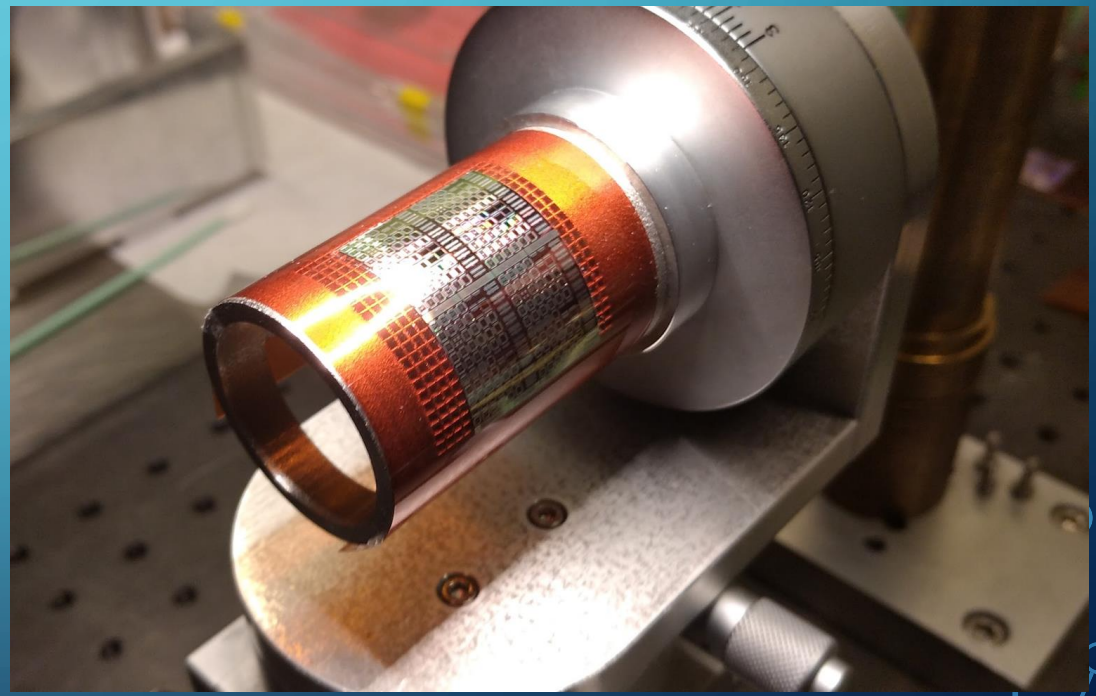




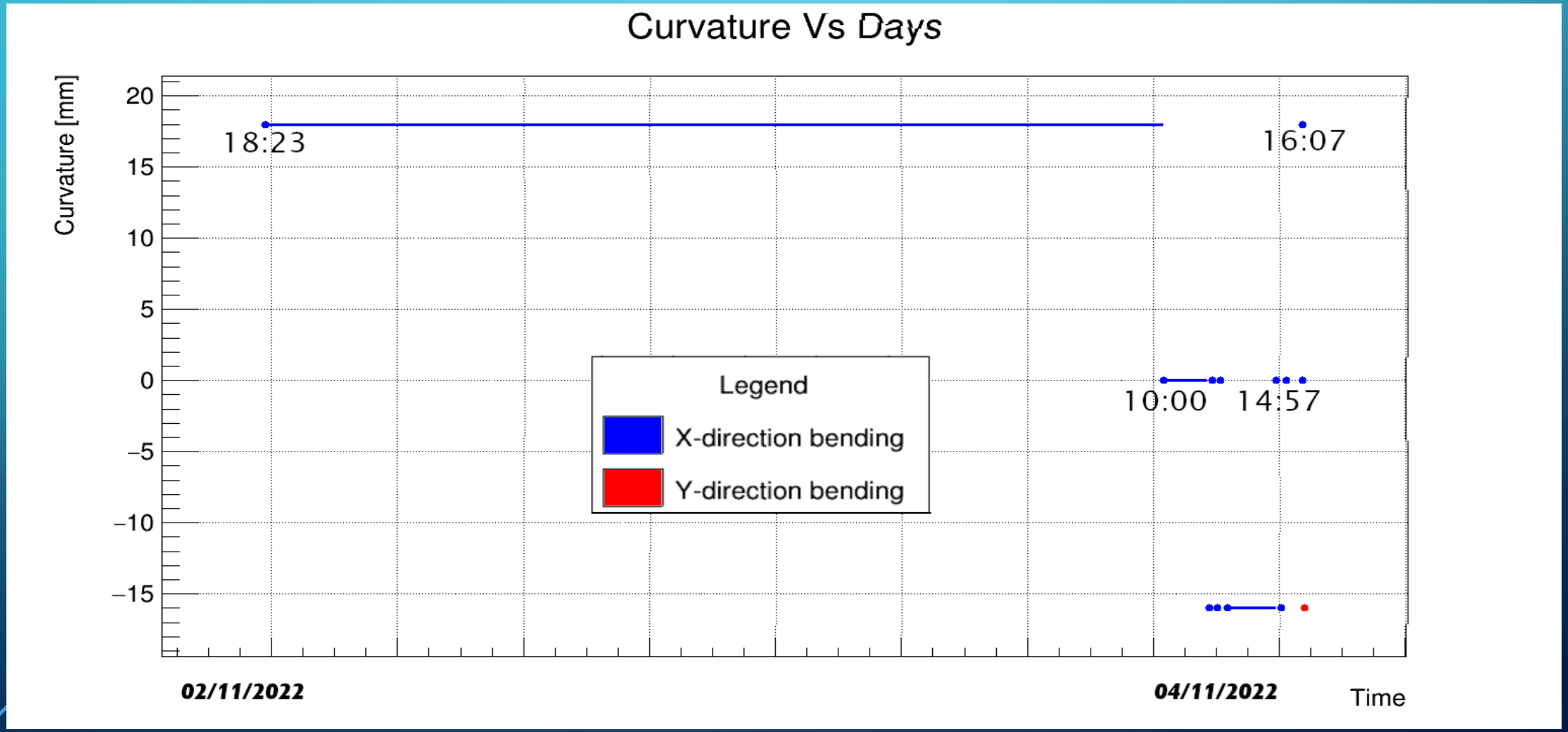
STRESS TEST WITH KAPTON SUPPORT - 2

- Many curvature tested in sequence
  - X direction: +18 mm, -16 mm, 0 mm





STRESS TEST TIME PLAN



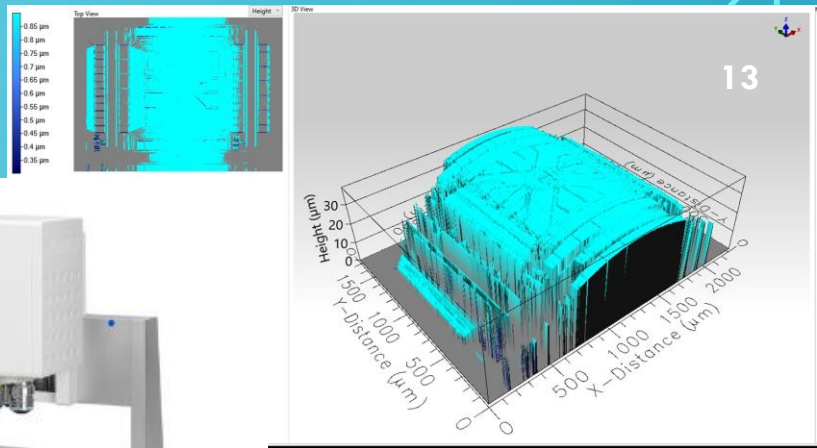
CURVATURE MEASUREMENTS

<R> = 18.1 mm

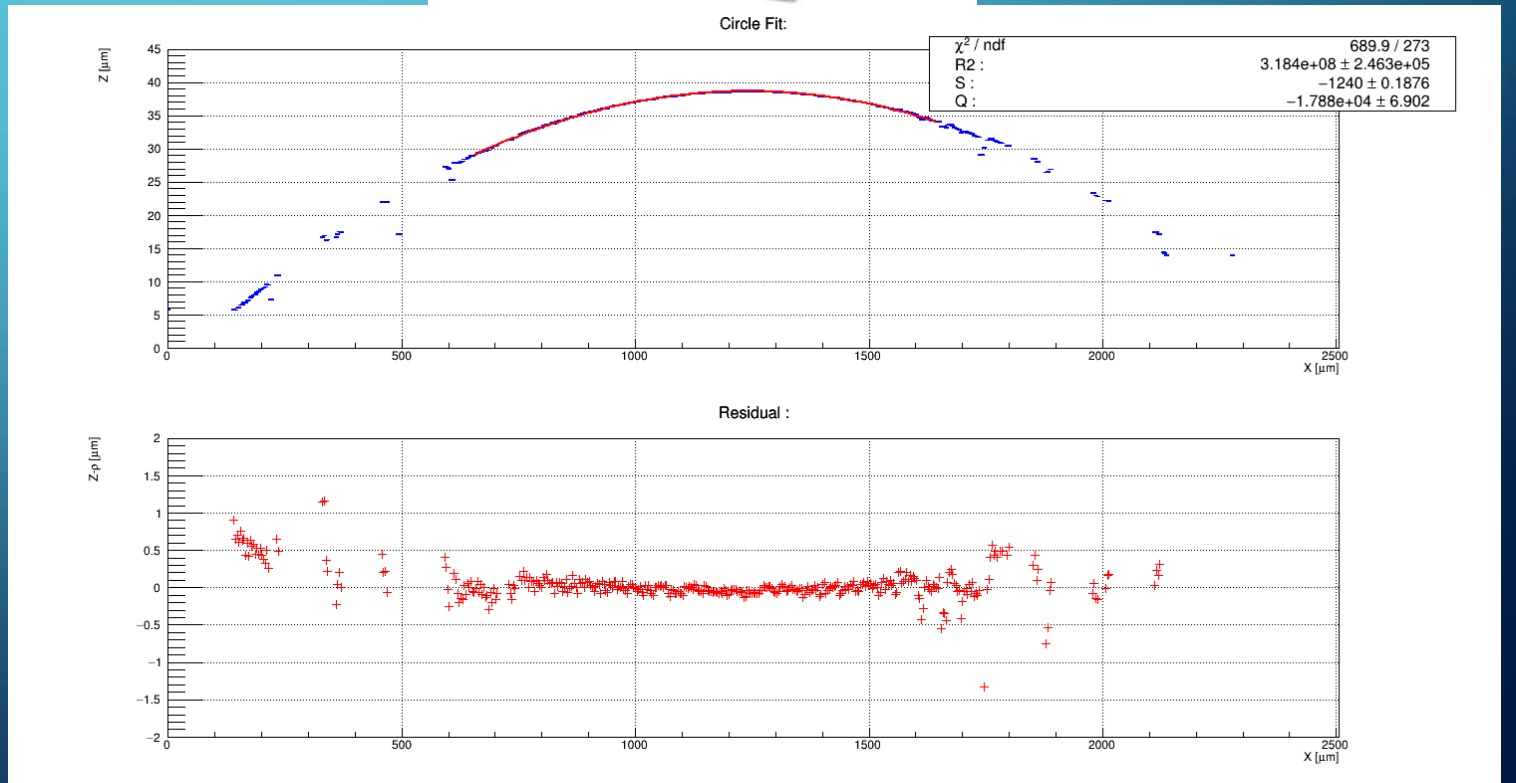
Main source of indetermination:

- fake points due to diffraction
- the scan is sensitive to superficial structures
- there is not perfect alignment between the chip and the profilometer plane

expected value R ~18.2 mm
cylinder radius ~ 18 mm
biadesive ~ 0.15 mm
chip ~ 0.05 mm

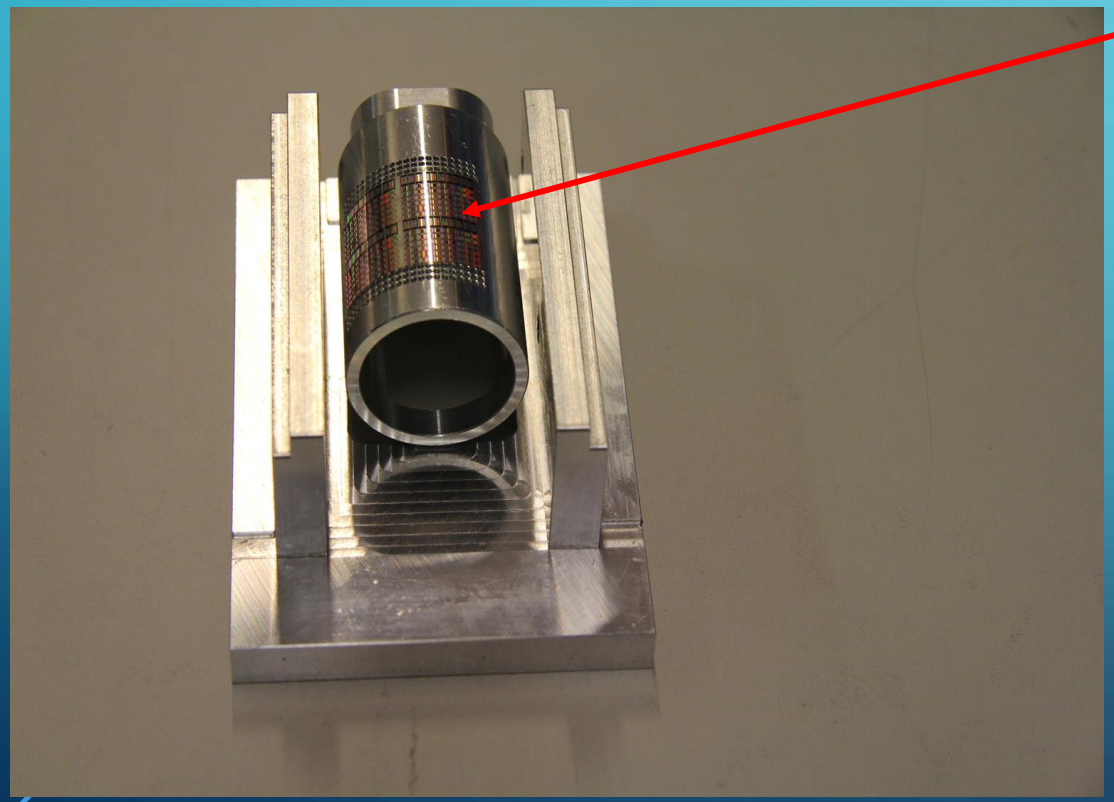


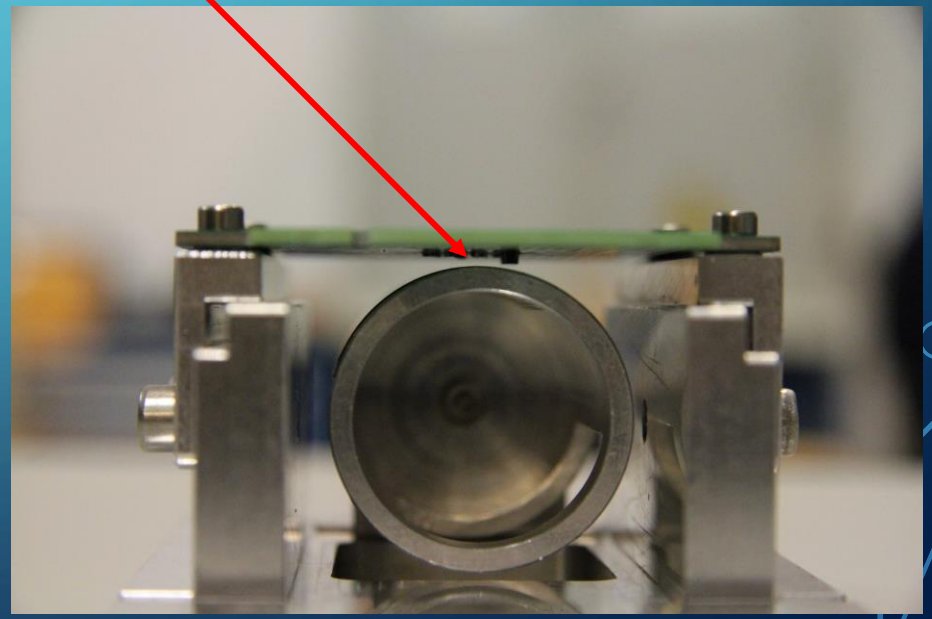
profilm3D machine



MOUNTING ON THE JIG

Hole to allow the wire bonding

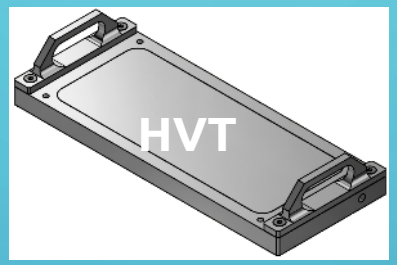


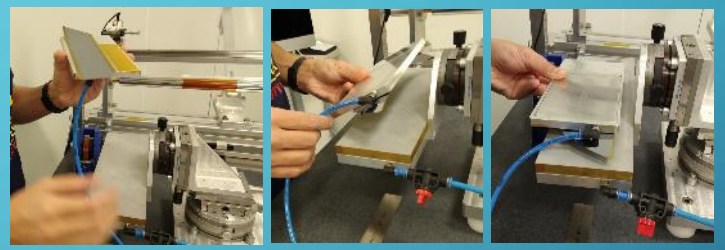


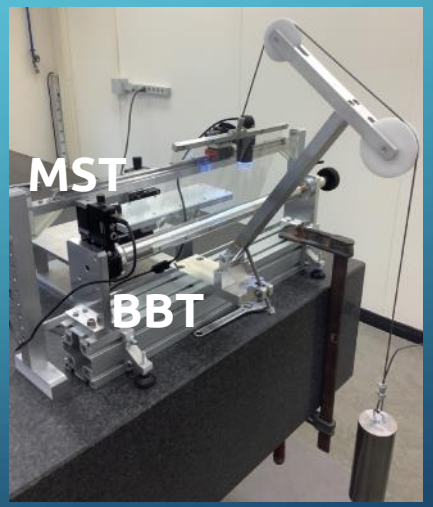
FINAL TOOLING

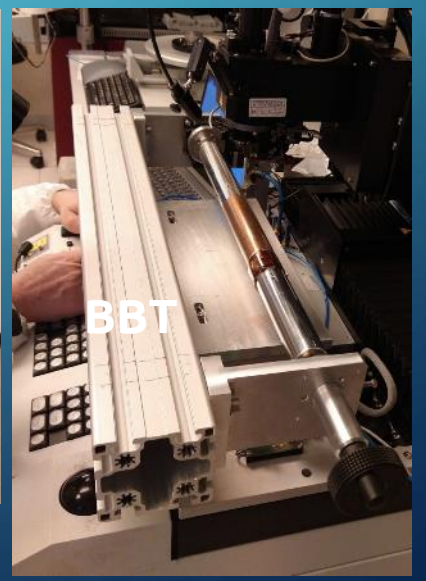
LIST OF TOOLS

1.Fixed vacuum tool (FVT)
2.Rotating vacuum tool (RVT)
3.Handling vacuum tool (HVT)
4.Microscope tool (MST)
5.Bending Bonding tool (BBT)

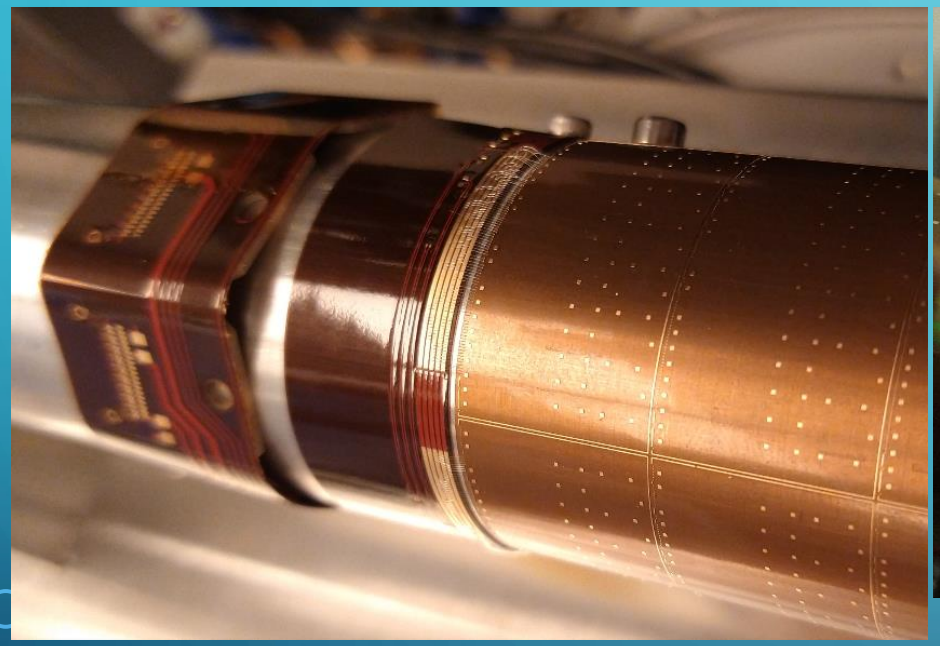


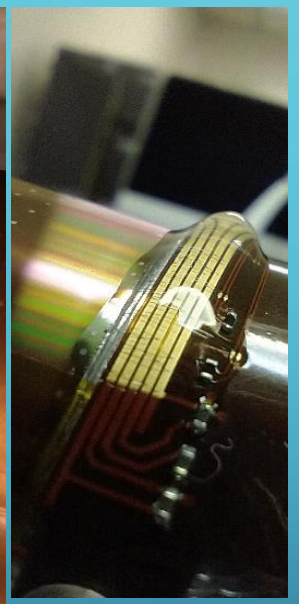


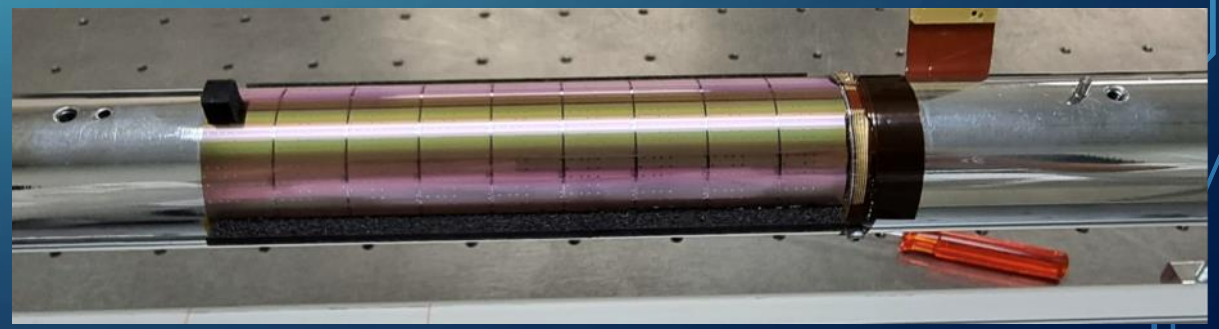




INTERCONNECTION AND GLUING

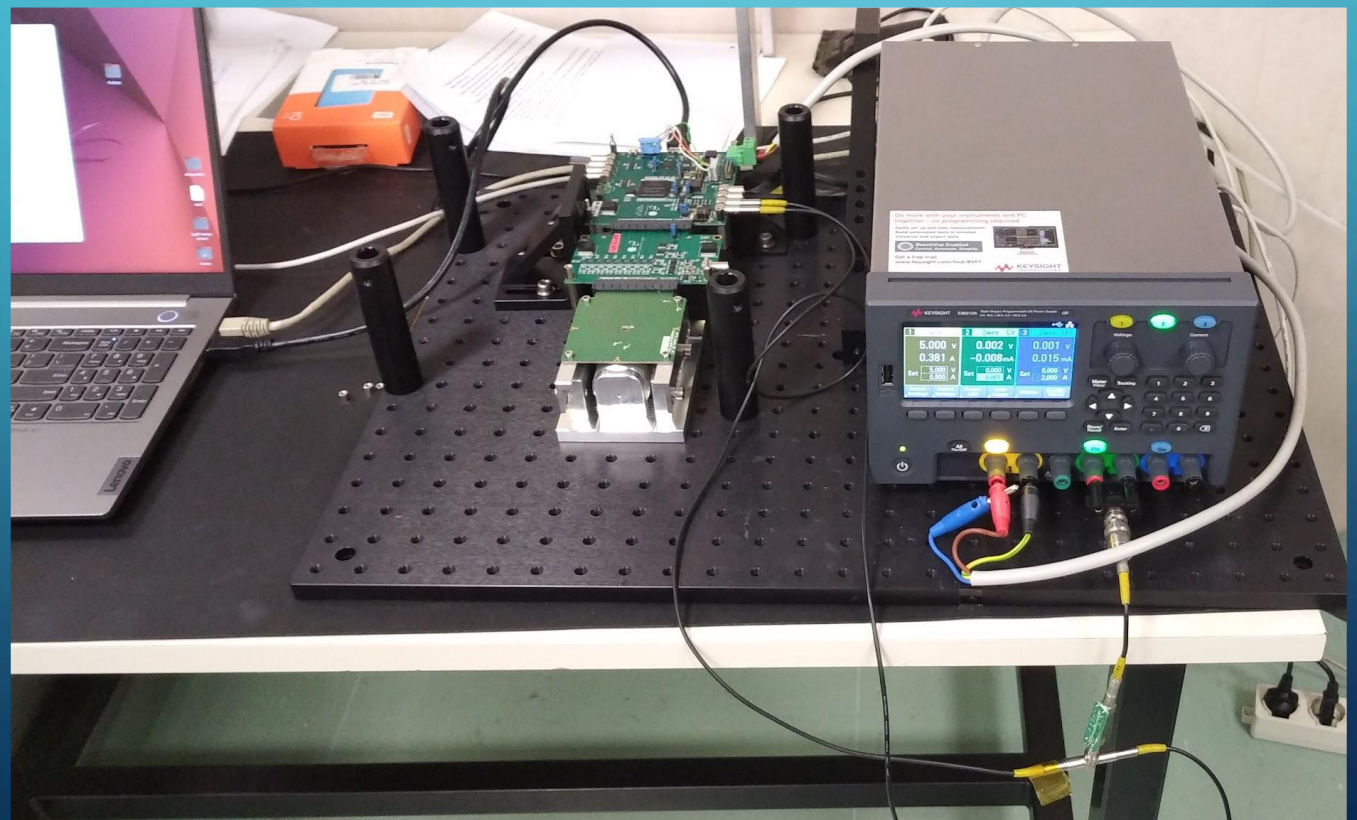






TESTING IN PADOVA

- DAQ received summer 2022, tests started fall 2022 upon test sample availability



MLR1 APTS TEST SYSTEM

DAQ board

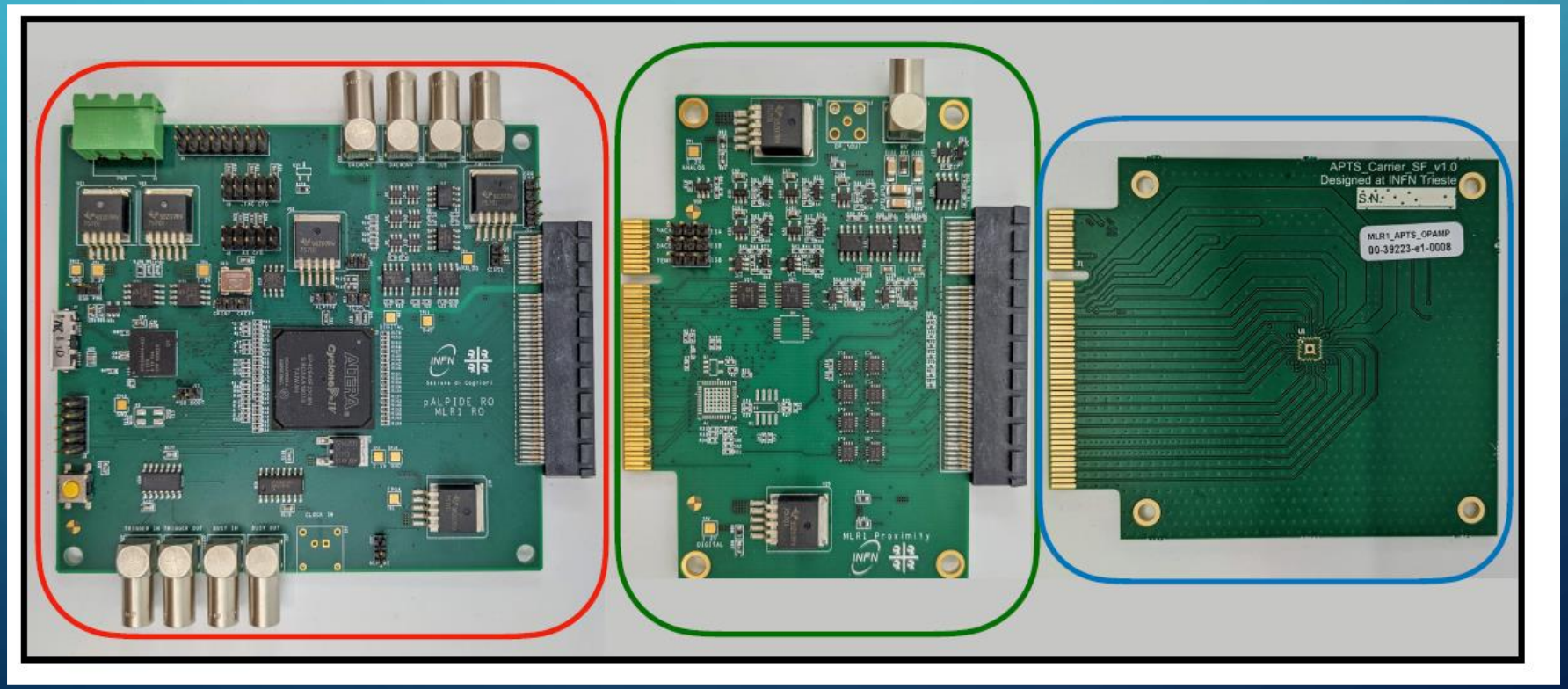
Adaptation of the previous readout system used for ITS2 and ALPIDEs

Proximity board

Designed specifically for each chip variant. Sets biases and reads analog signals

Carrier board

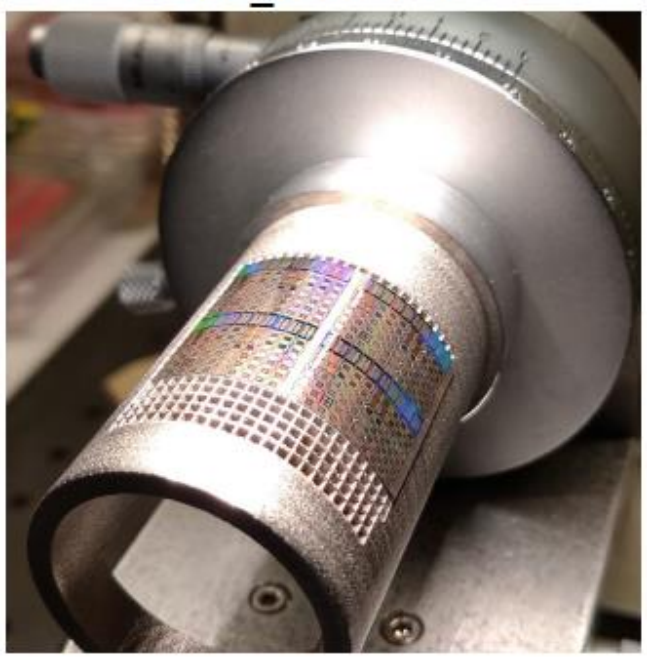
Chip carriers, designed specifically for each chip variant



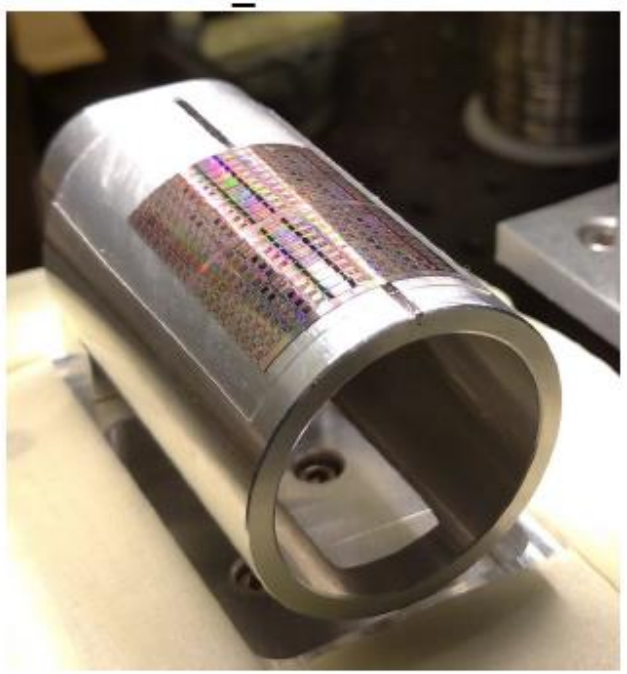
BENT CHIP TEST SAMPLES

- 3 **APTS-SF** available, bent in two different orientations, along the long edge MLR1 and along the short edge MLR1 (radius of curvature ~ 18.2 mm)

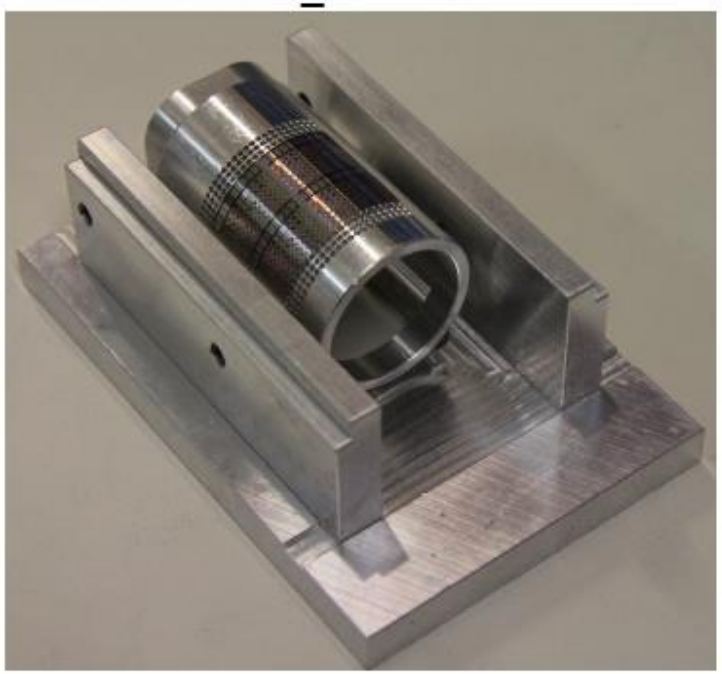
AF**15P_W16**B101



AF**15P_W16**B104

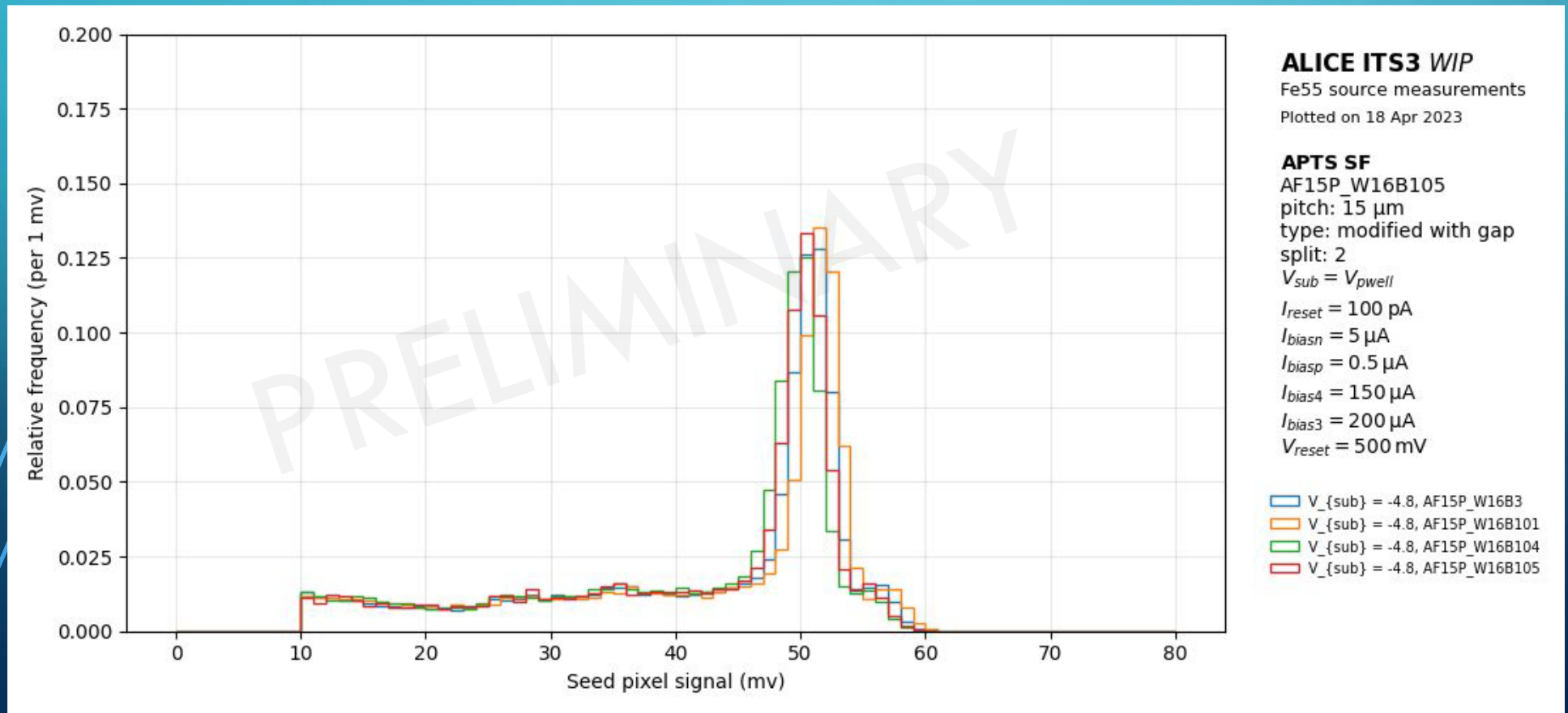


AF**15P_W16**B105



FLAT/BENT COMPARISON – ^{55}Fe SPECTRUM

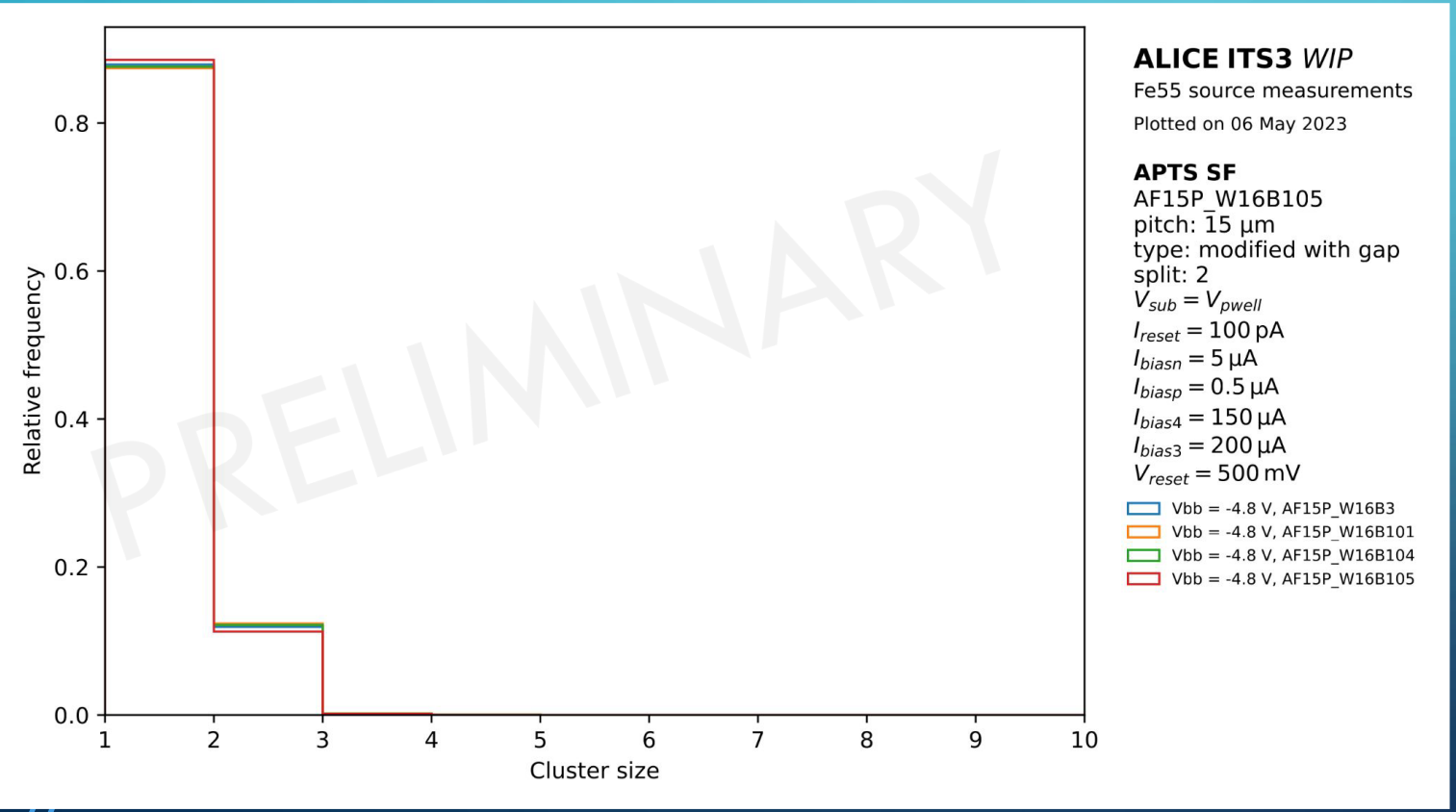
- Flat-Bent sensors comparison in [mV] @ V_{bb} = -4.8 V (bias voltage of bulk)



FLAT
LONG EDGE
SHORT EDGE
LONG EDGE

FLAT/BENT COMPARISON – CLUSTERS

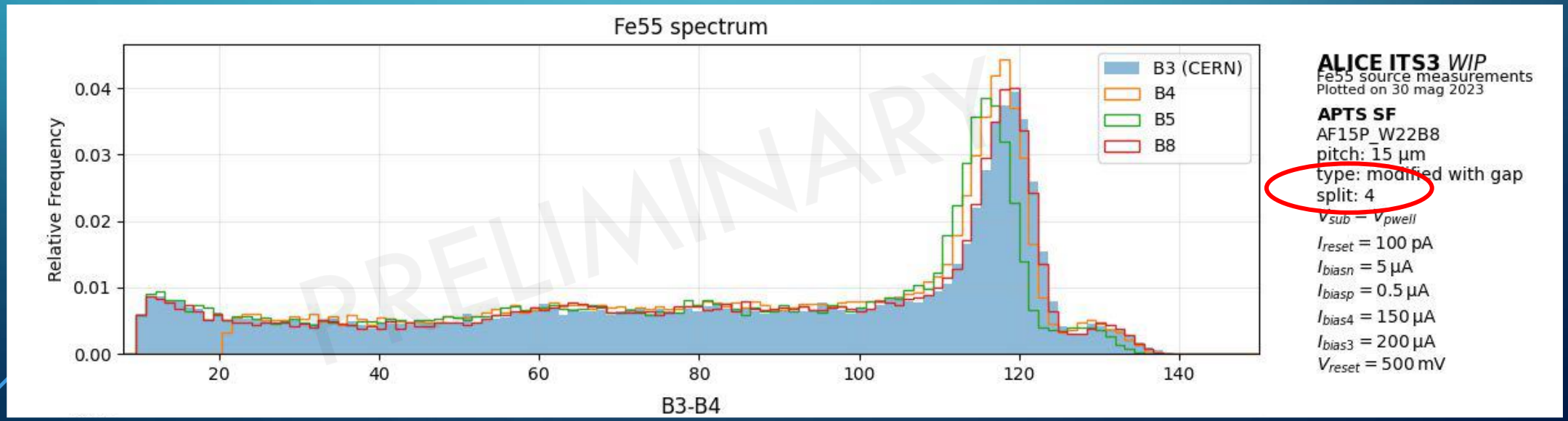
- Flat-Bent sensors comparison in [mV] @ V_{bb} = -4.8 V (bias voltage of bulk)



FLAT
LONG EDGE
SHORT EDGE
LONG EDGE

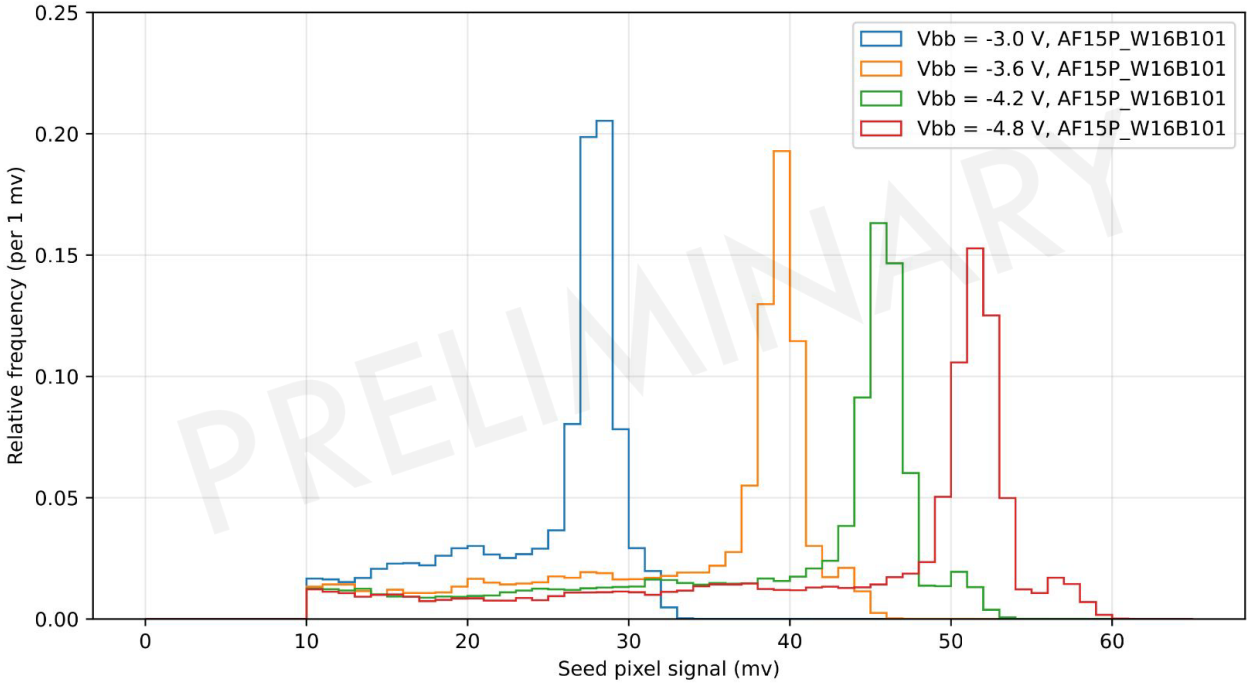
FLAT/BENT COMPARISON – CHIP-TO-CHIP VARIATION?

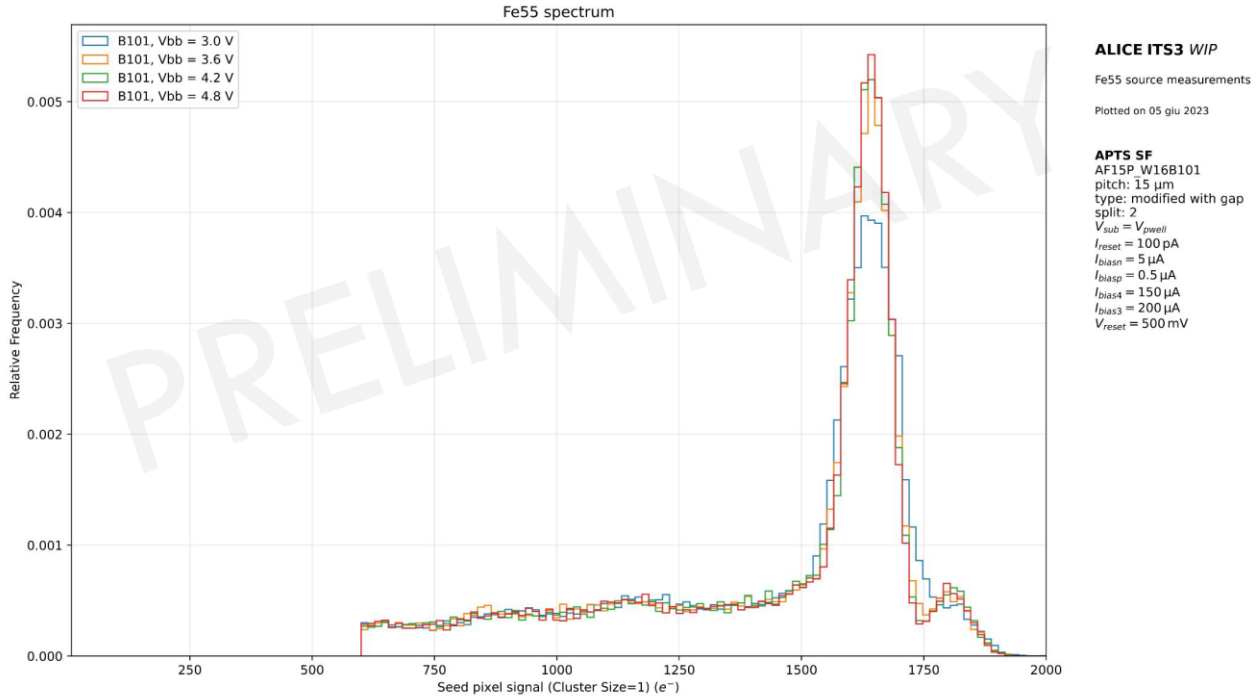
- **Flat** Chip-to-Chip variation from W22 (W16 not available)
- Trying to understand whether chip-to-chip variation is dominant over the effect of curvature
- Systematics to be obtained on the same wafer



ELECTRON-CONVERTED ^{55}Fe SPECTRUM

- Dependence on V_{bb}

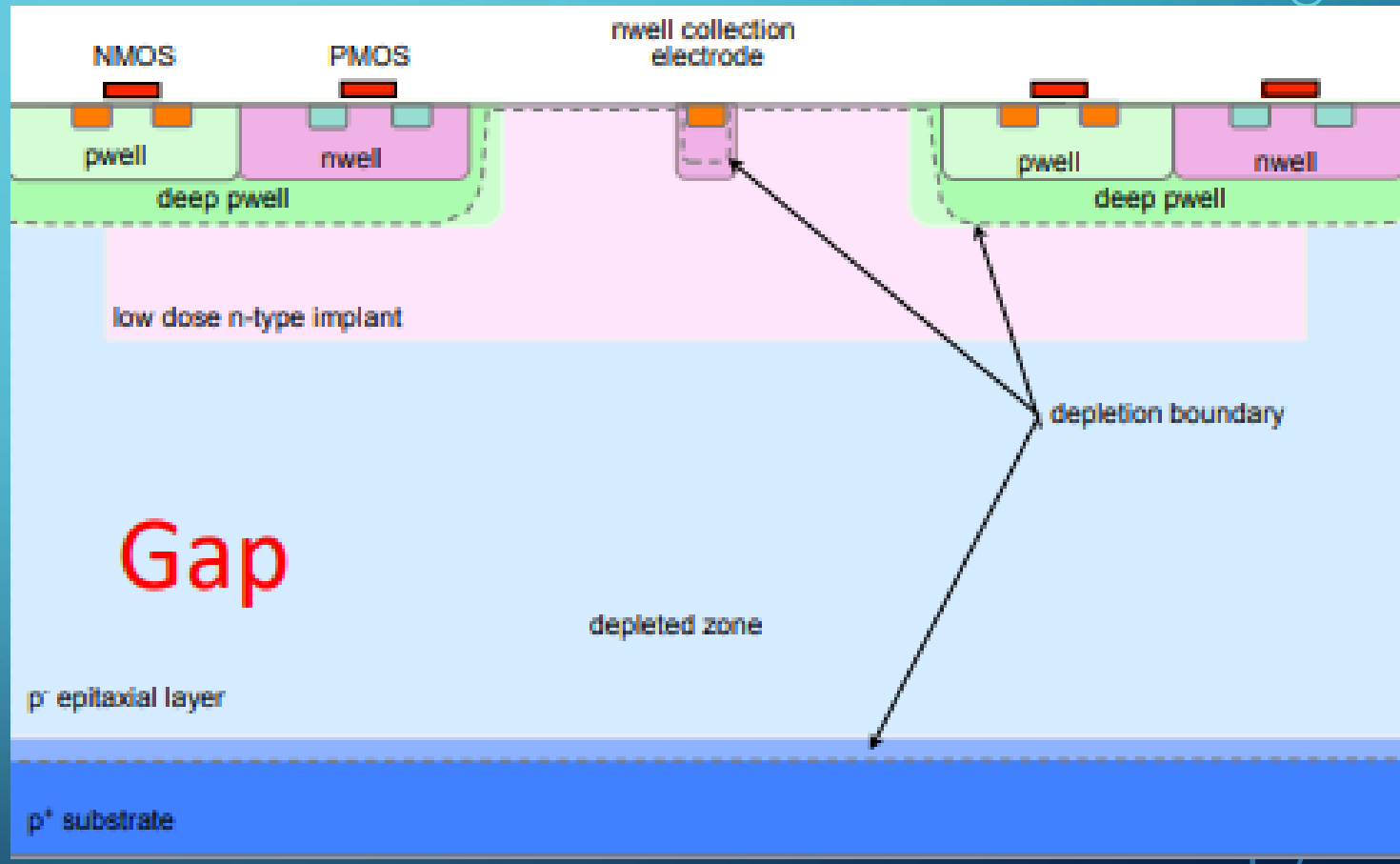




IRRADIATED CHIPS TEST – LAYOUT OF CHIPS

- AF10P_W22B57 → 10^{14} n_{eq}
- AF10P_W22B58 → 10^{15} n_{eq}
- AF10P_W22B61 → $2x10^{15}$ n_{eq}

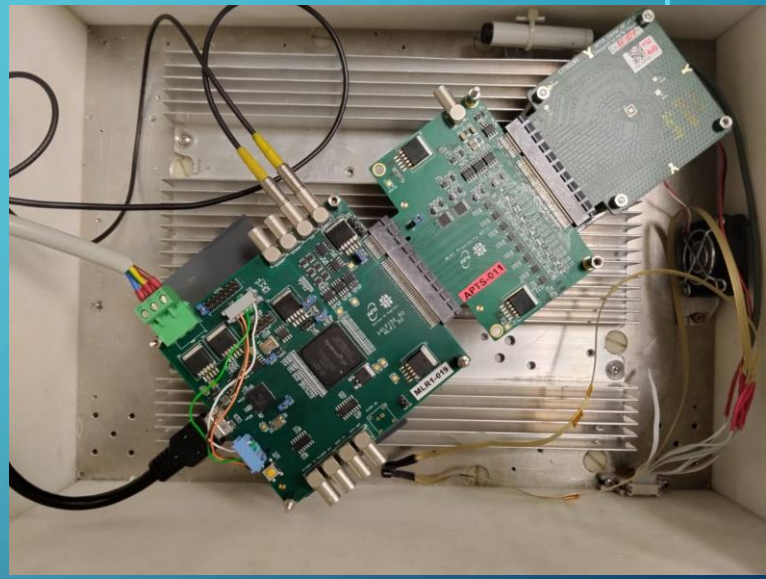
- basic source follower structure
- 10 µm pixel pitch
- Modified process with gap

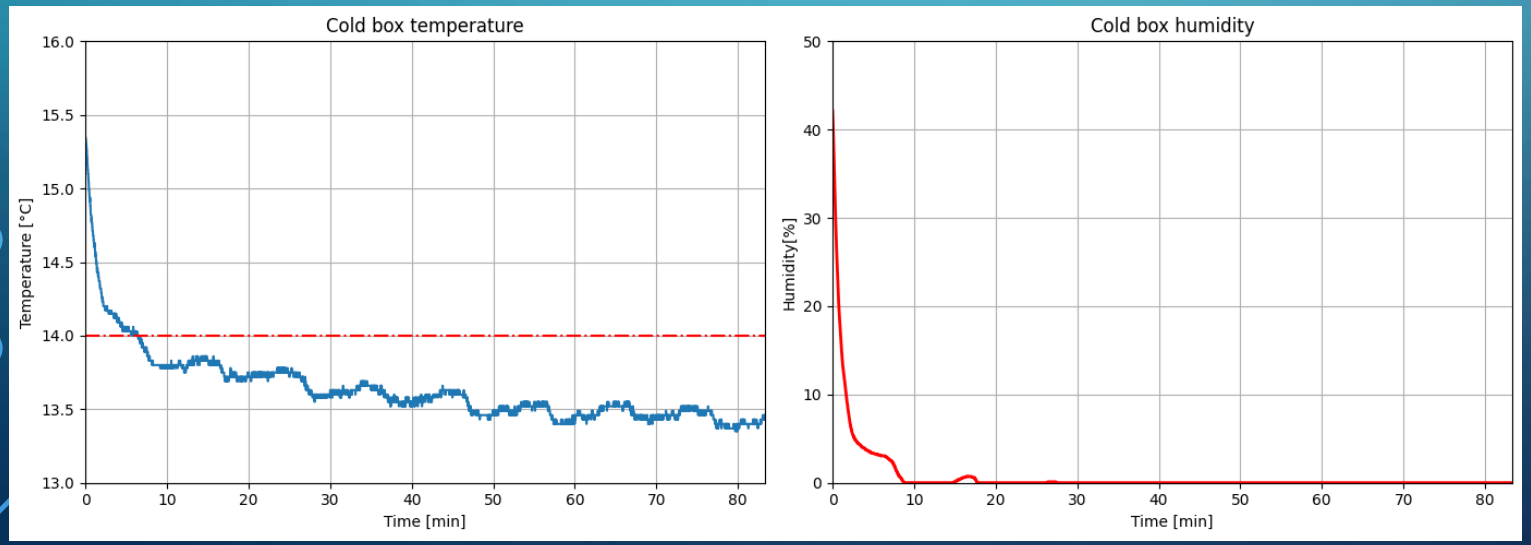


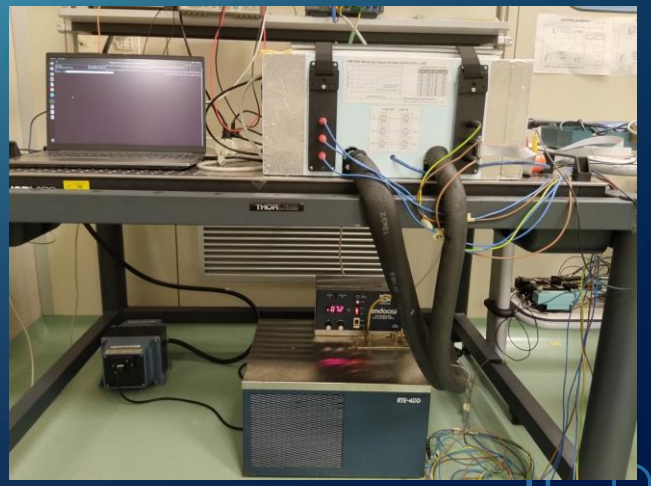
non-ionising, ionising, and combined doses were obtained by neutrons at JSI Ljubljana, 10 keV X-rays from a tungsten target at CERN, and 30 MeV protons at NPI Prague, respectively

IRRADIATED CHIPS TEST – COLD BOX

- Insulating walls box
- Cooled by a chiller – Peltier cooling possible (not needed):
- Need temperature of ~14°C

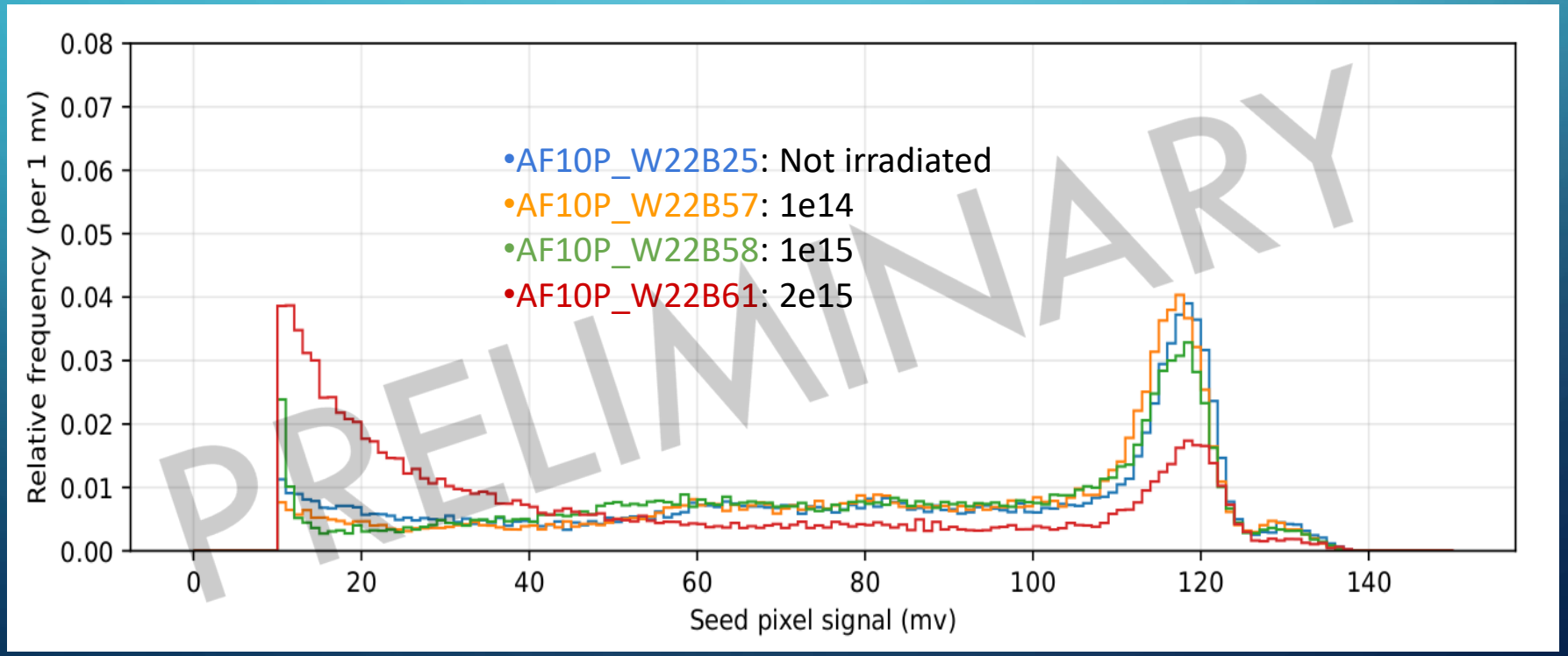






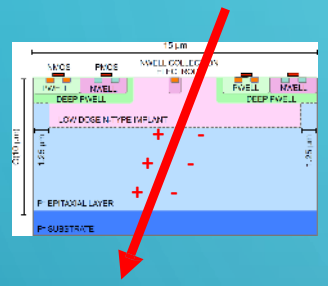
IRRADIATED CHIPS TEST – COLD BOX

- ^{55}Fe source
- Vbb = - 4.8 V

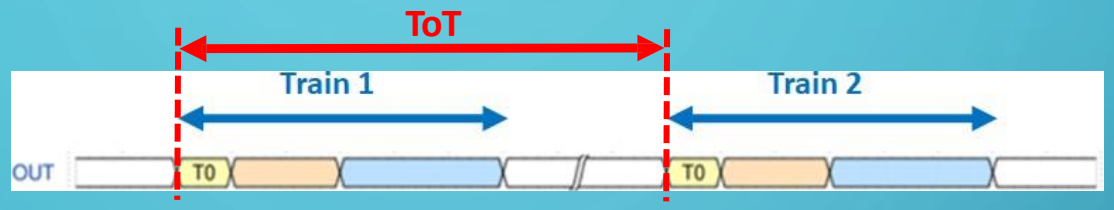


TRIESTE
DPTS TEST – ToT

- Two output lines: one positive and one negative

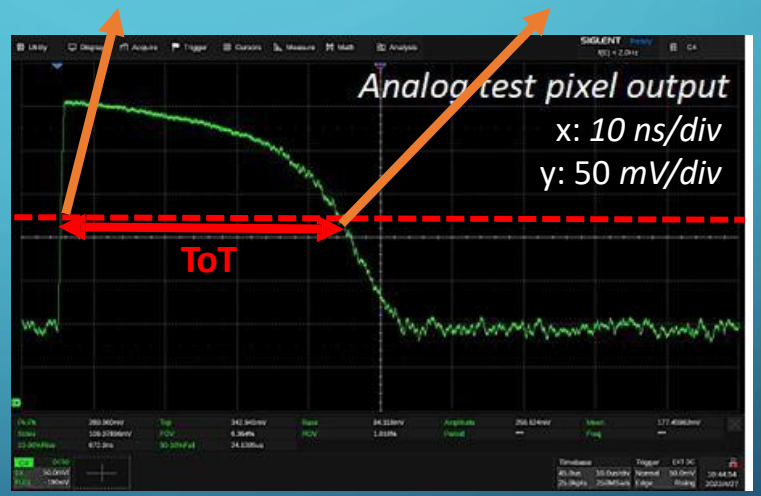


Output



- ToT measurement -> linked to signal amplitude

Threshold

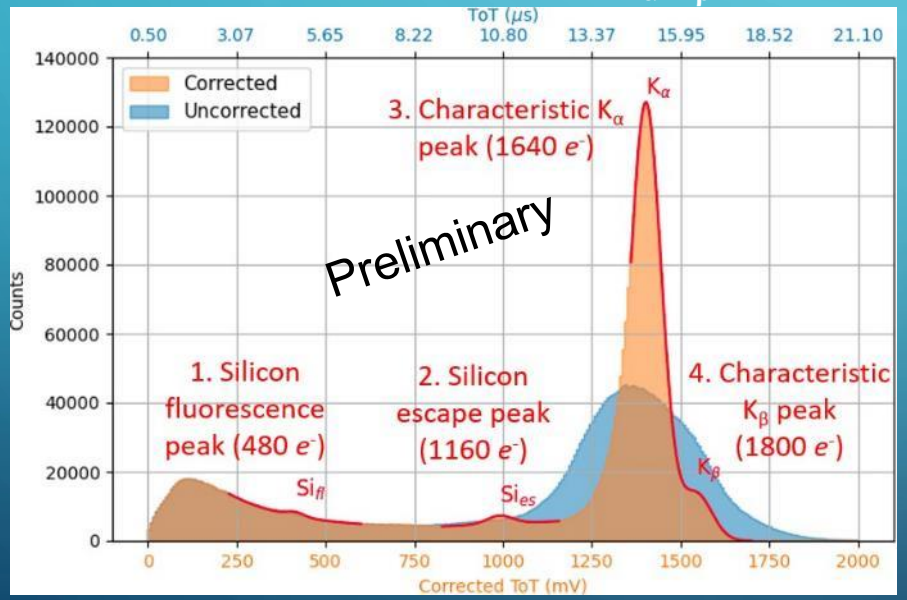


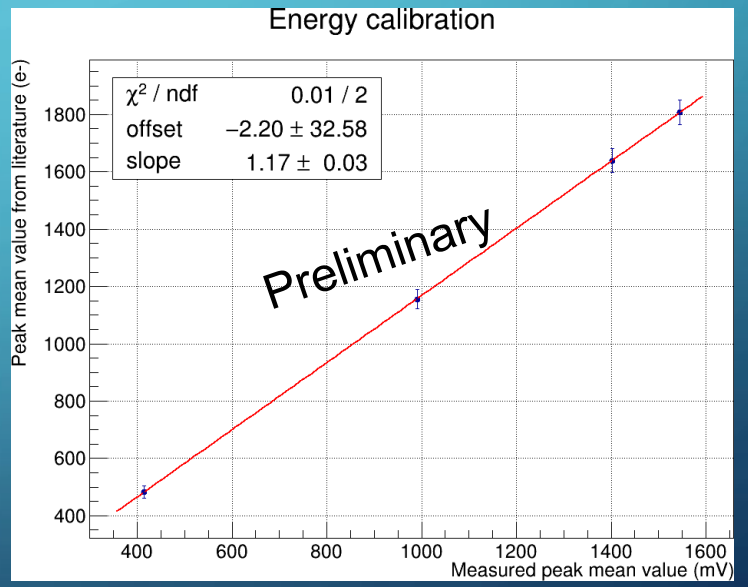
- For details, see paper:"Digital Pixel Test Structures implemented in a 65 nm CMOS process" arXiv:2212.08621v3, submitted to NIM-A

DPTS TEST – ENERGY CALIBRATION

- Two characteristic X-ray emissions + silicon fluorescence and escape peaks at fixed energies (corrected=calibrated, see paper cit.)

K_α,K_β of ^{55}Mn

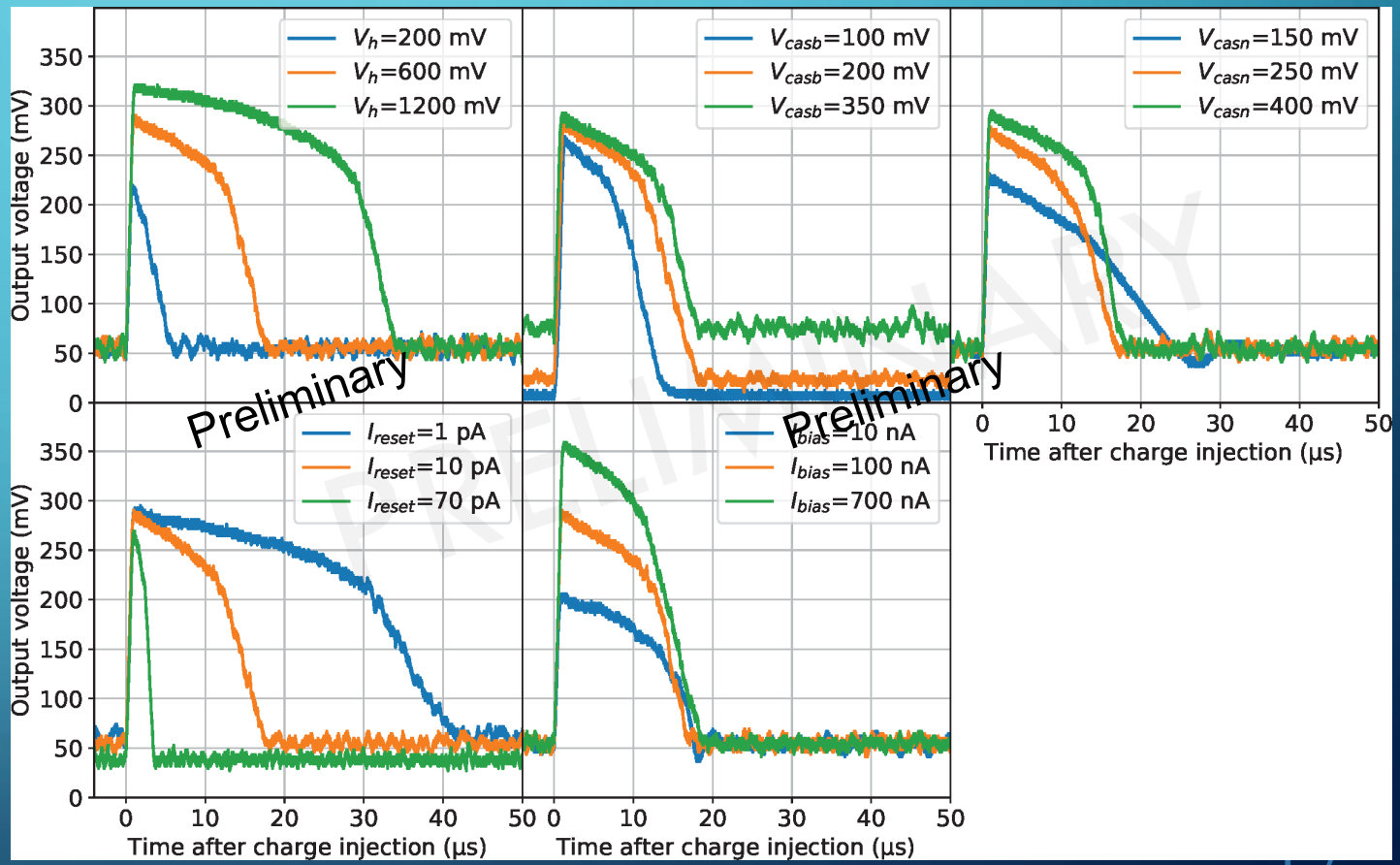




For details, see paper:"Digital Pixel Test Structures implemented in a 65 nm CMOS process" arXiv:2212.08621v3, submitted to NIM-A

DPTS TEST – PARAMETERS SCAN

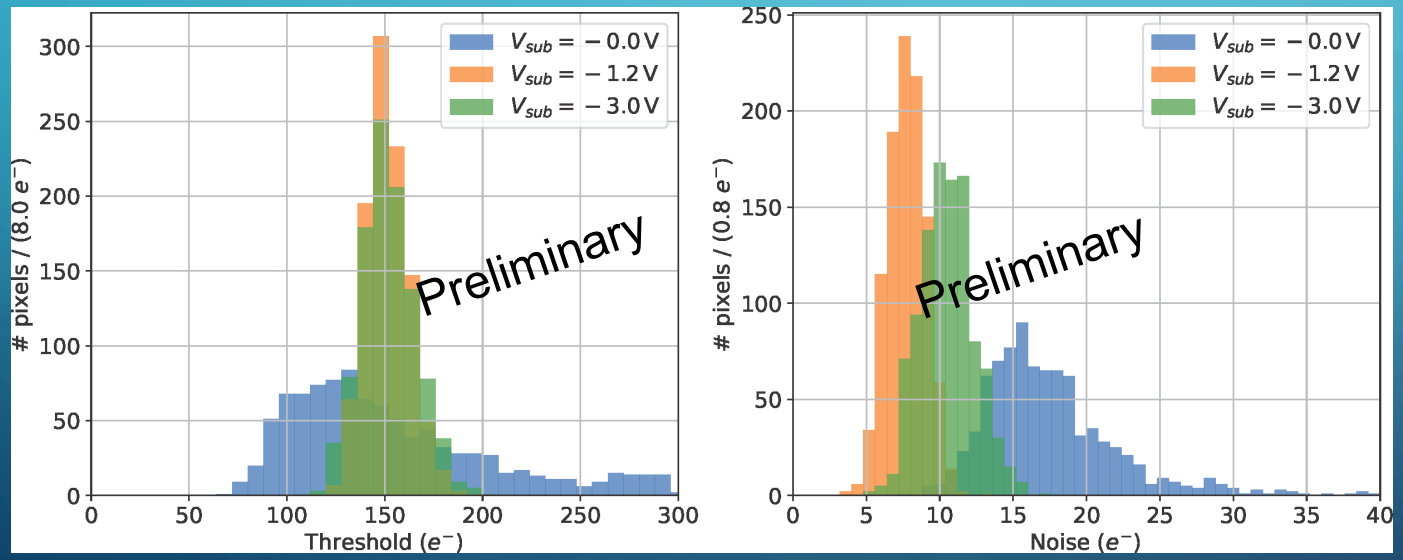
- Inject the analogue pixel
- Measure the response for different chip biases
- Provides a more intuitive understanding of the chip behaviour



For details, see paper:"Digital Pixel Test Structures implemented in a 65 nm CMOS process" arXiv:2212.08621v3, submitted to NIM-A

DPTS TEST - TRIESTE

- Comparable performance for Vsub = −1.2 V and – 3 V
- At Vsub = 0 V, the distribution is wider and asymmetric, indicating a substantial pixel-to-pixel threshold spread resulting in a non-uniform response across the matrix



For details, see paper:"Digital Pixel Test Structures implemented in a 65 nm CMOS process" arXiv:2212.08621v3, submitted to NIM-A


That's all Folks!