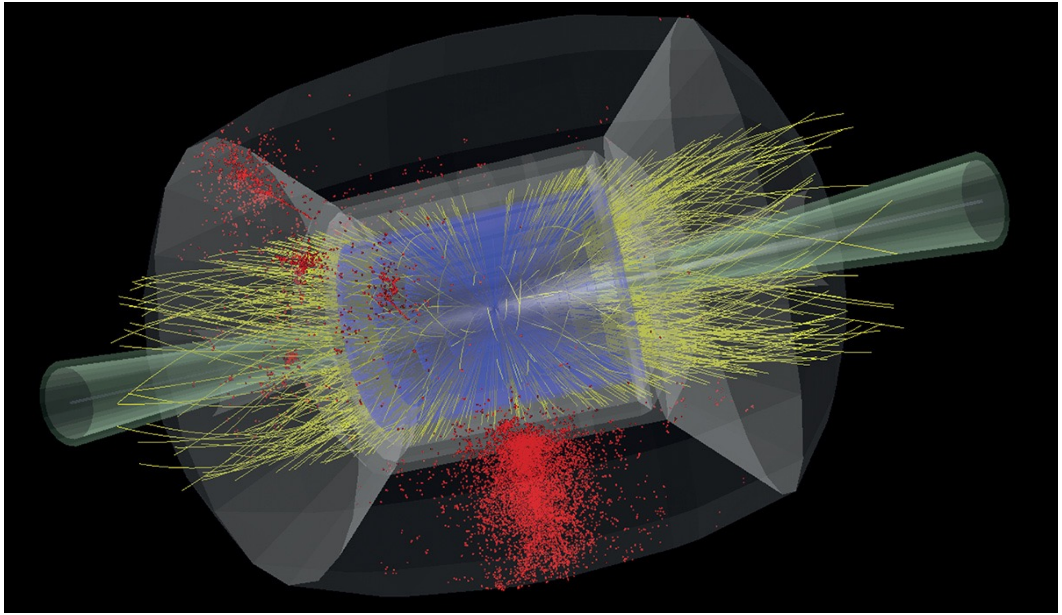


Occupancy and power considerations with large time windows for LLP signals

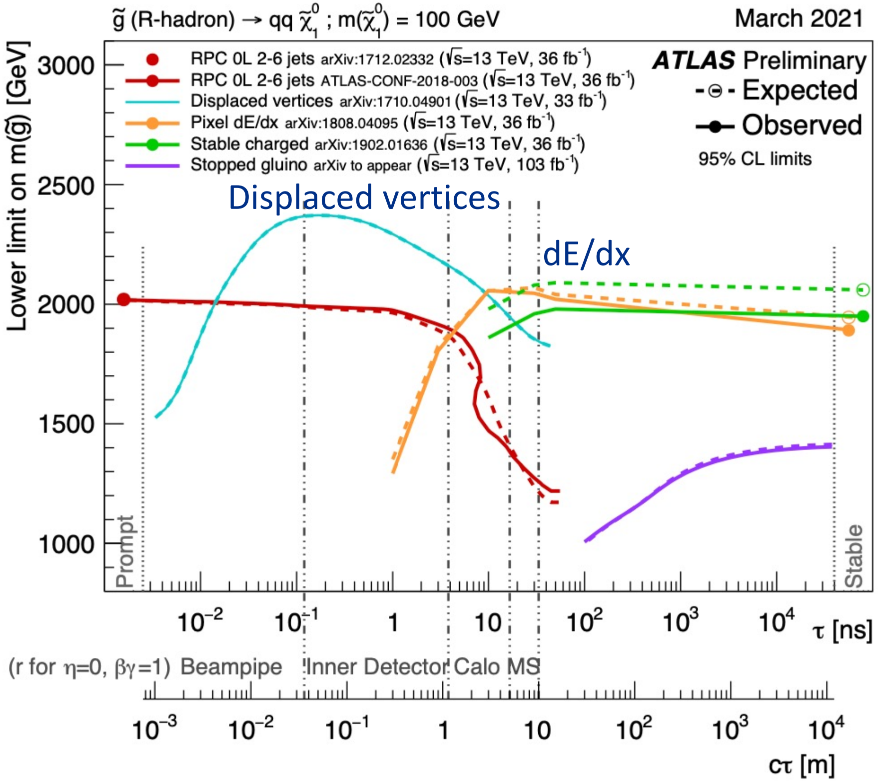
Sergo Jindariani (Fermilab) with big thank you to Massimo, Nazar, Ron Lipton, Alan Prosser

Feb 13, 2023

Introduction

- Are our timing cuts in the tracker prohibitive for LLP signals (displaced vertices, HSCP, etc) ? This question was asked at the Fermilab workshop in December
- TOF at the speed of light: 3 cm is 100ps, 1m is 3ns
  - At beta = 0.2 the corresponding numbers are 0.5ns and 15ns
- Can we use wider readout windows? Clearly, it does not have to be uniform – e.g. pixels can have a narrower window, but let's look at it
- Study based on tracker only BIB simhits, sample produced by Nazar - the time smearing effects in recohits should be negligible for this study
- The idea here is not to lock us into a specific scenario but rather to explore possible options

LLP signatures



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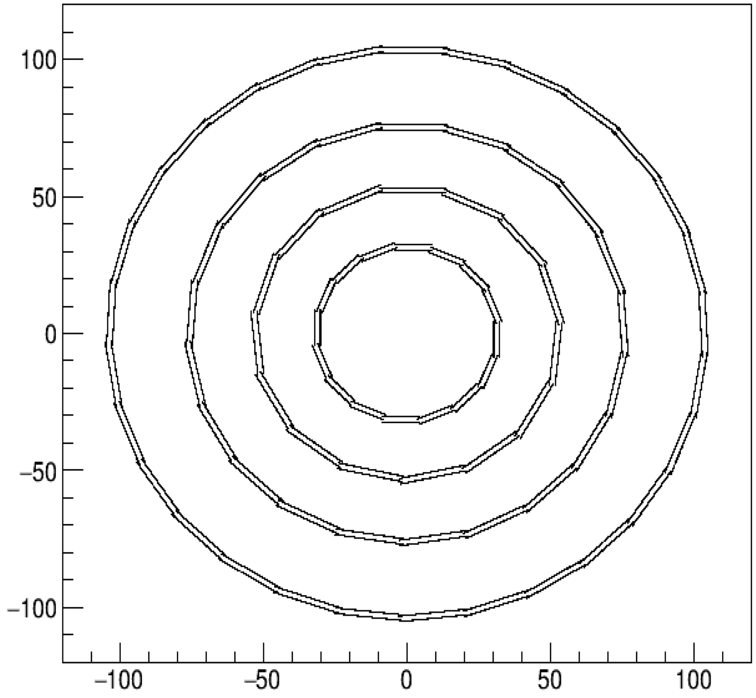
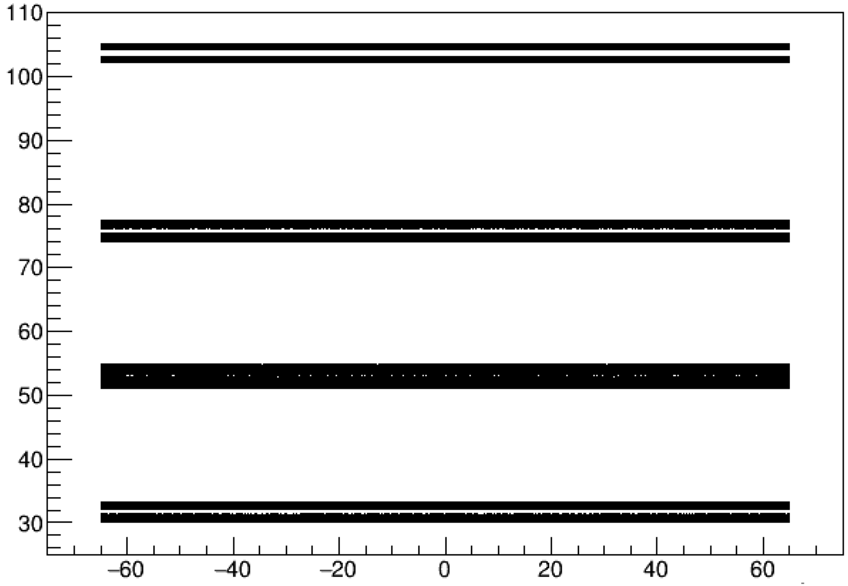
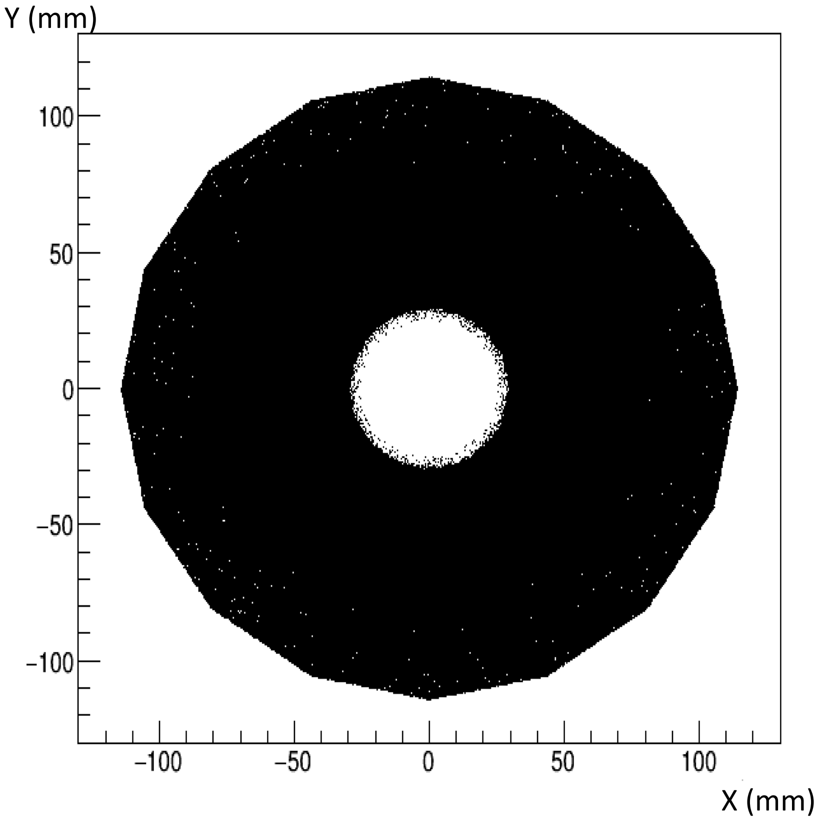
Understanding simhits – VXD Barrel

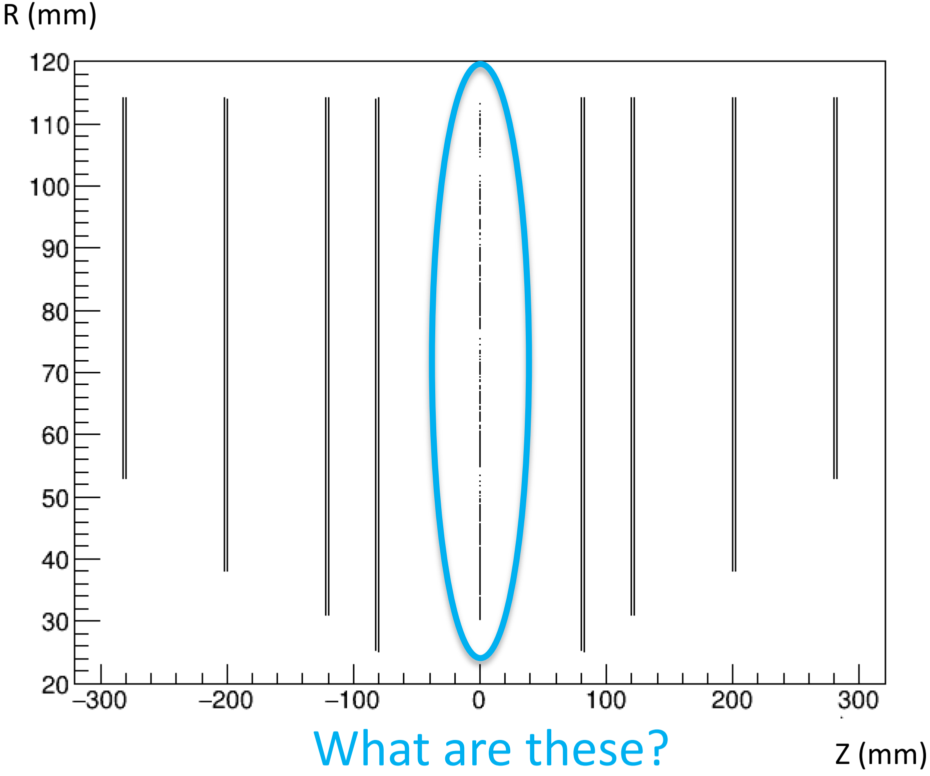




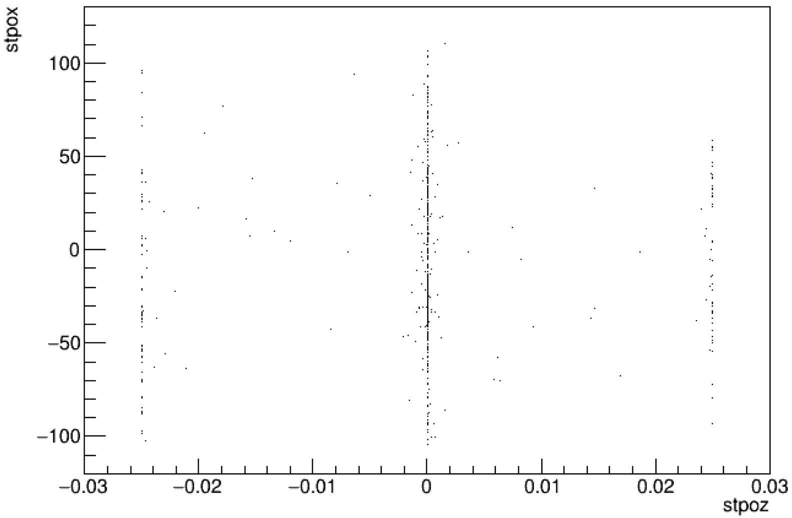
Understanding simhits – VXD Disks

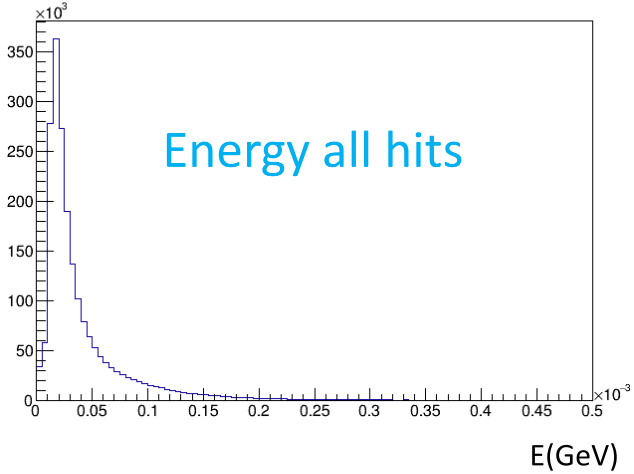
A small detour

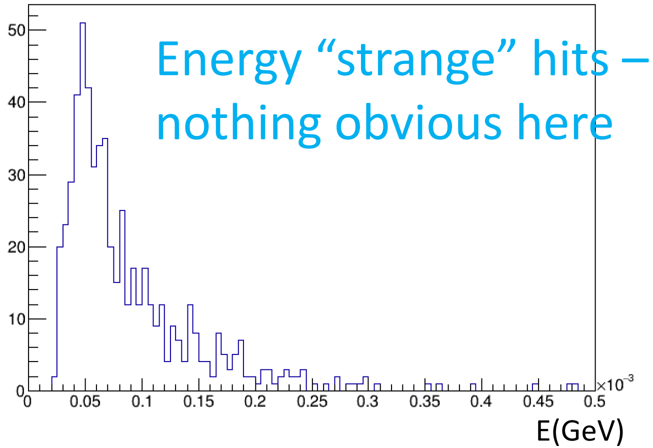




Small detour – VXD Disks

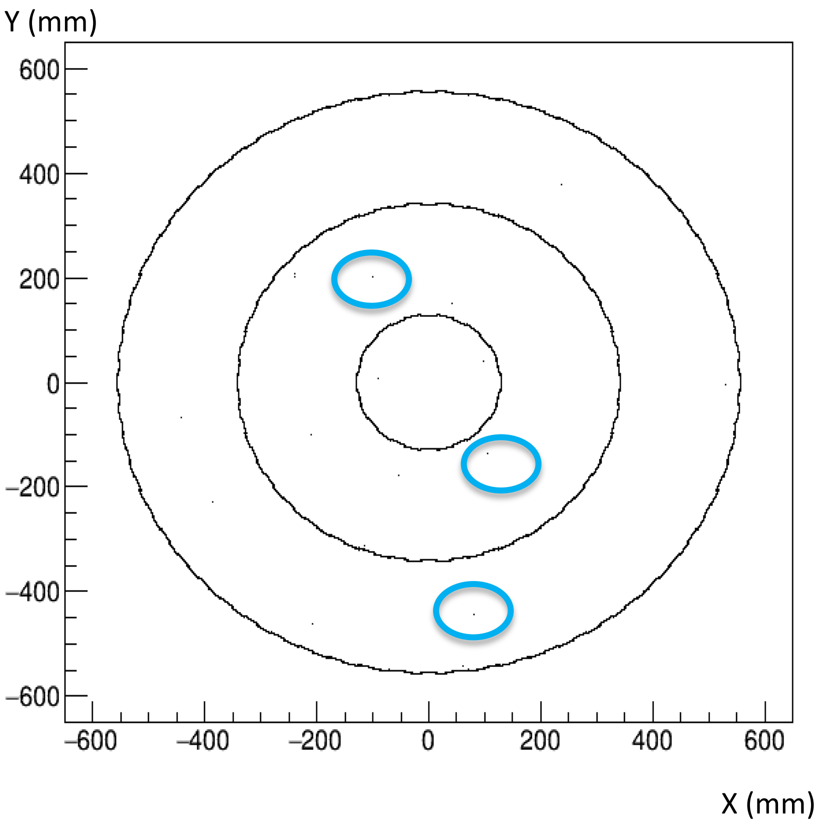


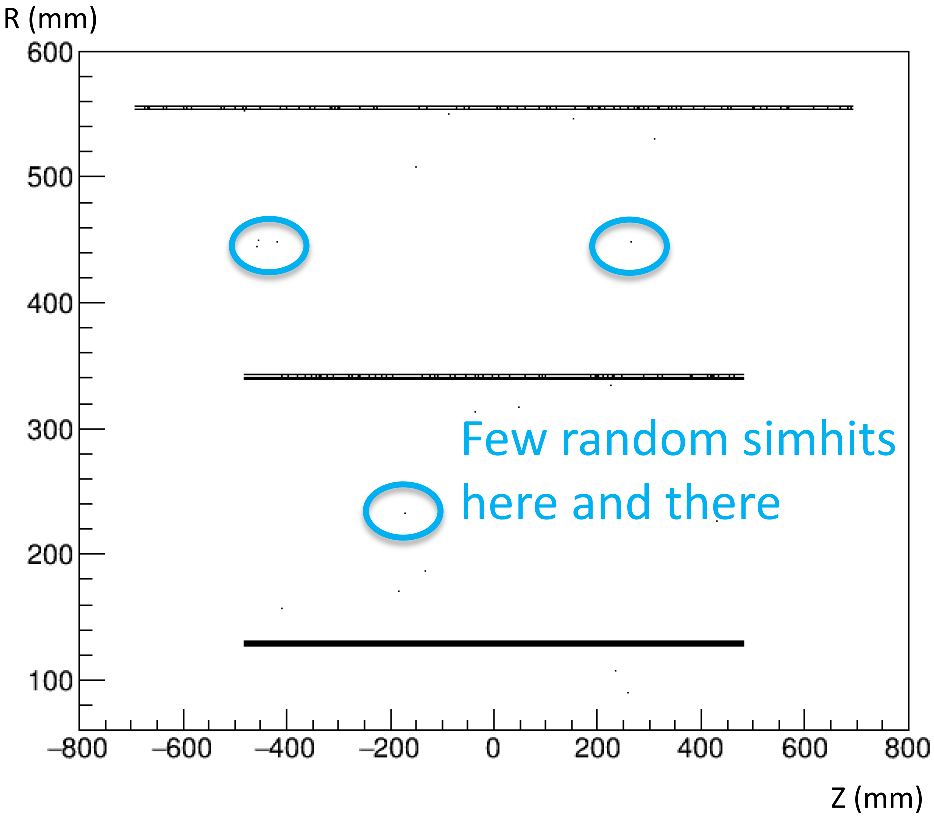




Only about 600 hits in total – negligible effect on the rates, but we should check what it is

Understanding simhits – IT Barrel





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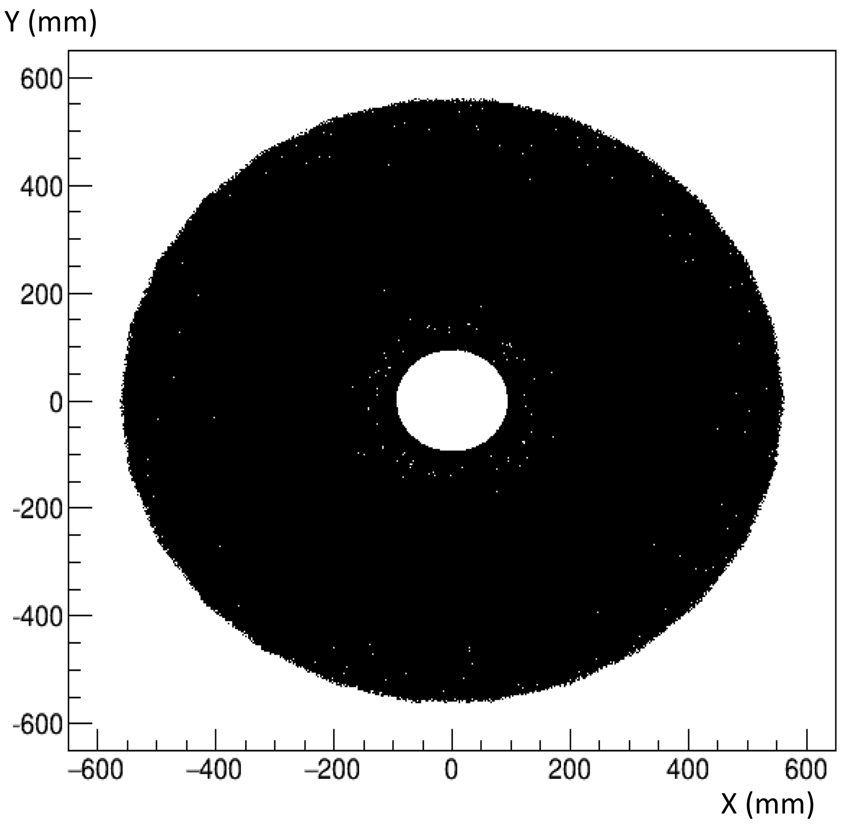
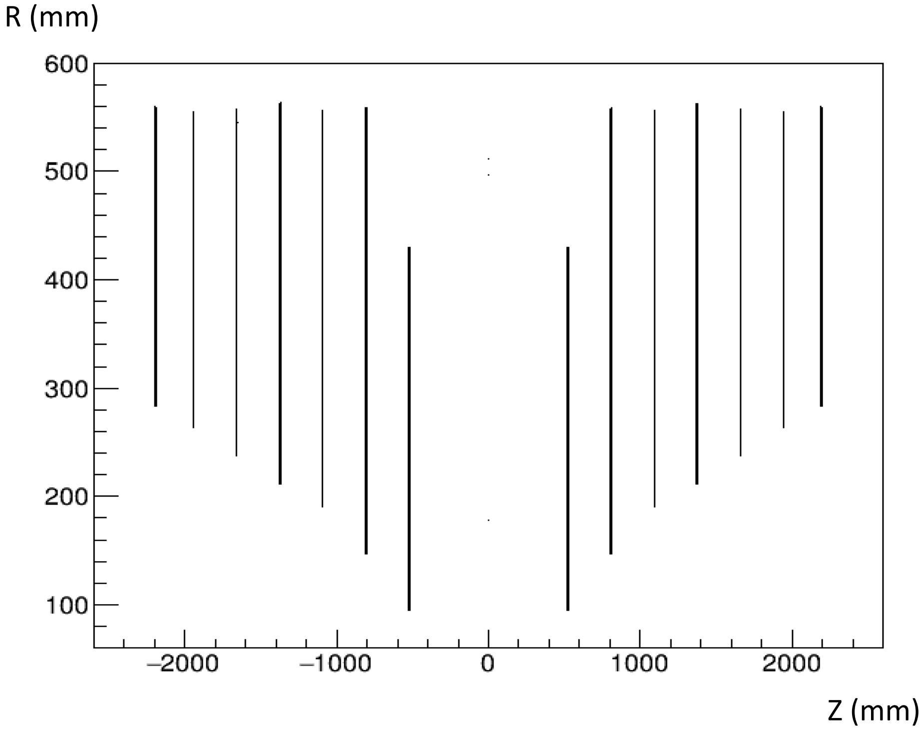
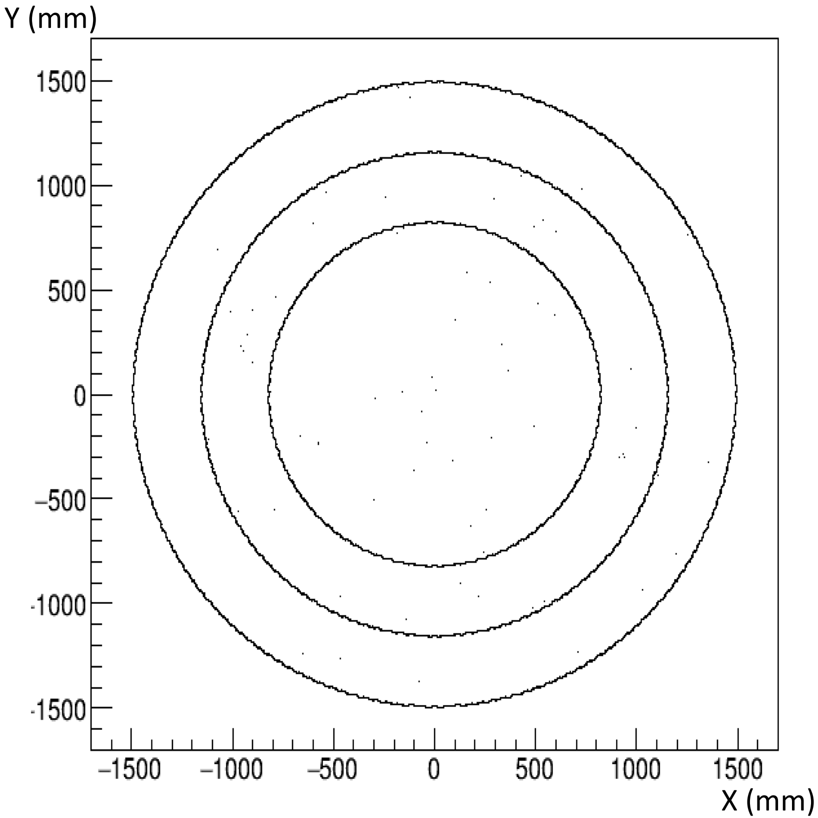
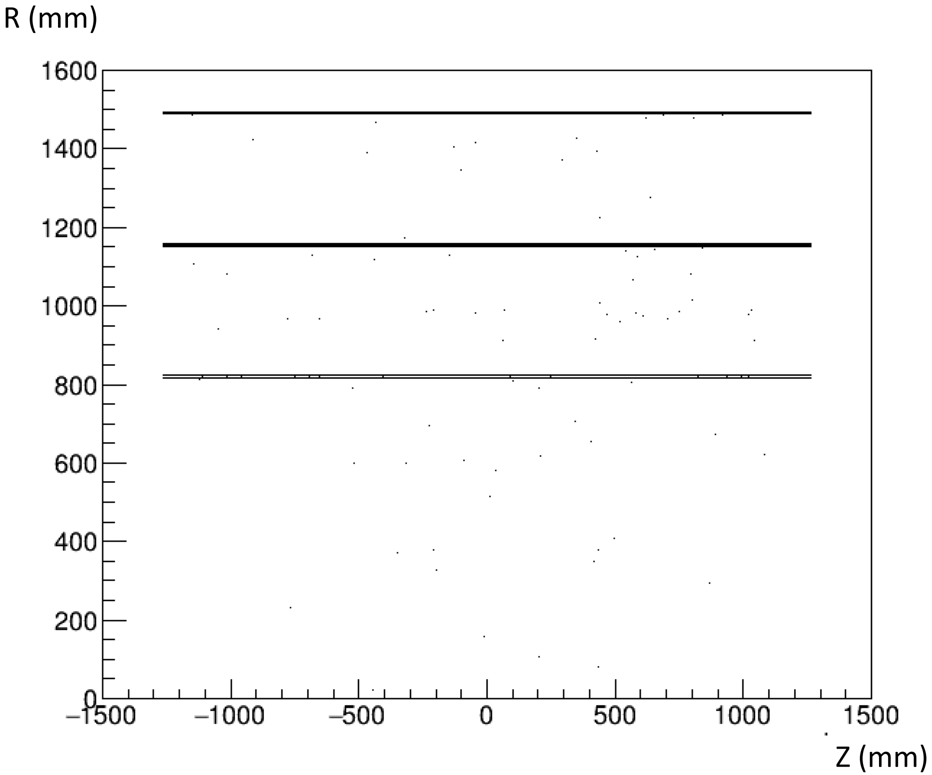
Understanding simhits – IT Disks



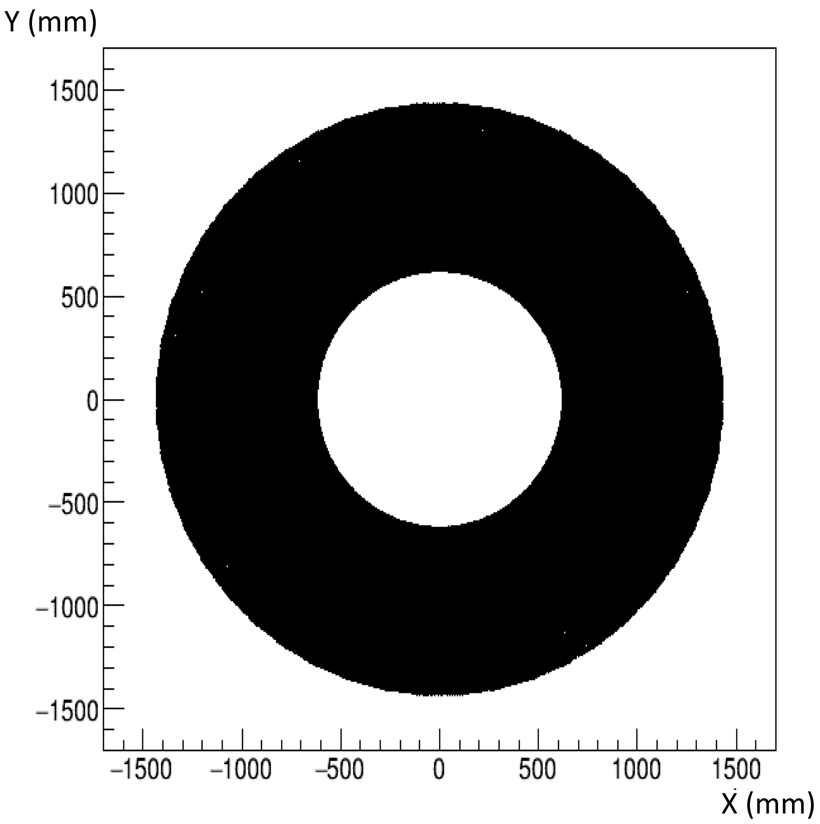


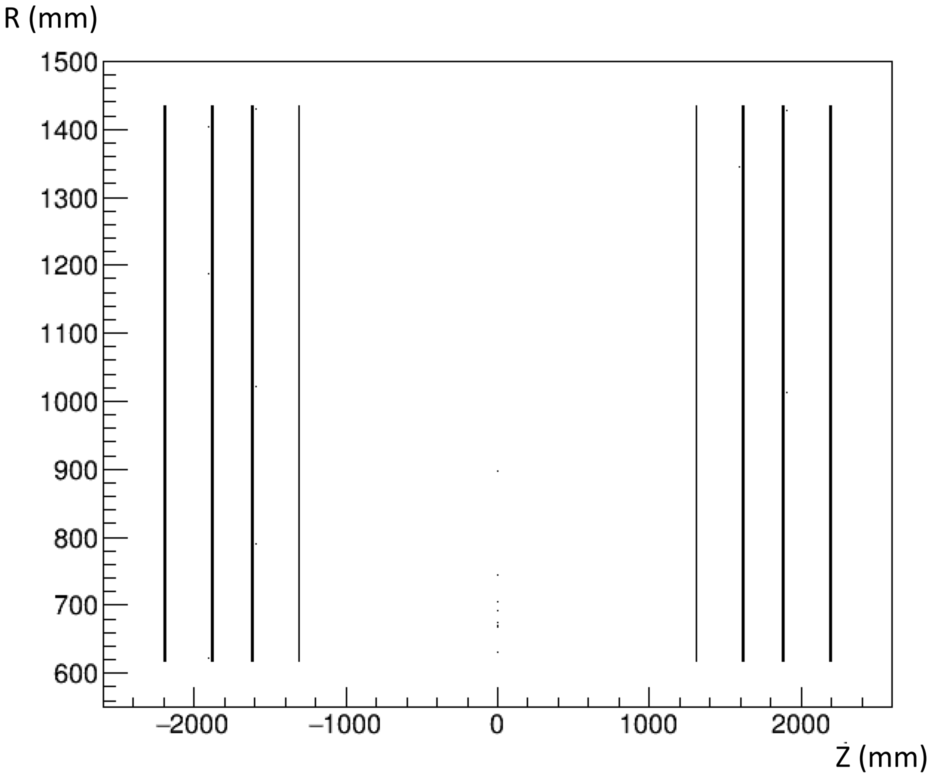
Understanding simhits – OT Barrel



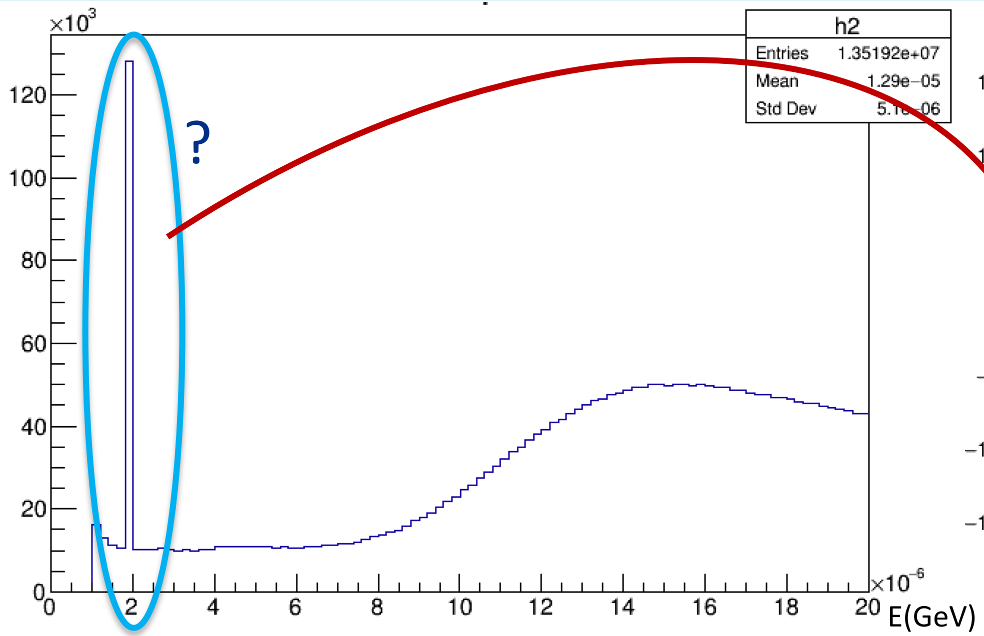


Understanding simhits – OT Disks

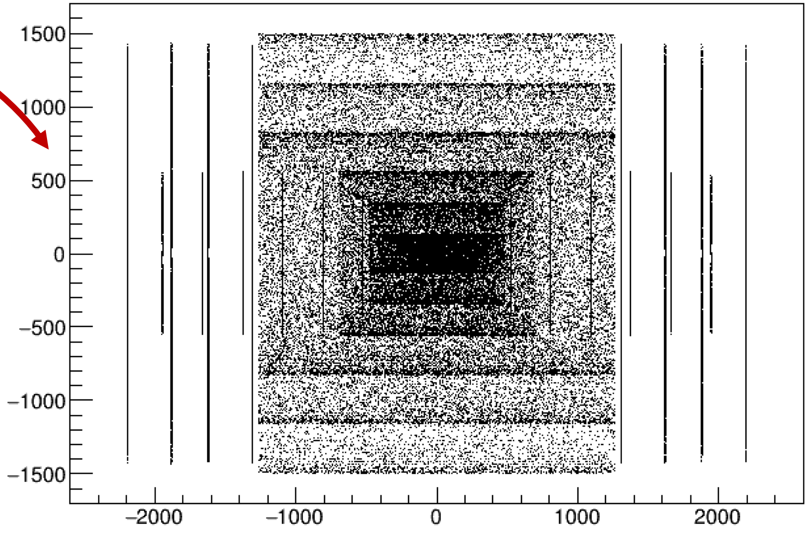




SimHit Energy Distribution



Not isolated in certain area

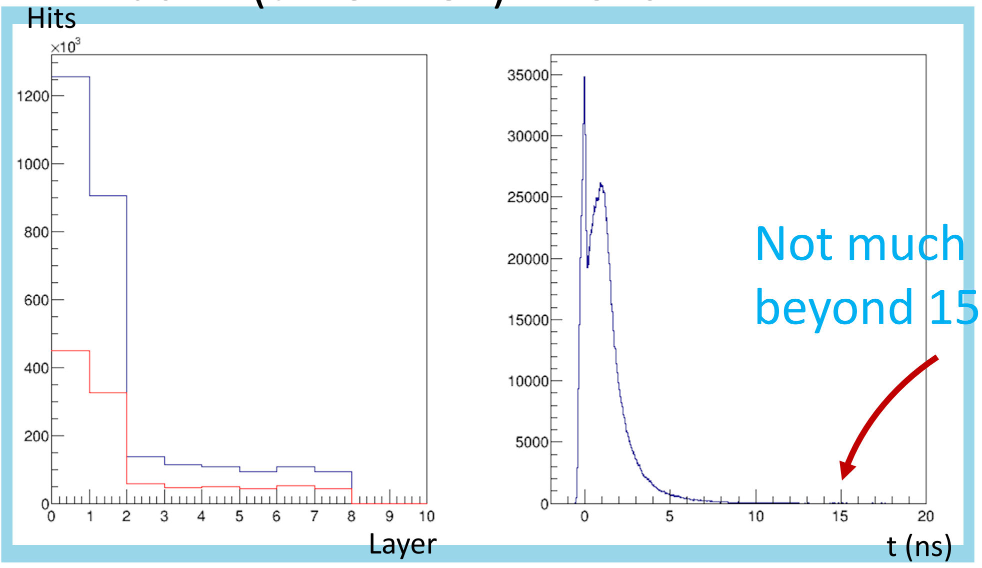


- Minimum energy is set at 1 keV, this is relatively low
- 3.6 eV needed to create an e-hole pair, ~ we require 300 electron-holes
- 1000 e- is a reasonable threshold => 3.6 KeV * thickness/100um
- The effect of cutting low energy hits on the hit multiplicity is small – about 1%

Hits per layer – VXD

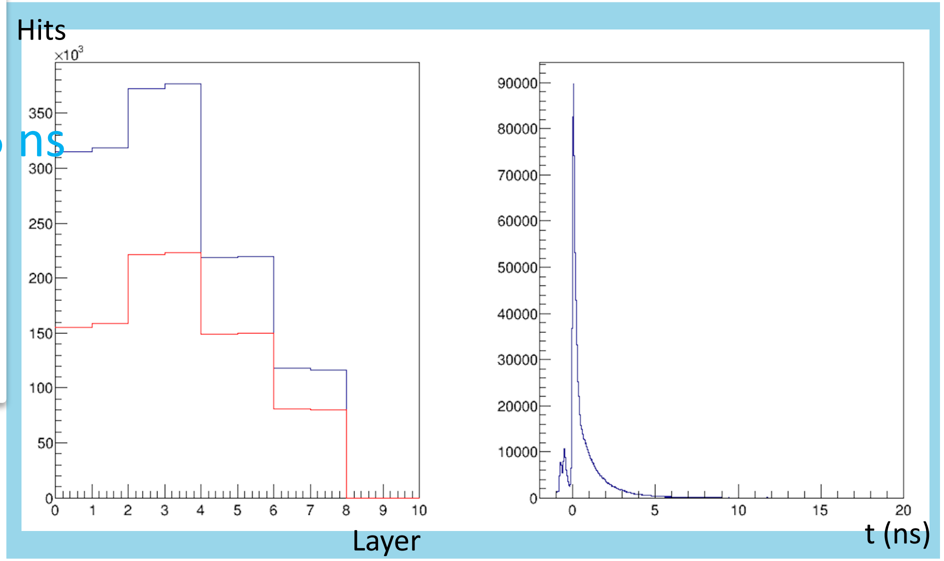
RED = (time – TOF) < 1ns

Black = (time - TOF) < 15ns



Barrel

Disks



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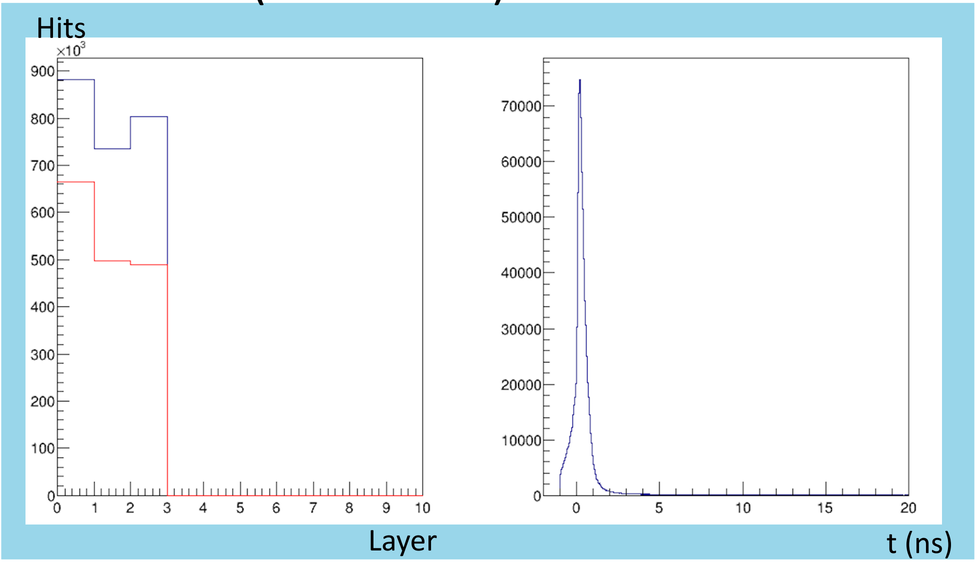
Hits per layer – IT

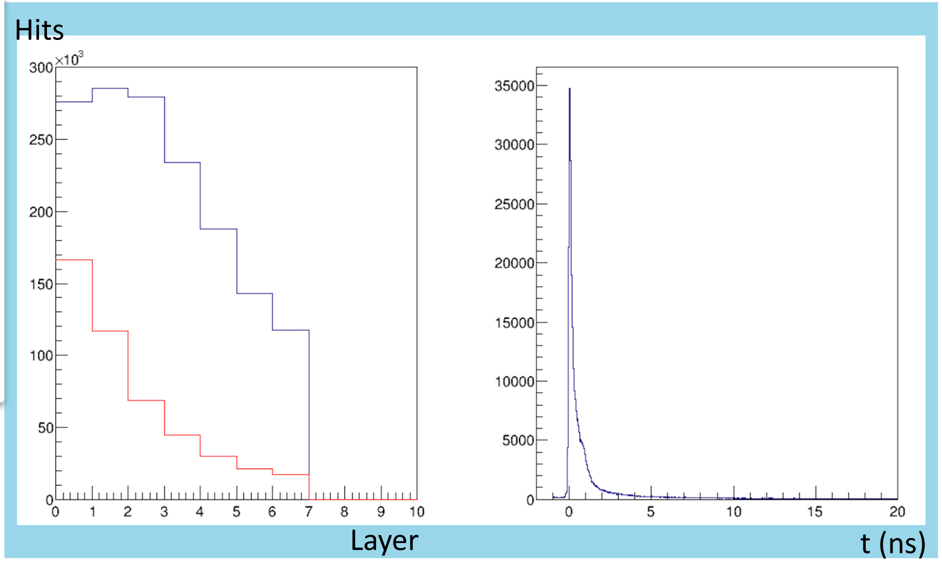
RED = (time – TOF) < 1ns

Black = (time - TOF) < 15ns



Barrel

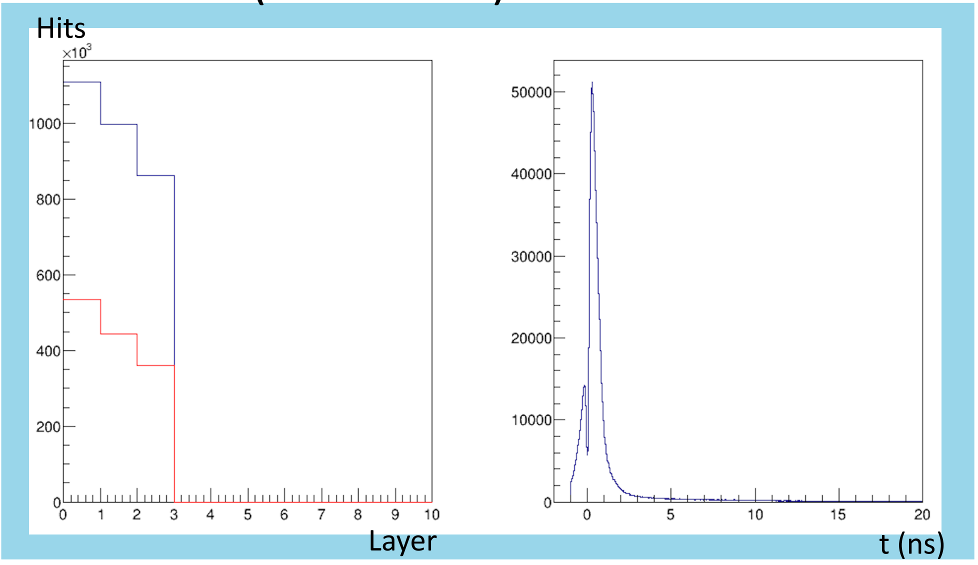
Disks



Hits per layer – OT

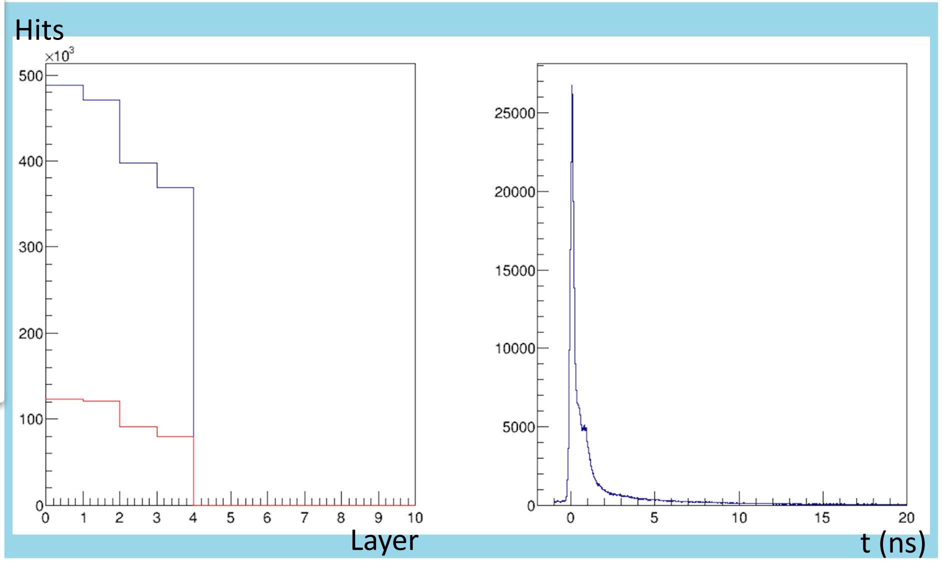
RED = (time – TOF) < 1ns

Black = (time - TOF) < 15ns



Barrel

Disks

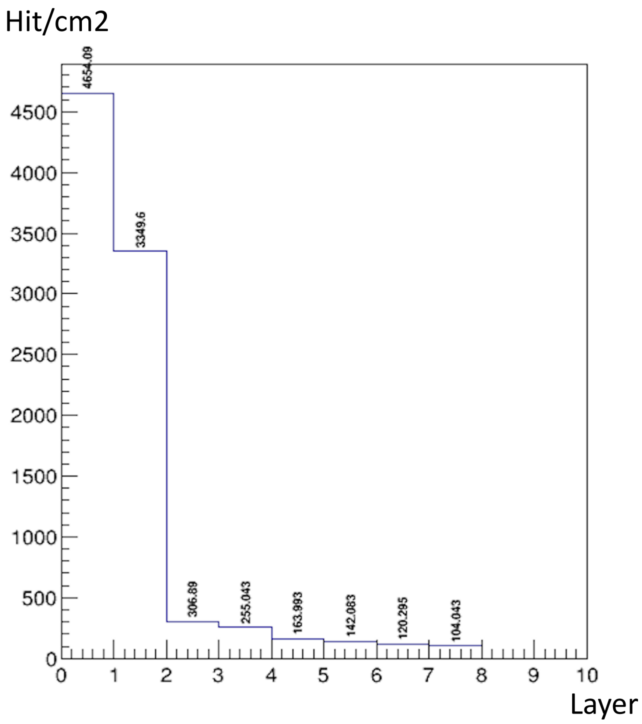


Surface Area – in cm^2 (numbers are approximate)

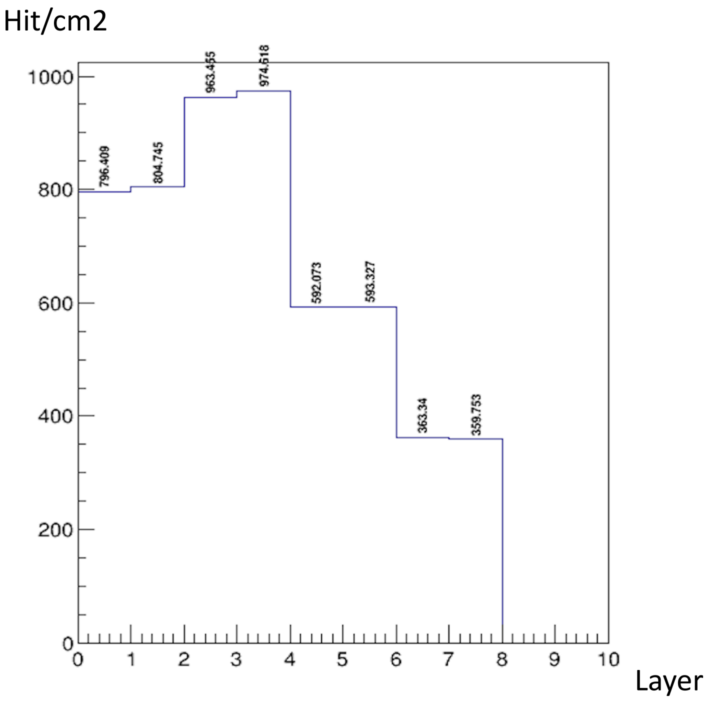
	L1	L2	L3	L4	L5	L6	L7	L8	Total
VXD barrel	270	270	450	450	650	650	900	900	4,540
VXD disks	400	400	390	390	370	370	320	320	2,960
IT barrel	7,690	20,580	48,200						76,470
IT disks	4,870	9,000	8,540	8,260	7,910	7,490	7,140		53,210
OT barrel	130,110	183,170	236,100						549,400
OT disks	52,280	52,280	52,280	52,280					209,100

Total area ~ 90 m^2

Occupancy per cm^2- VXD



Barrel



Disks

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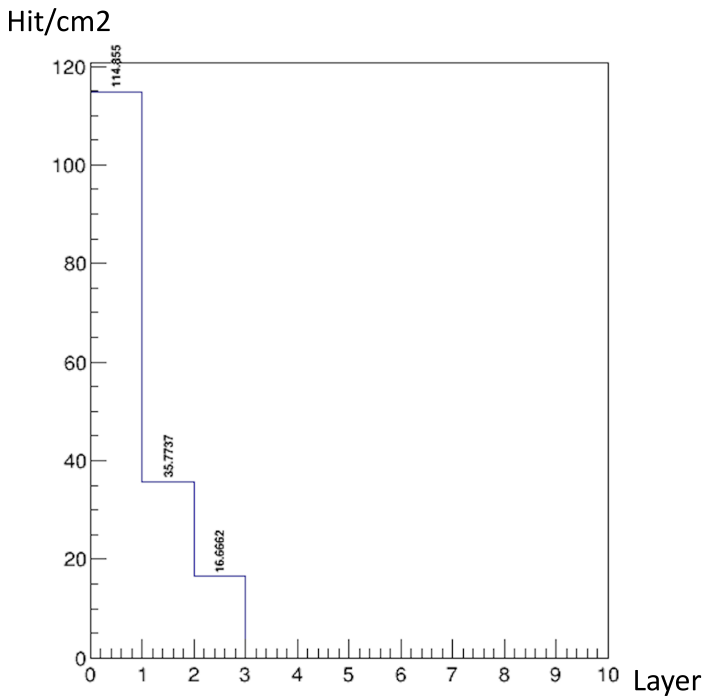
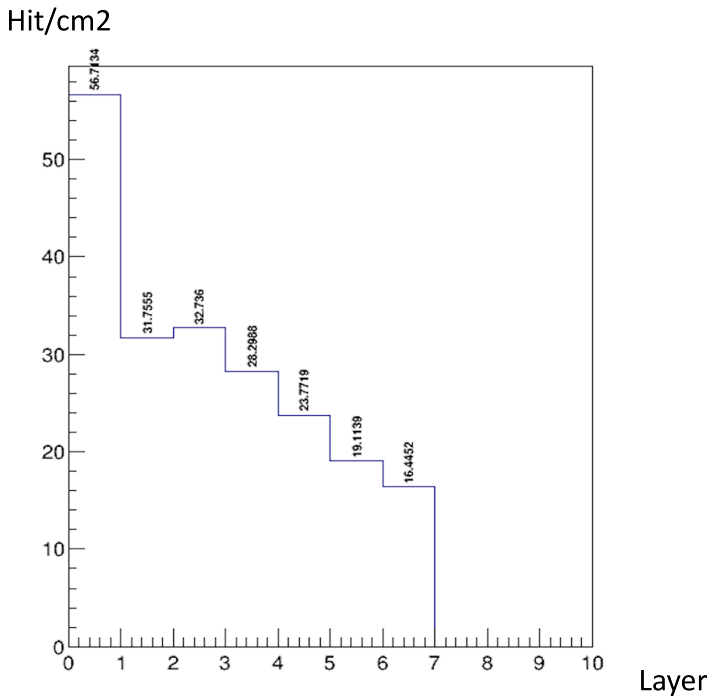
Occupancy per cm^2 - IT

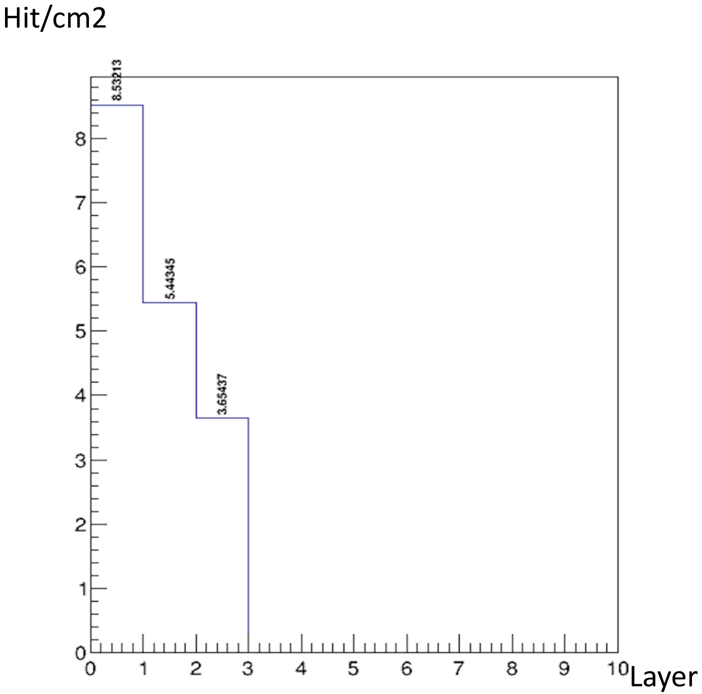


Barrel

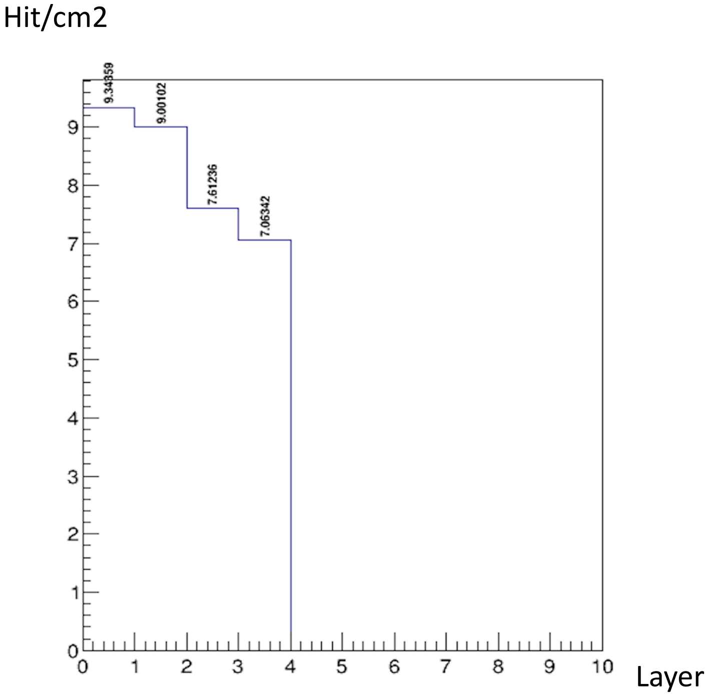


Disks

Occupancy per cm^2 - OT



Barrel



Disks

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A slide on high speed link R&D

- What speed is reasonable to assume in 20 years? Note that I am ignoring chip challenges (which can be significant) and focusing entirely on the speeds needed to bring the data out for HLT/offline processing

- LP-GPT aims to achieve one-directional speed of up to 10 Gbps for HL-LHC

- Use optical intensity modulators
  - Lithium-Niobate Mach-Zehnder modulators can operate at 40 Gbps on a single wavelength
  - Possibility of using Wavelength Division Multiplexing - additional gains
  - Lower power than direct modulation
  - Challenges – sensitivity to the environment (temperature), rad-hardness

- Have multiple channels, for example 4 operating at a single wavelength and 10 Gbps
  - Freedom Photonics (FP) and UCSB were working on an SBIR project with input from FNAL

- 40 Gbps is in my opinion a reasonable conservative assumption

Power expectations

- lp-GBT ~ 40 pJ/bit
- Comprehensive overview of what is achievable : Link to Paper
- Table 1 provides a comprehensive comparison of key performance parameters for 100G + optical transmitters
- Numbers are typically < 10pJ/bit, some as low as < 1pJ/bit
- I will assume 10 pJ/bit here (in line with past assumptions used in our "technology" paper)
- No power pulsing – I think power pulsing is difficult (if not impossible) at MuC with bunch crossing intervals of 10 microseconds

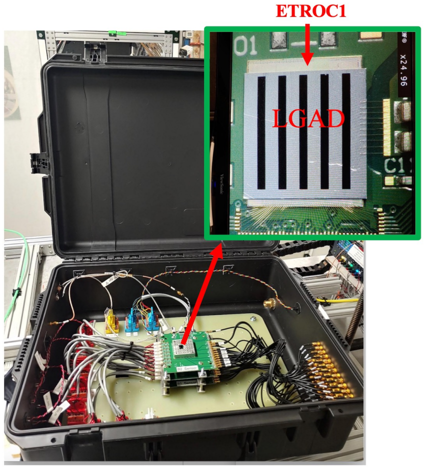
Convert into Data Rates and Power

	Upper timing cut (ns)	Module size (cm^2)	Maximum hits/cm^2	Reduction using cluster shapes	Data payload per module (Gbps)	Transmission power per module (W)	Total Transmission Power (W)
VXD barrel L1/L2	15	10	4600	x2	70	0.7	38
VXD barrel L1/L2	1	10	1600	x2	25	0.25	14
VXD barrel L3-8	15	10	300	-	9	0.1	18
VXD disks	15	10	1000	-	30	0.3	88
IT barrel	15	50	100	-	14	0.14	214
IT disks	15	50	60	-	9	0.09	96
OT barrel	15	100	10	-	3	0.03	165
OT disks	15	100	10	-	3	0.03	63

Estimating FE digital power

- We assume that every pixel (down to 25x25 microns) provides a precise time stamp. These are thousands of pixels per cm^2 - challenging

- Timing detectors are power hungry!
- Consider example of ETROC (CMS Endcap timing detector FE chip):
  - LGAD with large pixel size 1.3x1.3 mm^2
  - 65nm CMOS chip
  - TDC for every pixel
  - Power dominated by pre-amp and discriminator (2 mW level/channel) - large detector capacitance and small input charge
  - TDC power is 0.1 mW/channel



- bias power is typically negligible – high voltage but very low currents

Estimating FE digital power

- VXD:
  - Lower capacitance in MuC –estimated 40 fF (per Ron), this should help to keep the pre-amp power down (~ x100) wrt ETL
  - 25x25 microns allows very little space for transistor logic even at 28nm – cannot have TDC for every pixel
  - Occupancy 1% - one TDC per 100 pixels ?

	Technology	Pixel size (mm^2)	Detector Capacitance (pF)	Preamp power per channel (mW)	Total preamp power (kW)	TDC Power per channel (mW)	Total TDC Power (kW)
CMS ETL	LGAD	1.3x1.3	3.5	2	16	0.1	0.8 kW
VXD	?	0.025x0.025	0.040	0.02	0.2	0.1 (?)	1.5 kW

Cooling capacity

So total power L1/2 of VXD detector is:

- Per cm^2: 1.6 W (FE) + 0.3 (transmission)/ 10 cm^2 ~ 200 mW/cm2

- Air cooling power dissipation assumptions vary significantly in literature:
  - ILC 100 mW/cm^2
  - CLIC 50 mW/cm^2
  - Recent studies with Helium cooling achieve up to 400 mW/cm^2

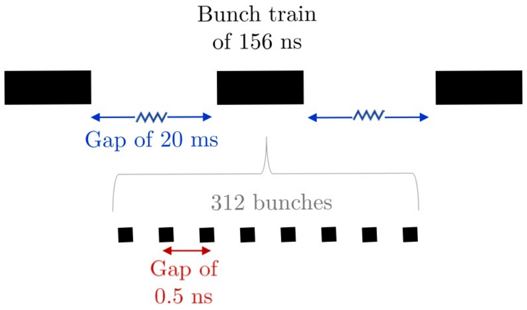
- Conventional CO2 cooling is capable of dissipating more power but would lead to extra material in the system → degraded performance (by how much?)

Summary

- Preserving delayed hit efficiency for exotic signatures in the tracker appears possible from the bandwidth and power point of view
- Wider time windows outside of the first 2 layers of VXD do not lead to unmanageable data rates
- For the inner 2 layers of VXD, the time window will probably need to be kept tight, but this should not be prohibitive of LLP searches
- Power estimates indicate that helium flow cooling is promising
- The study is simplistic as it assumes that every pixel can provide precise timing. Studies with more realistic FE constraints need to be carried out

Power Pulsing for CLIC

Introduction



Beam structure

- e^+e^- collision
- Trains of 312 bunches
- Spacing between bunches: 0.5 ns
- **Gap between trains: 20 ms** (50 Hz rate)

- Important for power pulsing since the electronics can be switched off most of the time.
- Study of the power-off state.

Vertex detector requirements

- Single point resolution $\sigma \sim 3\ \mu$m
- Time slicing of 10 ns
- **Power dissipation below 50 mW/cm²**
- **Ultra-low mass (~ 0.2 % χ_o per layer)**

Motivates power pulsing to reduce the heat dissipation and thus the cooling material.