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High frame-rate detectors for hard X-ray applications

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Two new ASICs have been developed for the readout of CdZnTe and similar detectors materials used for hard X-ray measurement. Although the two ASICs are targeted at different applications and use different CMOS process nodes, they implement the same concept of utilising in pixel digitisation and Gbps scale serialisers to operate at high frame rates. A common DAQ design is employed to aggregate the high data bandwidths and convert raw data into manageable, processed data formats in FPGAs. The design, performance and applications will be presented.

HEXITEC-MHz is a hyperspectral X-ray detector that measures the energy of each individual X-ray photon up to 300keV with a <1keV FWHM energy resolution. Each detector has 80x80 pixels on a 250μm pitch with an integrating amplifier with correlated double sampling. Each 2x8 pixels share a ramp-based TDC with 12-bit resolution. Every 4 columns are readout on independently controlled 4.1 Gbps serialisers with Aurora encoded 64b66b data. The 180nm CMOS process ASIC operates with a 1MHz frame rate and in conventional operating modes, measuring 1 photon per 3x3 pixels to be able to reconstruct charge sharing events, provides a count rate of ~10⁶ photons/mm²/s. Results from CdZnTe and p-type Si detectors will demonstrate the <1keV FHWM energy resolution and the ability to integrate multiple monochromatic photons in a frame and measure ~10⁸ photons/mm²/s.

DynamiX is an to measure the large intensity signals from 4th generation synchrotron facilities such as the proposed, Diamond II. A first test structure ASIC has been manufactured with 16x16 pixels on 110μm pitch with a view to scaling to 192x192 pixels in the future. The ASIC uses a two-stage charge cancellation design. The first "coarse stage"is optimised to cancel 25 photons at 25 keV at rates >100MHz with an 8bit counter. The second "fine stage"is designed to subtract charge at 0.2 photon segments with a 7bit counter. An "out of range"bit is included to give a 16bit value per pixel. The final operating mode will use the synchrotron RF clock (499.96 MHz) to drive and synchronise the ASIC with an integration time of 1.82μs, matching the rate of 1 turn of Diamond. At this 533kHz frame rate, the counting capability is ~10¹¹⁻¹²photons/mm²/s. The data is output on similar serilaisers to HEXITEC-MHz, with 64b66b aurora encoded which can reach 14Gbps in the 65nm process. The ASIC is programmable so that other energy X-rays, charge cancellation magnitudes and frame rates can be selected. The first test ASIC will be used to continuously readout CdZnTe detectors at up to ~10¹² photons/mm²/s and verify that the detector material is stable and suitable for these extreme applications in photon science.

Summary

Primary author: WILSON, Matthew (UKRI-STFC)

Co-authors: DENT, Andrew (Diamond Light Source); CLINE, Benjamin (UKRI-STFC); SOLE, David (UKRI-STFC); GIMENEZ-NAVARRO, Eva (Diamond Light Source); EVANS, Gwyndaf (Diamond Light Source); MATHESON, John (UKRI-STFC); NOBES, Joseph (UKRI-STFC); JONES, Lawrence (UKRI-STFC); FRENCH, Marcus (UKRI-STFC); PRYDDERCH, Mark (UKRI-STFC); HART, Matthew (UKRI-STFC); LARKIN, Matthew (UKRI-STFC); VEALE, Matthew (UKRI-STFC); WHEATER, Rhian (UKRI-STFC); SCULLY, Shane (Diamond Light Source); BELL, Stephen (UKRI-STFC); GARDINER, Thomas (UKRI-STFC); NICHOLLS, Tim (UKRI-STFC); HELSBY, William (UKRI-STFC)

Presenter: WILSON, Matthew (UKRI-STFC)

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