dRICH prototype readout

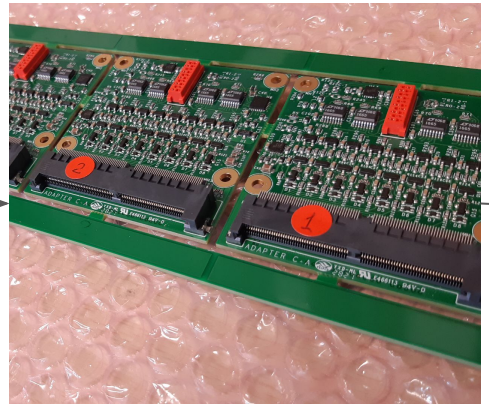
Roberto Preghenella
for the **sipm4eic-elettronica** group

dRICH SiPM optical readout unit (prototype)

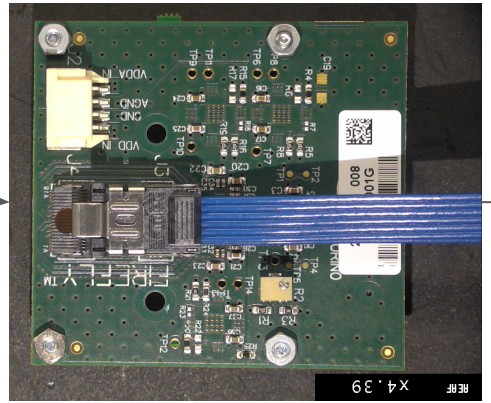
- **large-area SiPM optical readout for the dRICH prototype**
  - based on ALCOR readout
  - milestone deadlines
    - realisation: April 2023
    - beam test: October 2023
- **SiPM sensors and layout**
  - each readout unit comprises of
    - 4 Hamamatsu 8x8 matrices
    - 256 channels
  - ~ 52 x 52 mm² area
- **design with layout as close as possible to needs for final experiment**
  - critical engineering exercise in view of TDR
  - place cooling and electronics on the back of the sensors
- **use as much as possible of current electronics architecture**
  - no manpower capacity to develop new FPGA board this year
  - no manpower capacity di develop new firmware this year
  - use ALCORv2 (32 channels)
- **design new electronics boards to fit the new layout configuration**
  - possibly with the same features, if all needed

Current scheme

SiPM carrier



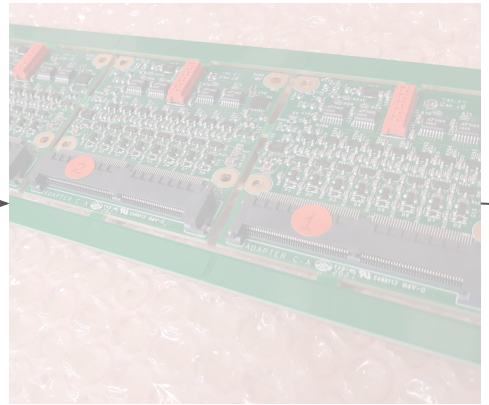
adapter board

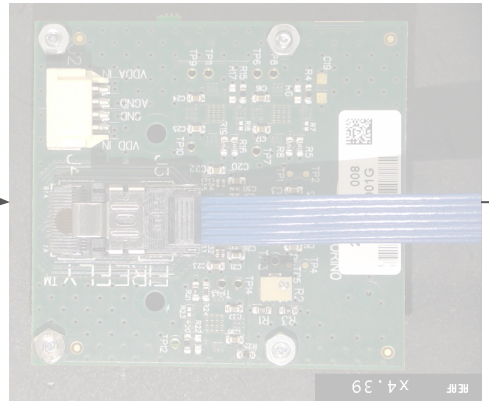


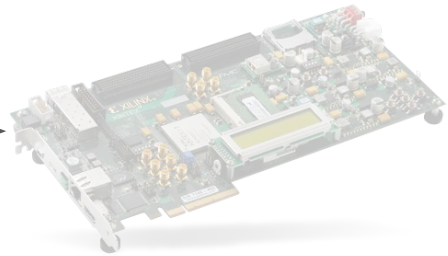
ALCOR FE

FPGA evaluation board

Current scheme adapted







SiPM carrier

temperature sensor must go on the back

resistors and capacitors must go somewhere else

no PCB holes, must have mounting on the back side

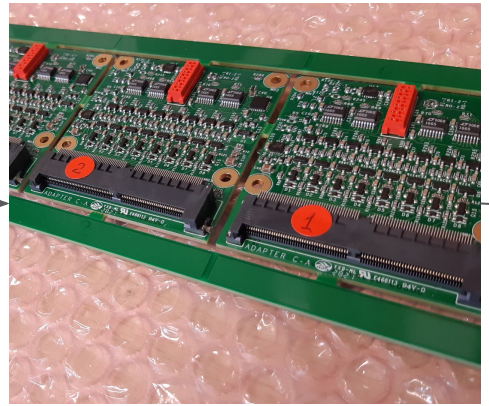
transport Vbias and signals via smart connection (flex)

keep high thermal conductivity of the PCB

keep high-T grade PCB and no plastic for annealing

one carrier will have
- 256 signals
- 32 Vbias lines
- several GNDs lines
- 4 NTC s

Current scheme adapted



we probably do not need DACs for coarse Vbias settings, but it was a nice feature

retain the trimming DACs for fine Vbias settings of single-channel if it fits on the

allow current-induced SiPM annealing (~25 uA / channel)

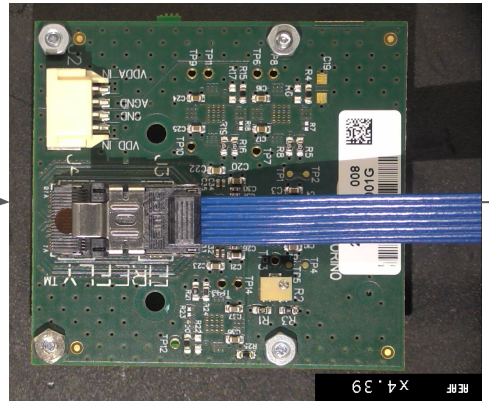
MOSFET to “isolate” downstream circuits (DACs, ALCOR)

LC based filters

one adapter to serve
- 64 channels
- 8 Vbias DACs
- 64 Vtrim DACs

not wider than 40 mm

Current scheme adapted



keep the FireFly connection to FPGA: big, but versatile as allows long cables for beam test

one FireFly cable for each ALCOR chip on board

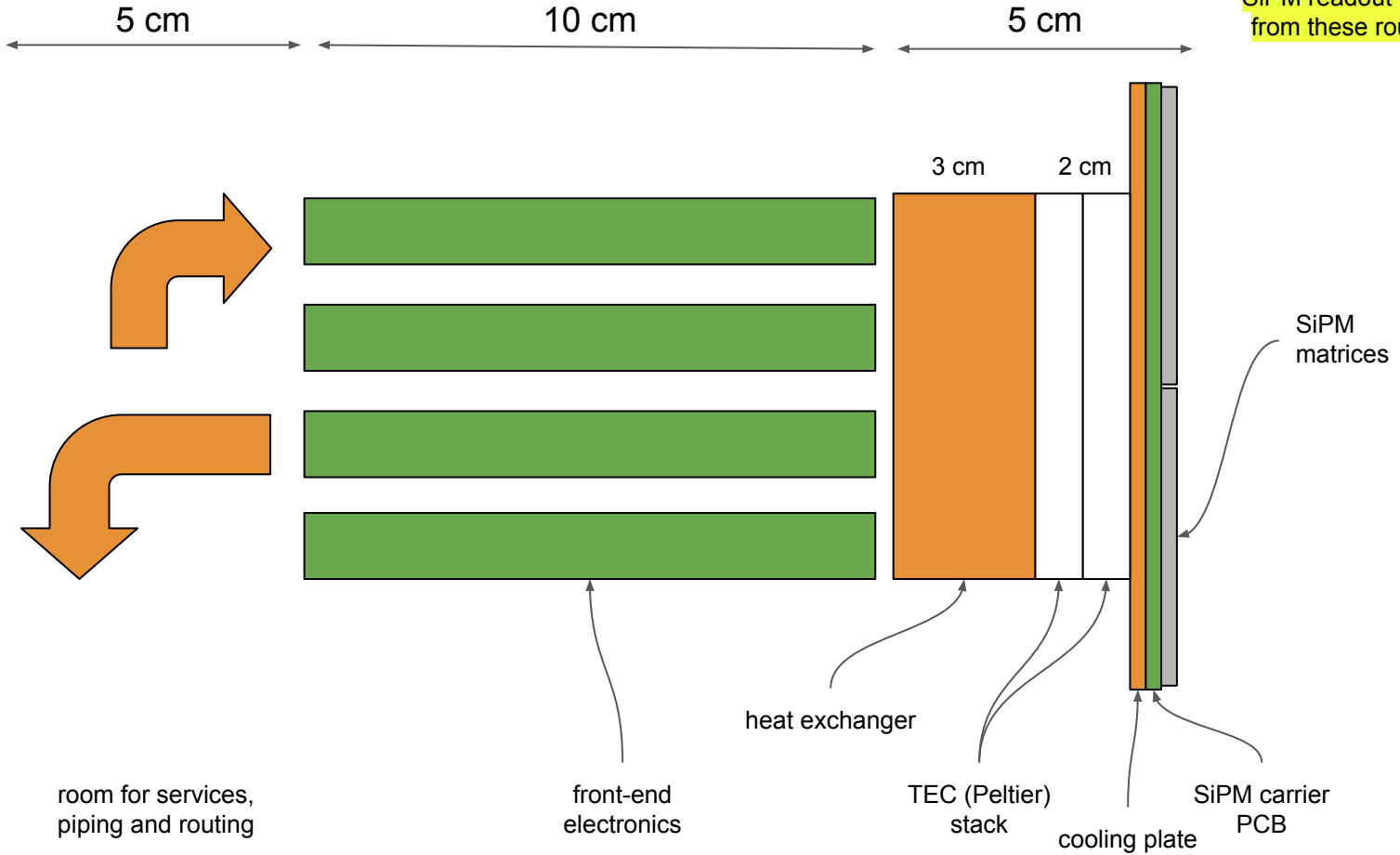
one LV regulator for all chips on board

one FE board to serve
- 64 channels
- mounts 2 ALCOR
- mounts 2 FireFly
- molex connector
- regulators

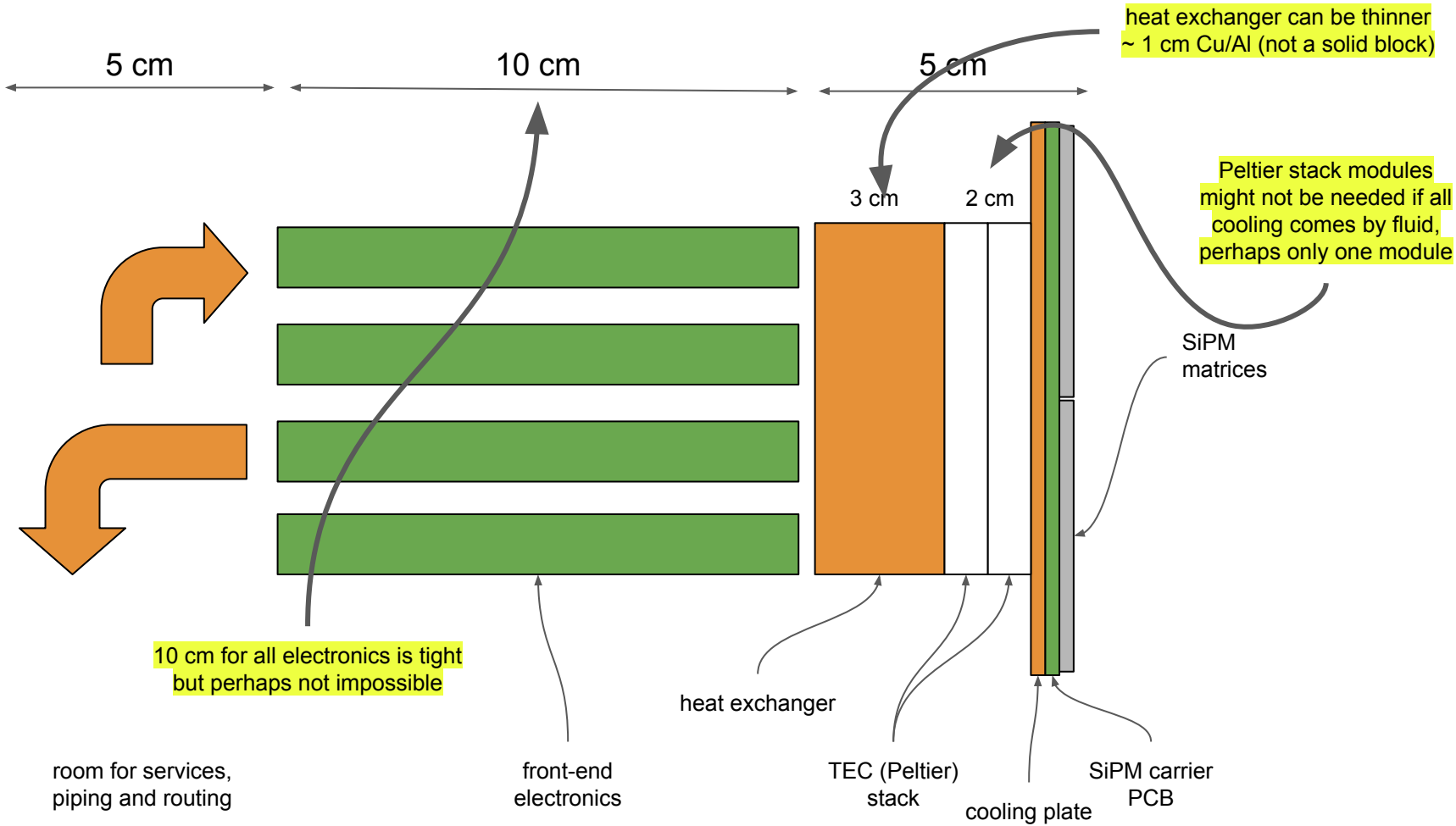
not wider than 40 mm

preliminary design concepts

20 cm longitudinal space for SiPM readout module comes from these rough estimates

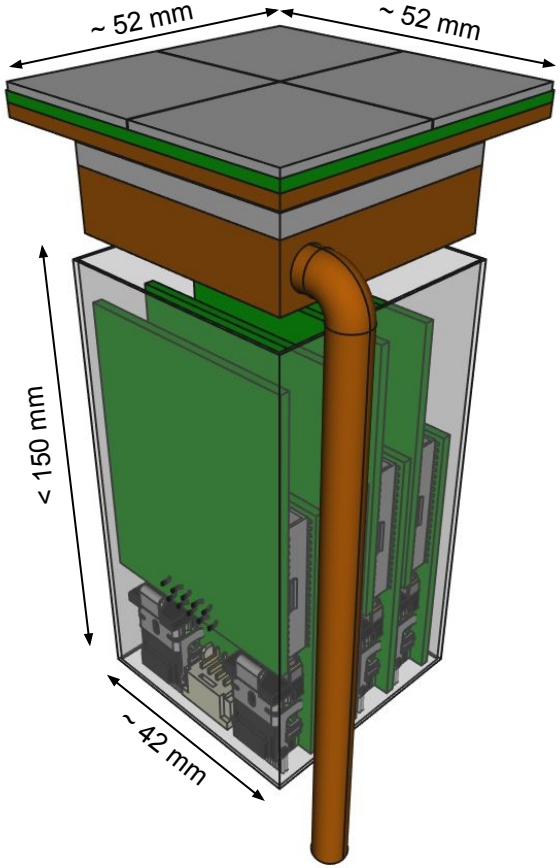


From GDI presentation on 24 October 2022: "Status of SiPM photosensor technology"



From GDI presentation on 24 October 2022: [“Status of SiPM photosensor technology”]

dRICH SiPM optical readout unit (prototype)



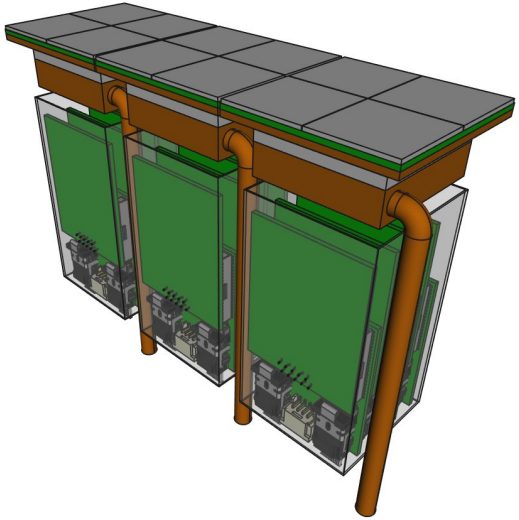
initial design concept

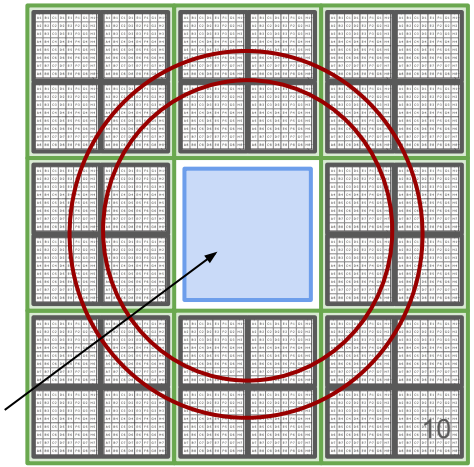
concept developed for the dRICH prototype

electronics engineers working on implementation of the electronics

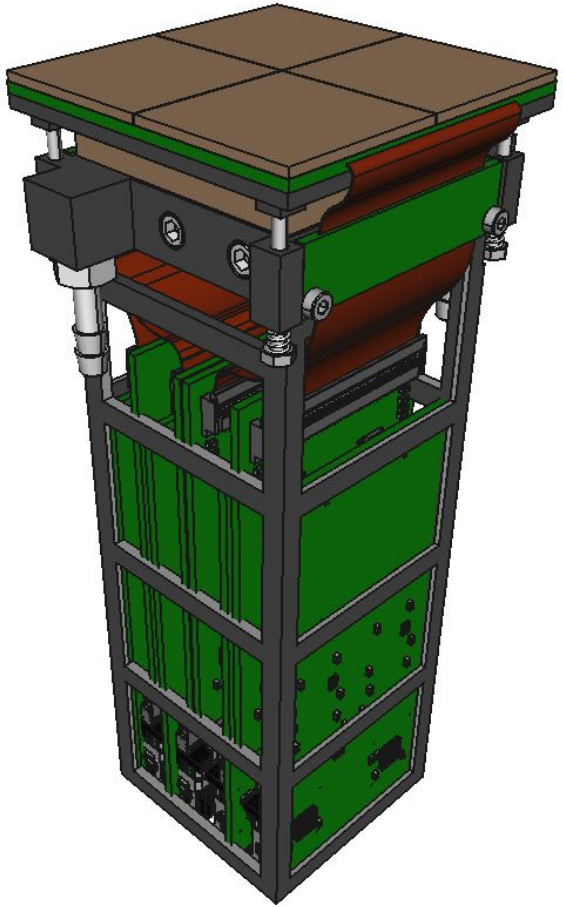
mechanical design will progress with the help of mechanical engineers

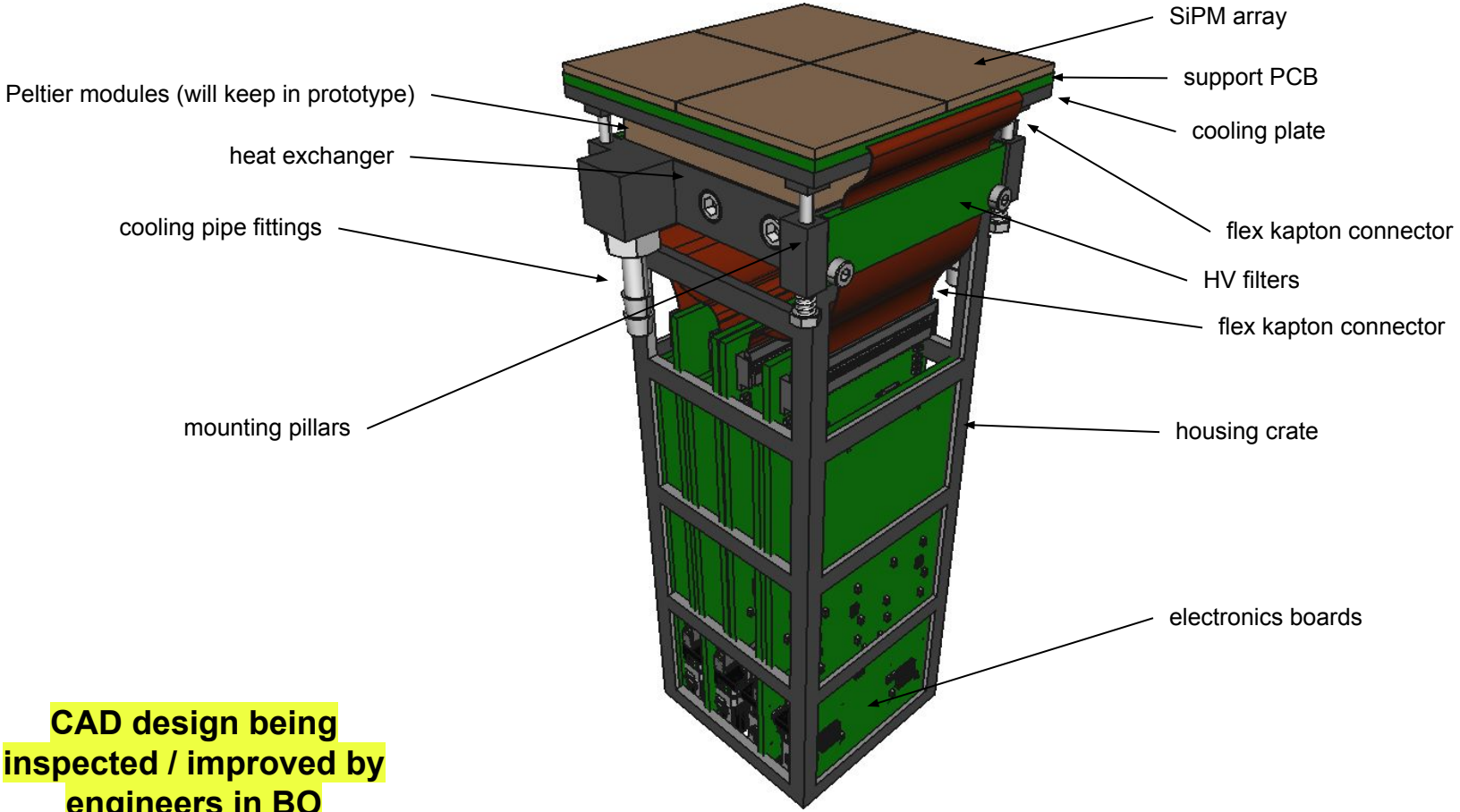
arrangement in beam test 2023





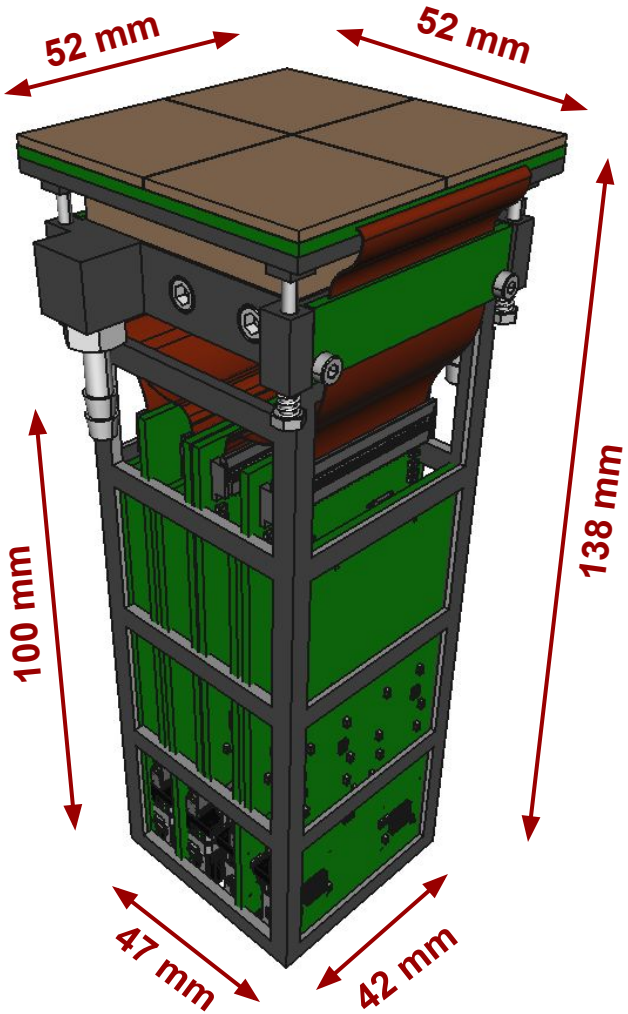
current status





CAD design being inspected / improved by engineers in BO

advanced design concept

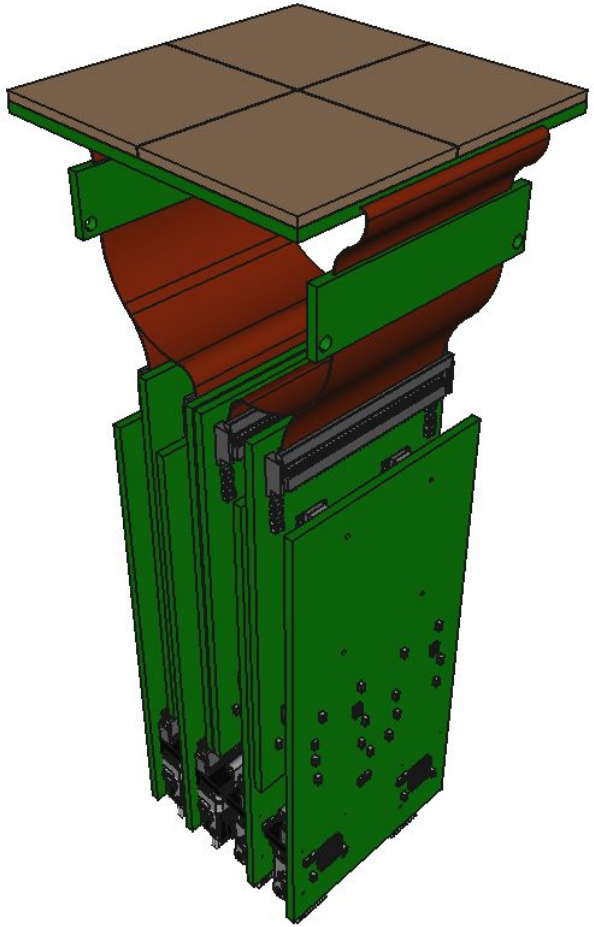


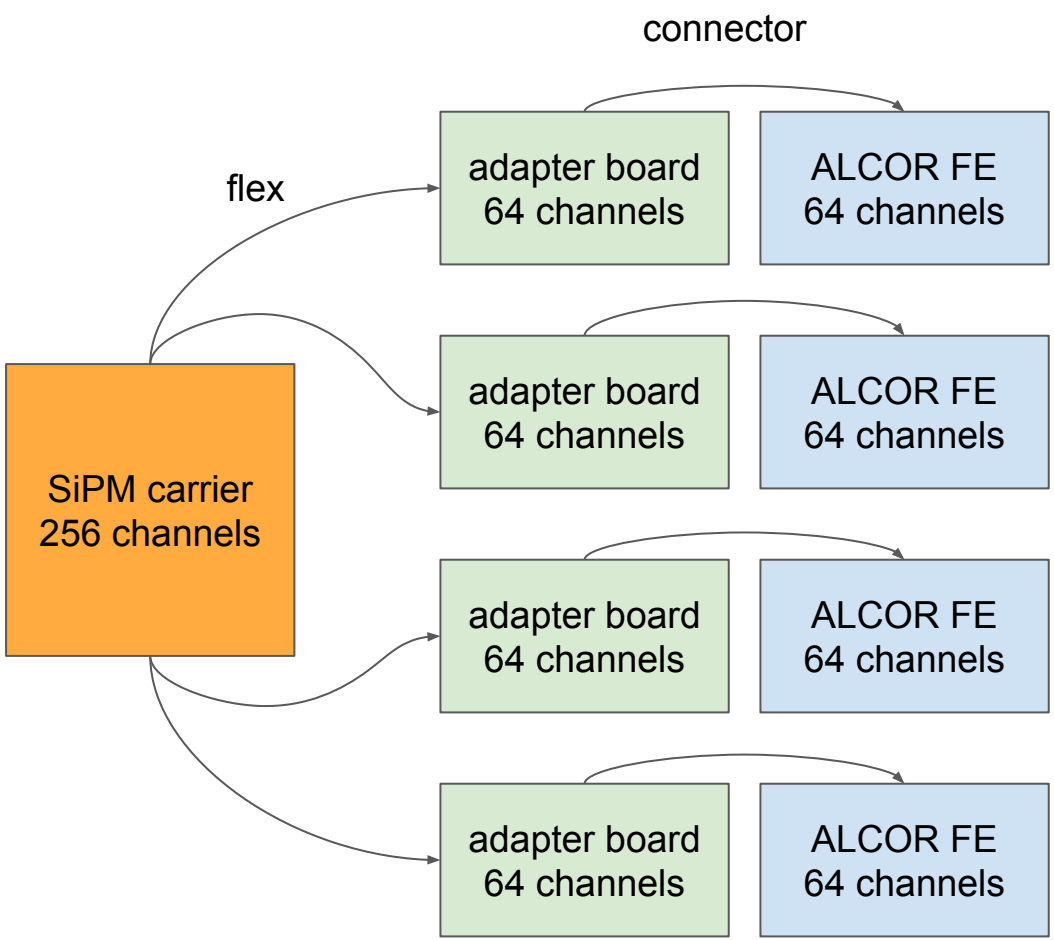
dimensions might slightly change

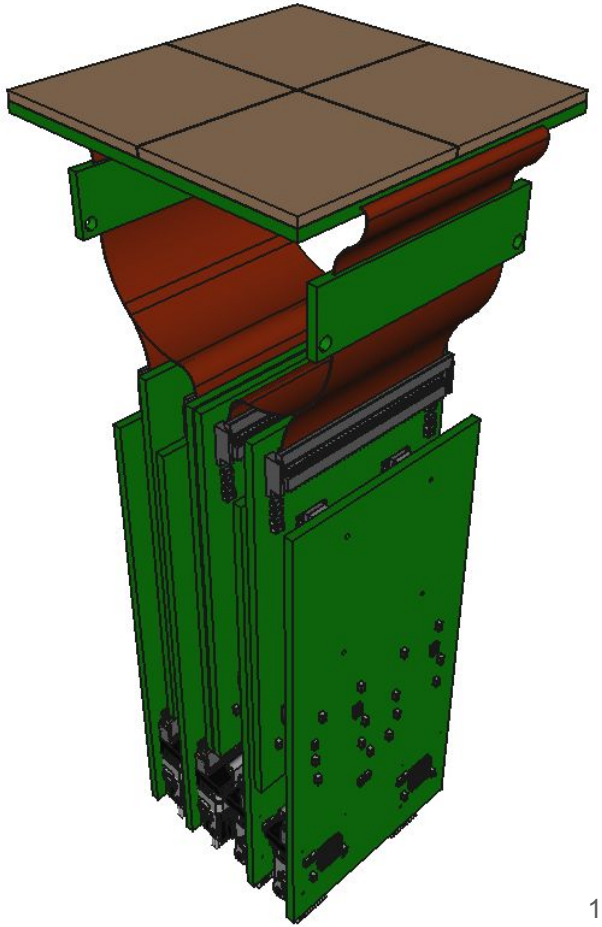
outstanding job to keep electronics within very small envelope

advanced design concept

electronics




connector
flex
SiPM carrier
256 channels
adapter board
64 channels
ALCOR FE
64 channels
adapter board
64 channels
ALCOR FE
64 channels
adapter board
64 channels
ALCOR FE
64 channels
adapter board
64 channels
ALCOR FE
64 channels

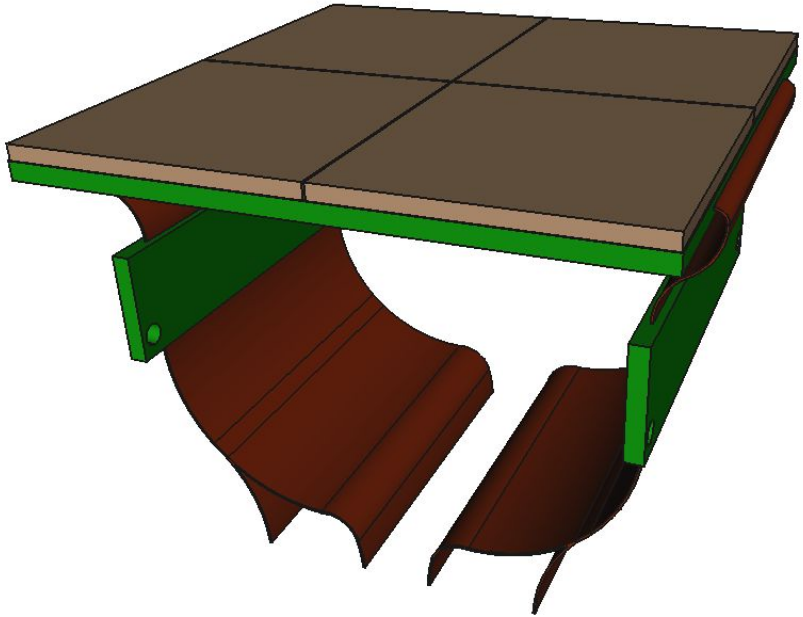


Carrier board V2

advanced stage

mounts 4x SiPM sensor matrices (256 total channels)
receives HV and sends signals via flex connectors (1 mm bending radius)
PCB-flex-PCB-flex design to host HV RC-filters
back-side temperature sensors for monitor / feedback

designed in Bologna
Casimiro Baldanza



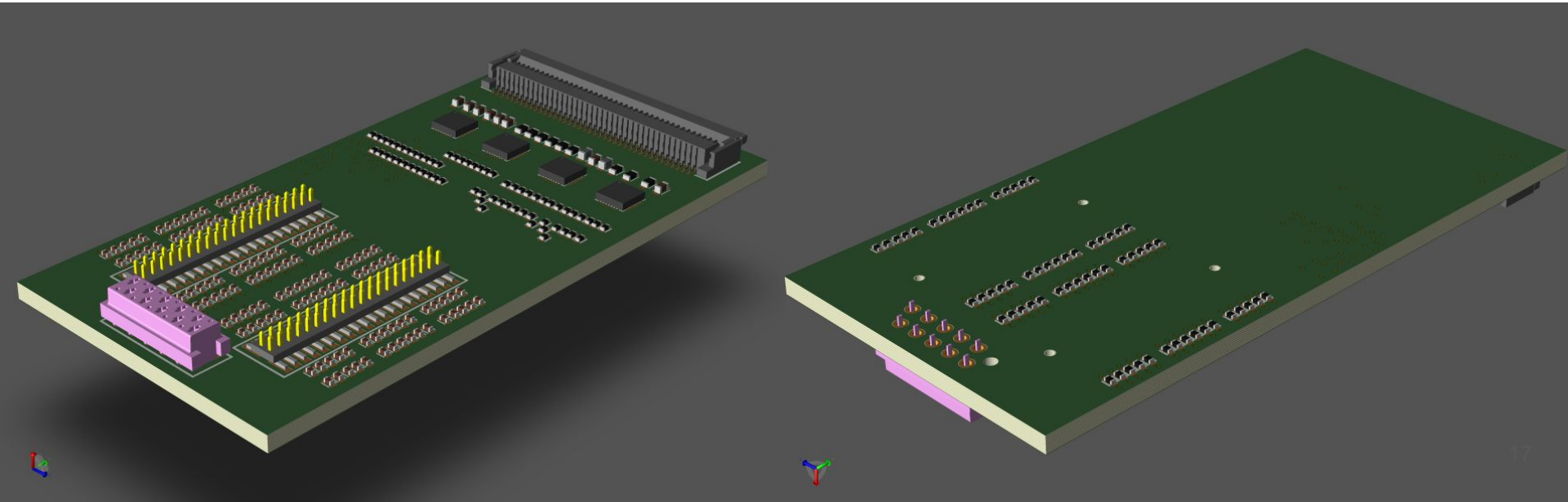
Adapter board V2

project completed
issue order by end Feb

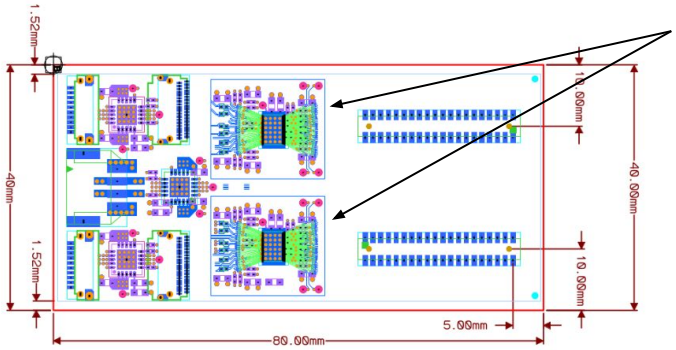
receives signals from SiPM, ships them to ALCOR
includes **complex circuitry** to

- allow HV regulation (0-5 V) for each channel
- derivate signals before ALCOR
- switch from “regular mode” to “annealing mode”

designed in Ferrara
Roberto Malaguti



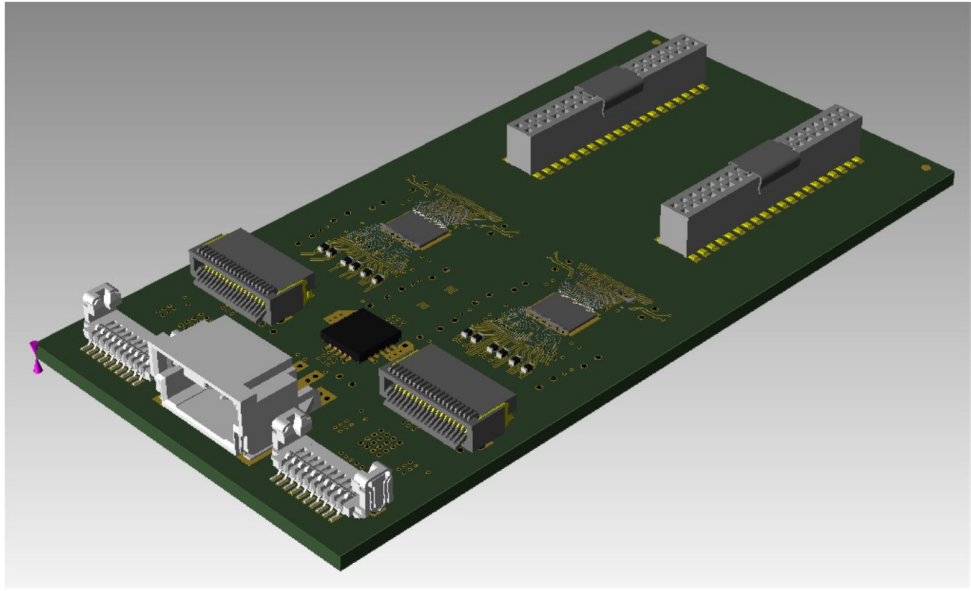
ALCOR board V2

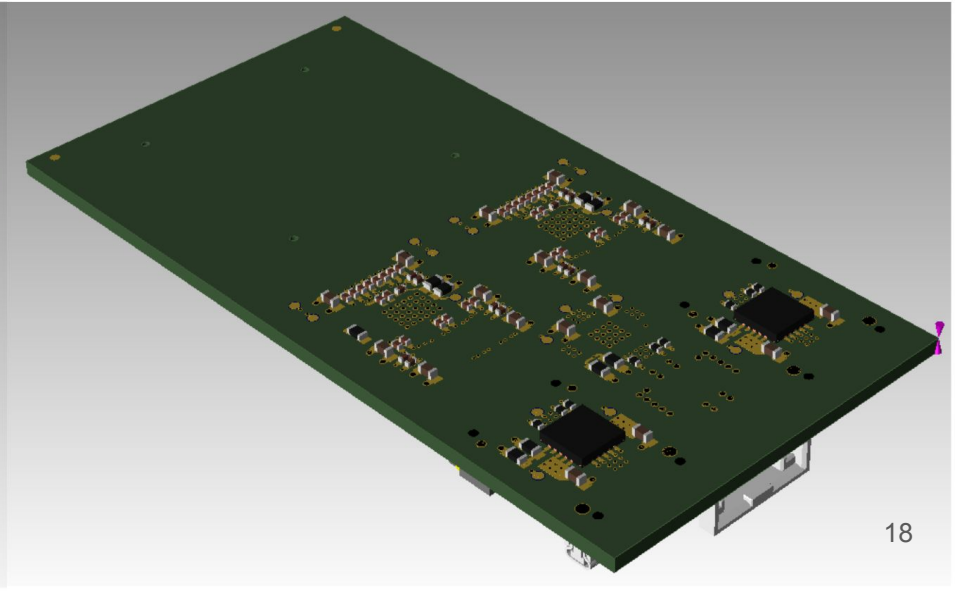


2x ALCOR-v2 ASICs (2x 32 channels)
future ALCOR-v3 will be 64 channels

project completed
issue order by end Feb

designed in Torino
Marco Mignone





Summary

- **design of dRICH prototype SiPM readout**
  - SiPM sensors selected
  - concept idea is mechanically advancing
  - development of new electronics almost completed
  - thank very much Casimiro Baldanza (BO), Roberto Malaguti (FE) and Marco Mignone (TO)
- **number of available ALCORv2 chips drives size of 2023 readout plane**
  - with MPW we can have ~ 50 chips, less than initially expected (thousands)
  - but it is crucial to have few chips in time for testing well before beam tests
  - we will eventually order 30 ALCOR and 30 ADAPTER boards
  - with plans to equip 6 readout units (~ 48 ALCORv2 chips needed + spares)
- **prototype electronics is as compact as it can be in 2023**
  - future developments for a dedicated FPGA board “close to the ASIC”
    - remove FireFly cables, which are nice but connectors are bulky
    - voltage regulators for ALCOR power could be common across multiple chips
  - think about how to integrate ALCOR and ADAPTER board features into a single board
    - perhaps move some features inside ALCOR chip?

SiPM sensors

SiPM sensors for large area dRICH prototype

Roberto Preghenella (INFN Sezione di Bologna)
November 20, 2022

A large-area optical readout surface for the dRICH prototype will be developed as a milestone for the eRD102 project. The readout will be based on modern SiPM photosensors coupled with the ALCOR ASIC [1,2] front-end chip. Hamamatsu S13361-3050 8x8 MPPC arrays [3] with 3mm^2 sensors have been chosen as the reference sensor to instrument the readout surface. In this document we summarise the details of the selection.

https://docs.google.com/document/d/1ld6ECmUsicYPZtr-JJJ5YB7spOVG8kJMT2iWek2L0xw

https://www.hamamatsu.com/content/dam/hamamatsu-photonics/sites/documents/99_SALES_LIBRARY/ssd/s13361-3050_series_kapd1054e.pdf

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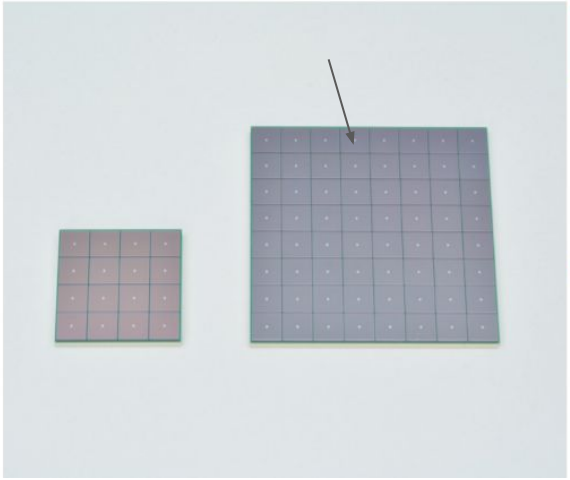
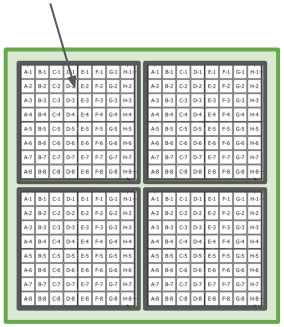


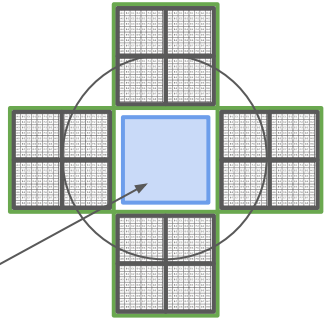
MPPC® (Multi-Pixel Photon Counter) arrays

S13361-3050 series

MPPC arrays in a chip size package miniaturized through the adoption of TSV structure

readout unit:
4 8x8 matrices





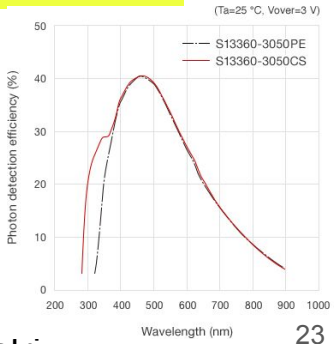
readout area:
4+ readout units
(and spares)

Structure

Parameter	Symbol	S13361-3050NE-04	S13361-3050AE-04	S13361-3050NE-08	S13361-3050AE-08	Unit
Number of channels	-	16 (4 × 4)		64 (8 × 8)		-
Effective photosensitive area/channel	-	3 × 3				mm
Pixel pitch	-	50				μm
Number of pixels/channel	-	3584				-
Fill factor	-	74				%
Package type	-	Surface mount	With connector*1	Surface mount	With connector*1	-
Window	-	Silicone ~~Epoxy~~ resin				-
Refractive index of window material	-	1.55				-

*1: A connector made by SAMTEC is mounted on the back side of the board.
ST4-20-1.00-L-D-P-TR (S13361-3050AE-04)
ST4-40-1.00-L-D-P-TR (S13361-3050AE-08)
These connectors mate with a SAMTEC receptacle (SS4-20-3.00-L-D-K-TR or SS4-40-3.00-L-D-K-TR).
See the following URL for detailed information.
http://www.samtec.com/ftppub/pdf/ss4.pdf

requested silicone resin



we want to have the full surface in contact for optimise the cooling of the matrix

https://www.hamamatsu.com/content/dam/hamamatsu-photonics/sites/documents/99_SALES_LIBRARY/ssd/s14160_s14161_series_kapd1064e.pdf

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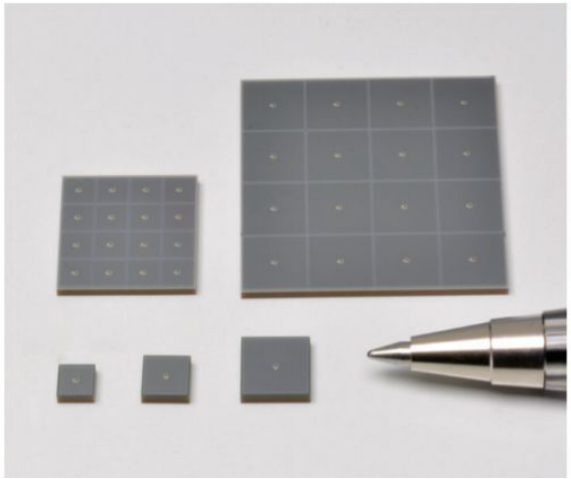


MPPC® (Multi-Pixel Photon Counter)

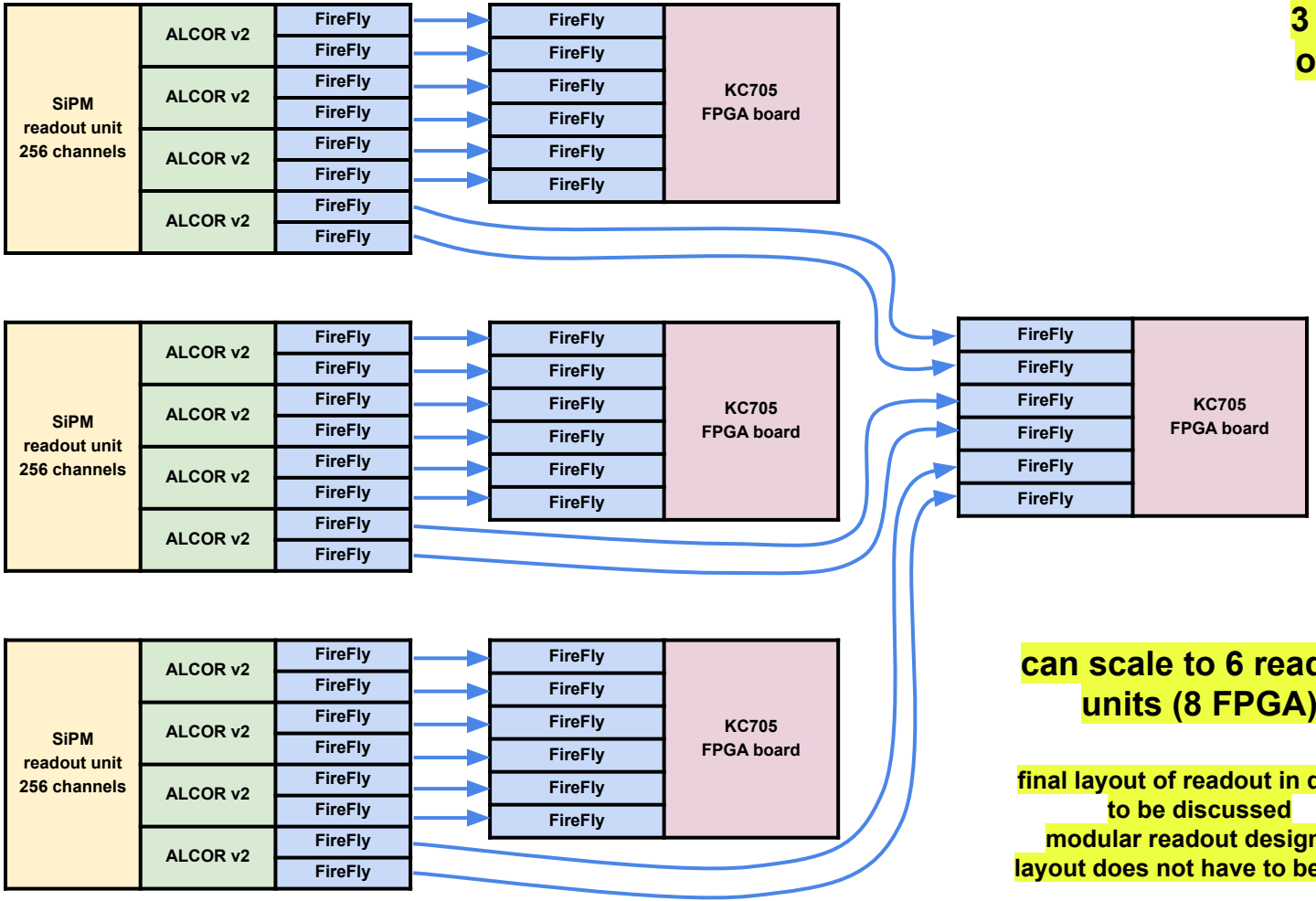
S14160/S14161 series

Low breakdown voltage type MPPC for scintillation detector

Structure

Typ. no.	Number of channels (ch)	Effective photosensitive area/channel (mm^2)	Pixel pitch (μm)	Number of pixels/channel	Package	Window	Window refractive index	Geometrical fill factor (%)
S14160-3050HS	1	3.0 × 3.0	50	3531	Surface mount type	Silicone	1.57	74
S14160-4050HS		4.0 × 4.0		6331				
S14160-6050HS		6.0 × 6.0		14331				
S14161-3050HS-04	16 (4 × 4)	3.0 × 3.0		3531				
→ S14161-3050HS-08	64 (8 × 8)	3.0 × 3.0		3531				
S14161-4050HS-06	36 (6 × 6)	4.0 × 4.0		6331				
S14161-6050HS-04	16 (4 × 4)	6.0 × 6.0		14331				

series 14 is also available in 8x8 matrices, same form factor and landing pattern: cheaper sensors with higher PDE (but higher DCR)
make few readout units based on this technology for comparison



3 readout units readout out by 4 KC705 boards

Xilinx Kintex 5 FPGA evaluation boards

can scale to 6 readout units (8 FPGA)

final layout of readout in dRICH to be discussed
modular readout design ⇒ layout does not have to be fixed