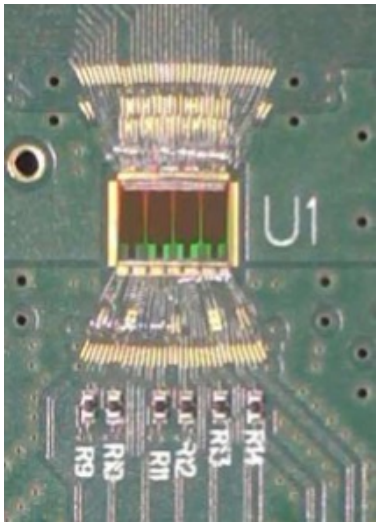
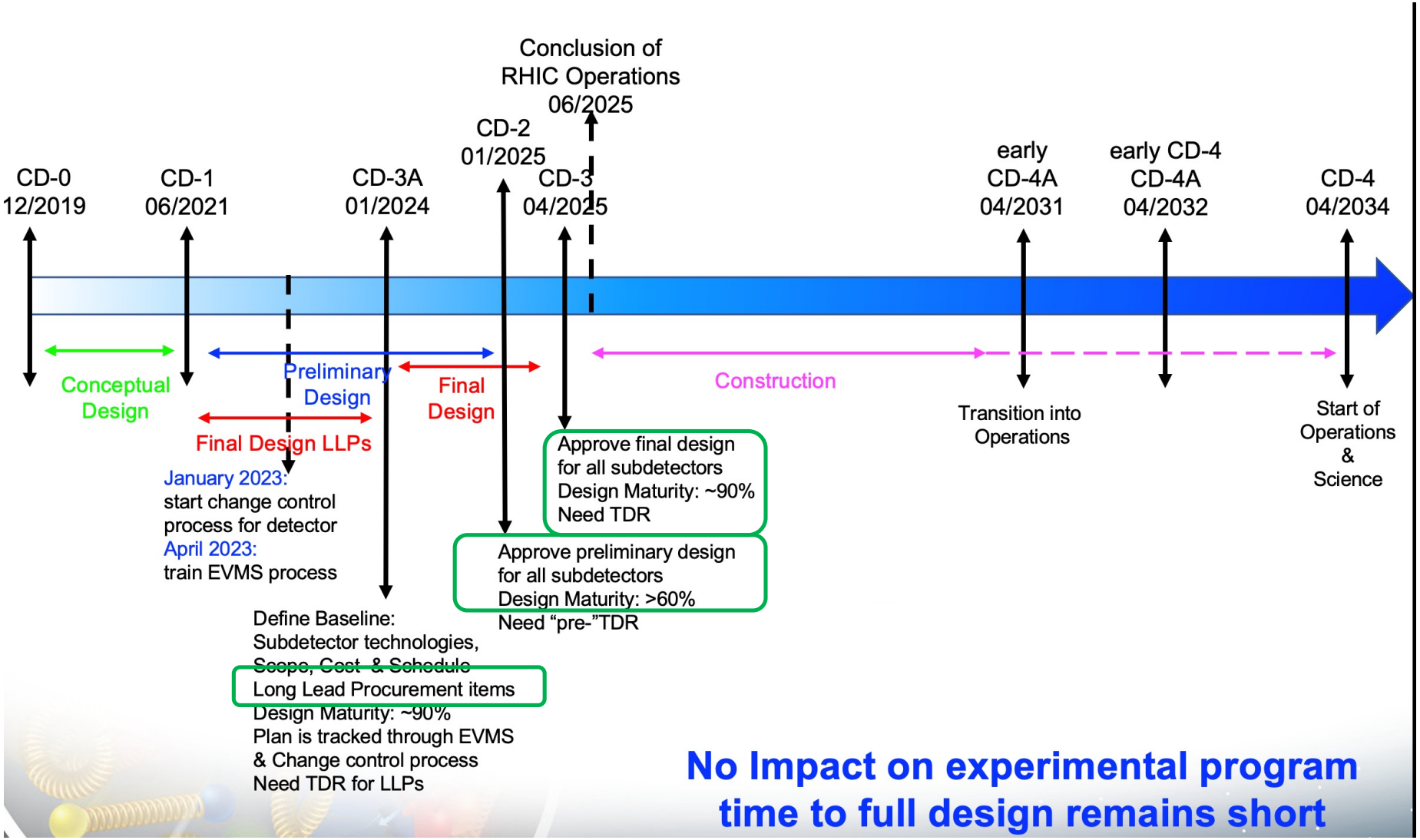


"ALCOR for EIC" day
Introduction

ePIC status, schedule, impact on ALCOR

ePIC

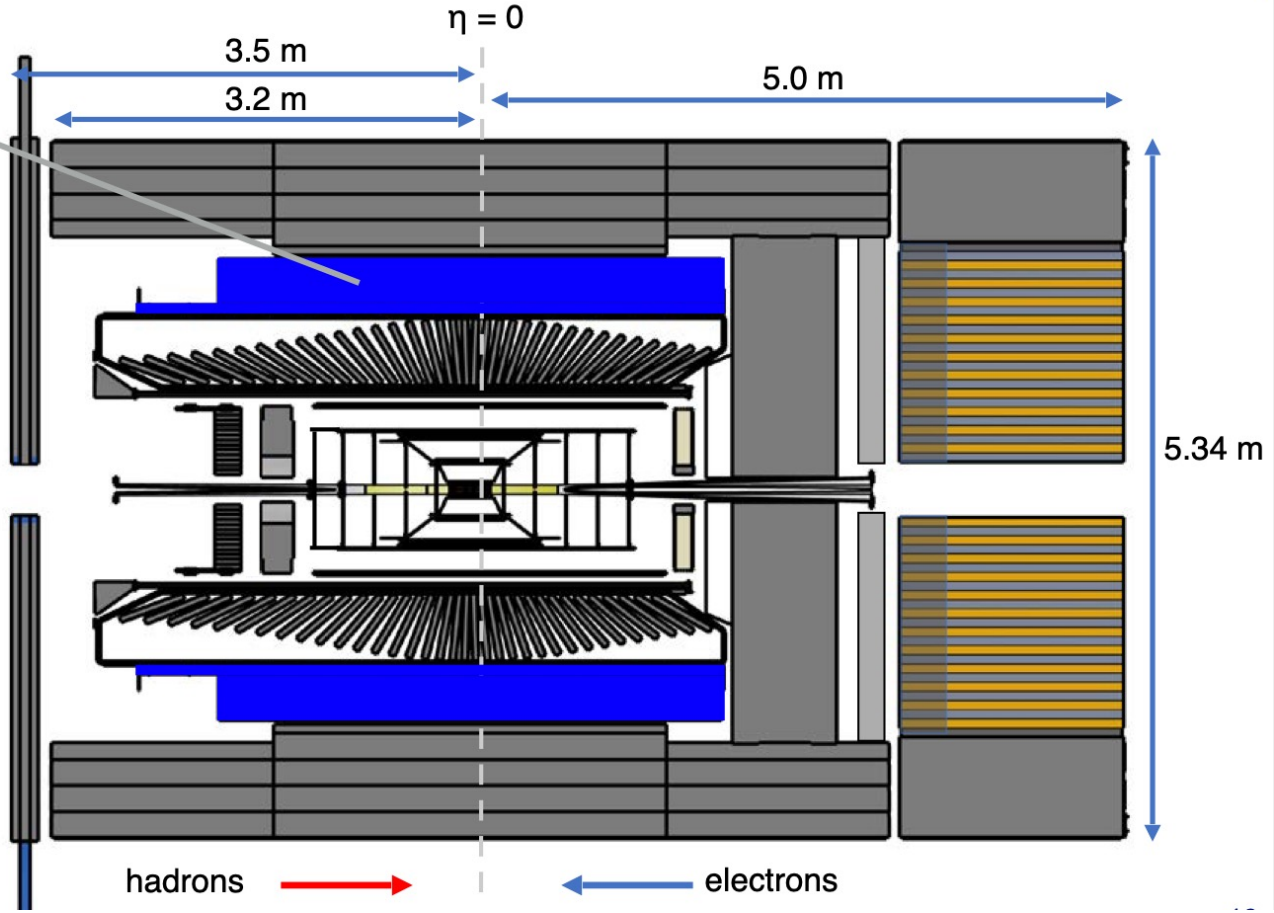
EIC timeline: 8 years and 2 months from starting oprerations



EPIC - Baseline Design

Magnet

- New 1.7 T SC solenoid



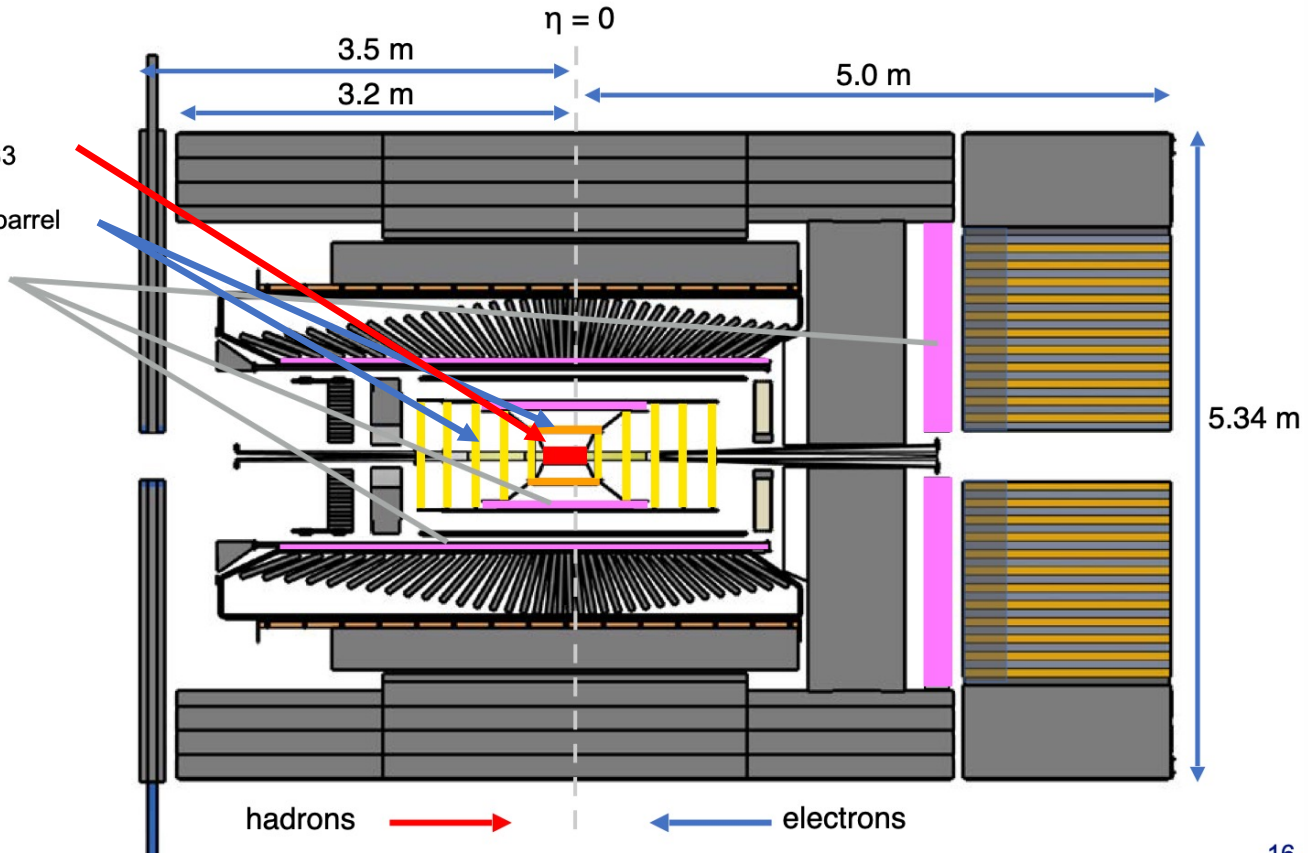
EPIC - Baseline Design

Magnet

- New 1.7 T SC solenoid

Tracking

- Si Vertex Tracker MAPS/ITS3 wafer-level stitched sensors
- Si Tracker MAPS/ITS3/EIC barrel and disks
- MPGDs (μRWELL/MMG) cylindrical and planar



EPIC - Baseline Design

Magnet
- New 1.7 T SC solenoid

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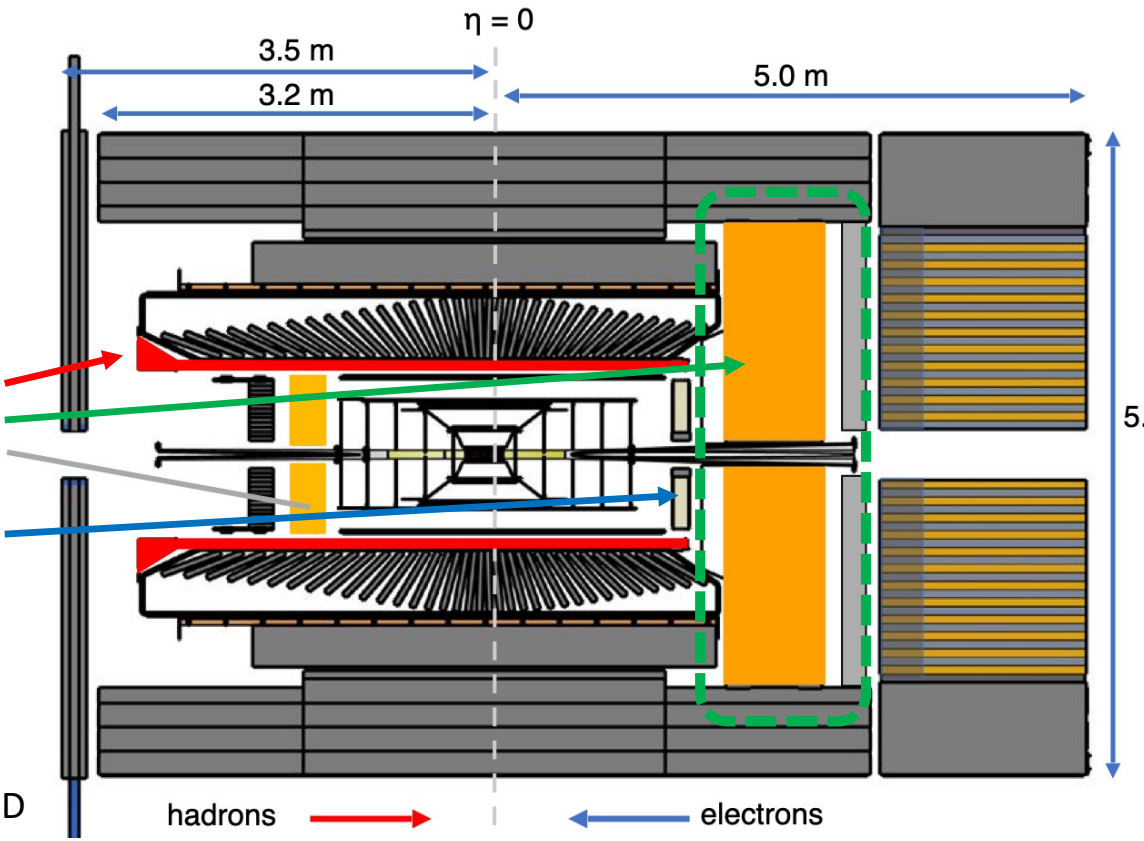
- Si Vertex Tracker MAPS/ITS3 wafer-level stitched sensors
- Si Tracker MAPS/ITS3/EIC barrel and disks
- MPGDs (μRWELL/MMG) cylindrical and planar

PID
- high performance DIRC (hpDIRC)
- dual RICH (aerogel + gaseous)
- aerogel RICH/modular w/ Fresnel **or** proximity focussing RICH
- ToF using AC-LGAD

nota su FAST



per dRICH:
317440 canali O (3 m2)
3x3 mm^2 pzel

315000 canali →
~5000 ALCOR 64ch

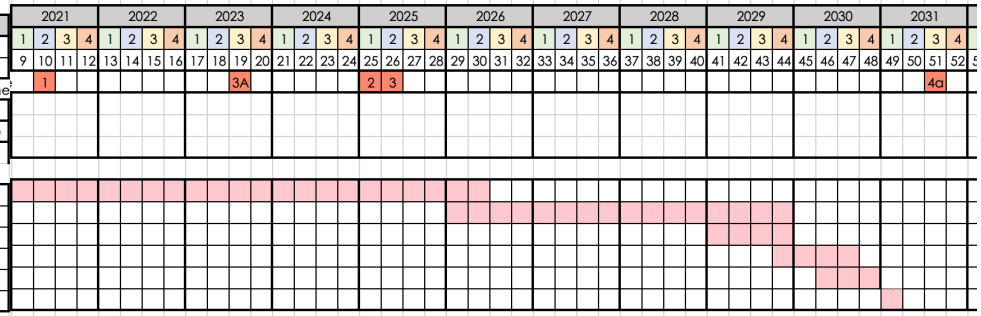
Per backward RICH e' stata scelta tecnologia LAPPD (nota su ALCOR)

dRICH schedule (adapted from ATHENA, shifted of one year)
assumes "in-house" assembly & test in Italy in one year and assembly and test in one year @ BNL + 1 quarter for "insertion"
CAVEAT: note this “primordial” schedule was done really in hurry and limited consultation

Gantt chart: ePIC Detector Sub-System Quarterly Schedule

Starting date	01/01/19
Year:	2019
Quarter:	1

ID	Task	Start Time	Year	Quarter	Start Time nQ	End Time	Year	Quarter	End Time nQ	Duration Q
1	dRICH R&D	01/01/20	2020	1	5	30/06/26	2026	2	30	25
2	dRICH Procurement	01/01/25	2025	1	25	31/12/28	2028	4	40	15
3	dRICH Assembly (In-House)	01/01/28	2028	1	37	31/12/28	2028	4	40	3
4	dRICH Assembly (in-situ)	01/10/28	2028	4	40	30/09/29	2029	3	43	3
5	dRICH Test (in situ)	01/06/29	2029	2	42	31/12/29	2029	4	44	2
6	dRICH Installation	01/01/30	2030	1	45	31/03/30	2030	1	45	0



SiPM targeted for early procurement: some pressure to choose soon the sensor
How ALCOR would fit in this Gantt?

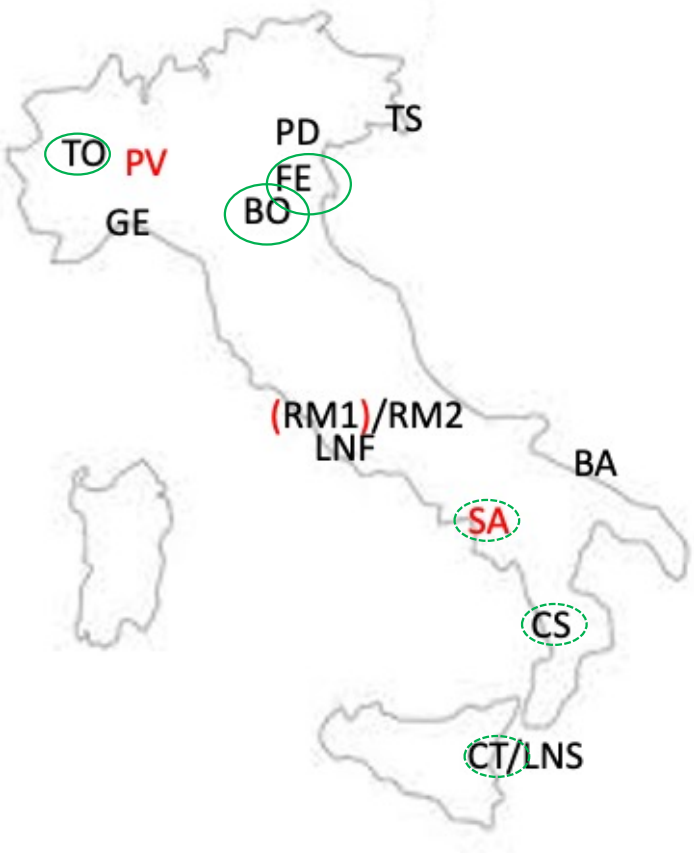
2023: v2 tests
2024: v3 proto (including packaging) + electronics proto?
2025: production? -→ 6000 (packaged/tested....)
2026 is ultimate deadline to define electronics

Who is using/will use ALCOR4EIC?

BO currently coordinating electronics development

TO → ALCOR "card" + ASIC
BO → carrier card
FE → adapter card
BO → readout à la ARCADIA (break-out board)

- setup under developments in SA/CS/CT
- On the long-run potentially "two centers for assembly" ?
- TO-site: natural candidate for ALCOR production & test, “ALCOR” card production, functional test -→
- On the long-run potentially "two centers for assembly" ?
- "portable setup"



- ALCOR used for characterization after irradiation/annealing (in 2022 only at BO, we hope to achieve ”South Cluster” by 2023
- ALCOR used during test beam 2021 (unsuccessfull) and 2022

(quite successfull, "bug" limited – and also noise...)

Relevant eRD projects (DoE funded) and CSN3 planning – relevant milestones for ALCOR

project	topic	FY	
eRD102	dRICH	22	• Realistic implementation of dRICH into the EIC detector (02/23), subject to the release of a common simulation framework, agreed by Detector-1 Collaboration, by 10/22 • Initial assessment based on the first test beams (12/22) • **Realization of a suitable detector plane for the dRICH prototype (03/23)**
eRD110	photosensors	22	• **Automated setup for SiPM characterization in climatic chamber (9/2022)** • **Comparative assessment of commercial (and prototypes not yet available on the market) of SiPM performance after irradiation 2/2023 (interim results available at 9/2022)** • **Definition of an annealing protocol 2/2023**
eRD102	dRICH	23	• Initial characterization of realistic mirror and aerogel components (04/23) • Projected performance of the baseline detector as integrated into EPIC (06/23) • **Assessment of the dRICH prototype performance with the EIC-driven detection plane (10/23).**
eRD109	ASIC	23	• **Inhibit paradigm studies on ALCOR v1: 1/2023** • **Qualification of ALCOR v2: 7/2023** • **Results above presented for the draft TDR of EIC Detector 1: 9/2023** • **Design of ALCOR v3: 9/2023**
eRD110	photosensors	23	• **Timing measurement of irradiated (and annealed) sensors [6/23]** • **Comparison of the results achieved with proton and neutron irradiation sources [8/23]** • **Study of annealing in-situ technique with a proposed model selected as baseline for the draft Technical Design Report (TDR) [9/23]**

Non potevamo piu' aspettare quindi siamo andati con MWP (solo 50 ALCOR v2) ma ora "finestra engineering run" (in 2023)

Milestones Concordate

Data	Descrizione
31-07-2023	Sottomissione su rivista di risultati ottenuti in campagna di irraggiamento SiPM
30-11-2023	Realizzazione di una ampia superficie di rivelatori SiPM per la lettura ottica del prototipo dRICH basata su readout ALCOR.
31-12-2023	Presentazione schema di ottimizzazione delle dimensioni dei sensori CMOS 65 nm stitched per EPIC tracker sulla base della resa di produzione da ER1 ITS3
31-12-2023	Contributo a simulazioni Detector 1 (in particolare per Si-Vertex e dRICH) per pre-TDR Detector 1
31-12-2023	Contributo a studi di physics performance per Detector-1 nei canali esclusivi attraverso EpIC generator
31-12-2023	Organizzazione giornate nazionali EIC
31-12-2023	Misura in campo magnetico delle performance di prototipo LAPPD.

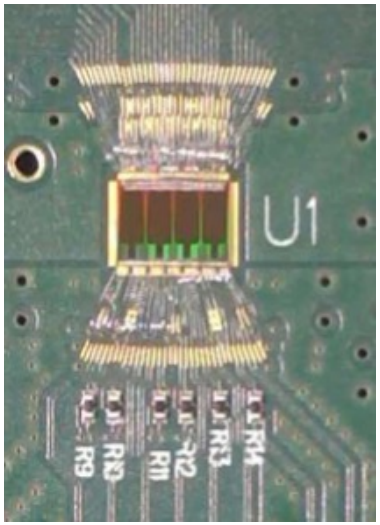
Punti per discussione / "desiderata" / requirements / misure da fare per ALCOR

2023 e' anno in cui si presenta piano finanziario a INFN per ePIC (a luglio 2023) e draft TDR (ottobre 2023):

→ stima costi

→ planning Gannt

Non potevamo piu' aspettare LNGS quindi siamo andati con MWP
(solo 50 ALCOR v2) pero' ora "finestra engineering run" (in 2023) che fare?
Parte discussione oggi



"ALCOR for EIC" day

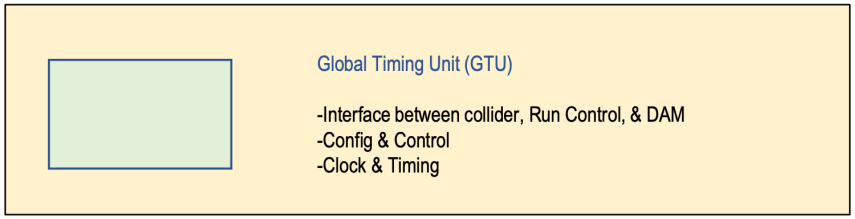
requirements/constraints for ALCOR:

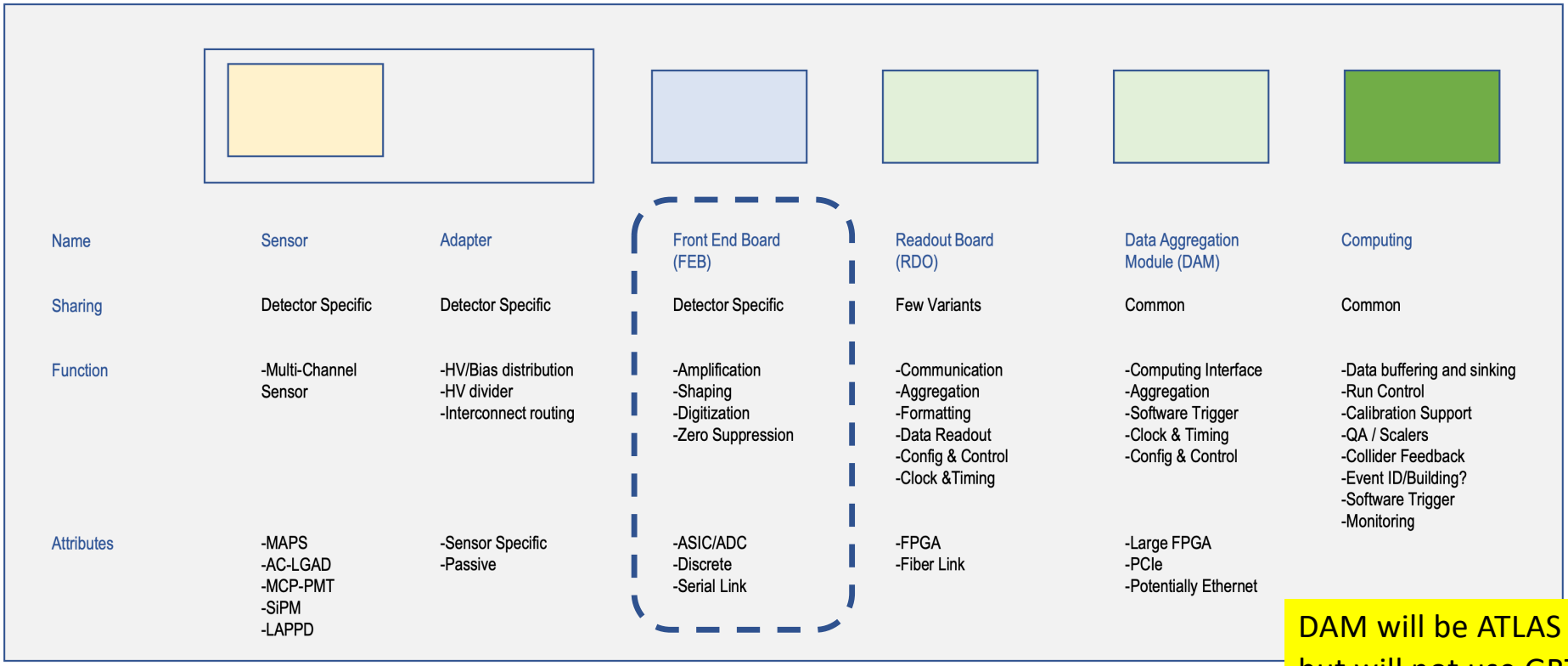
ePIC DAQ, dRICH DAQ, DCR, throughput

ePIC

EPIC Electronics / DAQ

Standard Component Names and Functions





Name	Sensor	Adapter	Front End Board (FEB)	Readout Board (RDO)	Data Aggregation Module (DAM)	Computing
Sharing	Detector Specific	Detector Specific	Detector Specific	Few Variants	Common	Common
Function	-Multi-Channel Sensor	-HV/Bias distribution -HV divider -Interconnect routing	-Amplification -Shaping -Digitization -Zero Suppression	-Communication -Aggregation -Formatting -Data Readout -Config & Control -Clock &Timing	-Computing Interface -Aggregation -Software Trigger -Clock & Timing -Config & Control	-Data buffering and sinking -Run Control -Calibration Support -QA / Scalers -Collider Feedback -Event ID/Building? -Software Trigger -Monitoring
Attributes	-MAPS -AC-LGAD -MCP-PMT -SiPM -LAPPD	-Sensor Specific -Passive	-ASIC/ADC -Discrete -Serial Link	-FPGA -Fiber Link	-Large FPGA -PCIe -Potentially Ethernet	

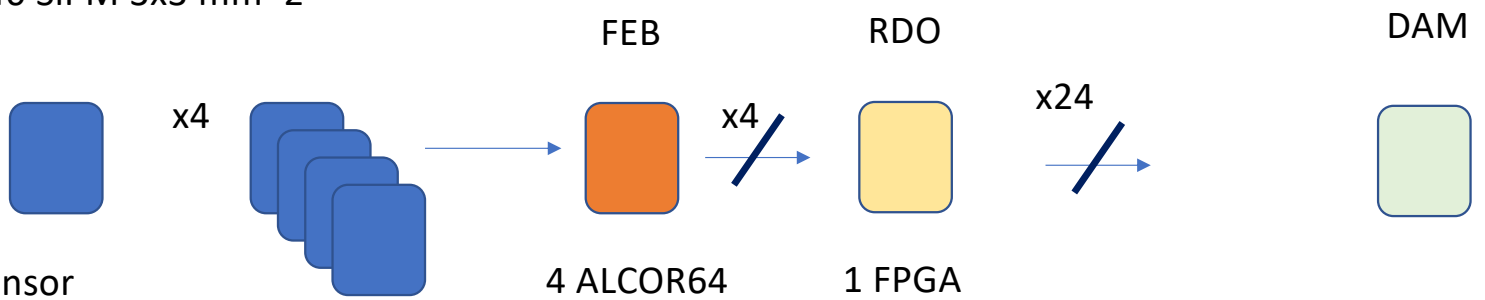
DAM will be ATLAS Felix card but will not use GBT link

“standard” but triggerless: continuous (streaming) readout à la ALICE/LHCb

How would fit ALCOR in dRICH readout?

"current" scheme (need to make budgeting for ATHENA proposal, this year this has to be reviewed)

317440 SiPM 3x3 mm^2



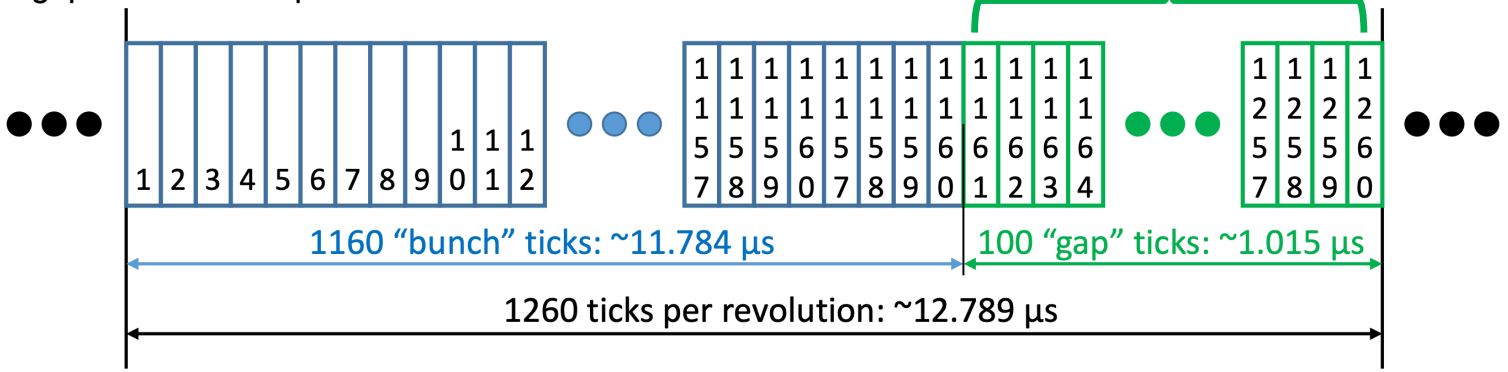
See Roberto's talk: prototype electronics for 2023 keeps in mind ALCOR v2 + different aggregation: learning exercise

Beam structure and bunch crossing timing

- Beam structure repeats every ~12.7886 μs
  - → Revolution frequency: ~78.195 kHz
- There are 1260 clock ticks in each revolution
  - → Clock period: ~10.14968 ns
    - Frequency: ~98.52525 MHz
  - → 1160 "bunch" ticks *approximately* marking *potentially* active intervals with particles
    - *Approximately*: electron beam structure is much more stable compared to hadron beam structure
    - *Potentially*: there can be 290 or 1160 active bunches with particles
  - → 100 "gap" ticks without particles

Sep 8, 22

Here we need to enable ALCOR inhibit for sure!



- Assume a stable clock can be derived from Machine with this frequency despite of bunch time variations
  - → This clock or its (sub)multiples is distributed to frontend electronics as "System clock"
    - With bunch-phase recovery mechanism
    - Used for bunch level synchronization, coarse timestamp bookkeeping, serial communication and possibly timing measurements.

EIC clock 98.52 MHz → candidate clock for ALCOR: 295.56 MHz **(or 394.08 MHz)**

Coarse bin: 3.38 ns (or 2.54 ns)

dRICH estimates of throughput (ATEHENA)

Table 2.5: Maximum data volume by detector.

Detector	Channels	DAQ Input (Gbps)	DAQ Output (Gbps)
B0 Si	400M	<1	<1
B0 AC-LGAD	500k	<1	<1
RP+OMD+ZDC	700k	<1	<1
FB Cal	4k	80	1
ECal	34k	5	5
HCal	39k	5.5	5.5
Imaging bECal	619M	4	4
Si Tracking	60B	5	5
Micromegas Tracking	66k	2.6	.6
GEM Tracking	28k	2.4	.5
μRWELL Tracking	50k	2.4	.5
dRICH	300k	1830	14
pfRICH	225k	1380	12
DIRC	100k	11	11
TOF	332k	3	.8
Total		3334	62.9

ASSUMPTIONS

This was computed assuming an average 270 kHz DCR per pixel MAX before moving to annealing cycles given limitations on ALCOR and DAQ bandwidth

We considered already a factor 3 reduction due to timing selection (it might be 5 or 10…) [at the time of proposal it was ambiguous if It was at ALCOR or FPGA level]

Throughput assumed 64 bit per hit (TOT)

Throughput (I)

- ALCOR clock 320 MHz ma dati serializzati a frequenza DDR a gruppi di 8 canali → le parole di 32 bit sono encoded a 40 bit
- Questo porta a un limite massimo di 640 Mb/s che corrisponde a un nassimo rate su 8 canali di 16 MHz → quindi siamo ora limitati a 2 MHz su singolo canale (averaged su 8)

Starting to play with numbers and known limitations:

- Below no TOT
- Note that 10 Gbps limitation might be overcome (20 Gbps seems reachable even if rad. Tol. might be problem) to be investigated ---→ current target link at **14 Gbps** (DAQ subwg where Pietro/Davide are involved) target FPGA: Xilinx Artix Ultrascale++ or Microchip Polarfire
- Exploit timing reduction

Singolo canale	serializer 8 canali ALCOR column	8 ch → ALCOR-64	FPGA (16 ALCOR-64).	Timing reduction	Opt Link
5 MHz	**16 MHz** → **2 MHz**	64 MB/s. → 512 MB/s	8 GB/s → 64 Gbps	1	10 Gbps
300 kHz	300 kHz	9,6 MB/s. → 76,8 MB/s	1,2 GB/s → 9,8 Gbps	1	10 Gbps
300 kHz	300 kHz	9,6 MB/s. → 76,8 MB/s	1,2 GB/s → 9,8 Gbps	3	**3,3 Gbps**

Throughput (II)

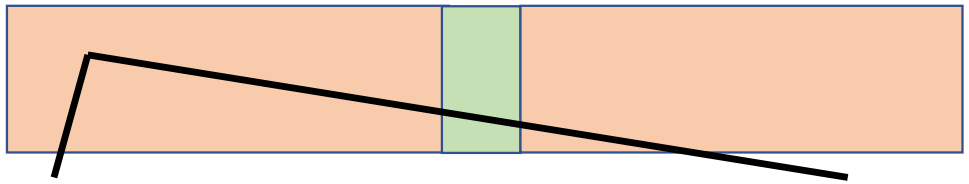
ALCOR test pulse (in inverse polarity) can act as “inhibit” of the digitalization. This could help greatly to reduce data throughput
Note EIC beam bunch timing presentation by Todd (Sep. 2022)

Short summary:

EIC Orbit	**12.78 usec**
Bunch spacing (Nb 290)	40.599 ns
Bunch spacing (Nb 1160)	10.150 ns
Gap length	1.01 usec
Collision spread (bunch length)	23-30 ps (ESR) 250-200 (ps) HSR

Notes:

- we will need to implement disable during gap region which is sizeable (8% data reduction ‘for free”)
- Bunch crossing every 10 ns! With a bunch length of 250 ps if we could select just 1 ns data reduction by a factor 10 before serializing stage in ALCOR



Critical measurement to be done in Turin:

- How react ALCOR to such “short” shutter cycles?
- What happens to the TOT measurement?
- What happens if trailing edge is ON and leading edge was OFF

See Giulio’s talk today

Note LHCb is thinking something very similar with FastRich

If it works then requirement on precise clock alignment / phase shift inside FPGA sending shutter to ALCORs

Throughput (III)

Singolo canale	serializer 8 canali ALCOR column				
	16 MHz	8 ch → ALCOR-64	FPGA (16 ALCOR-64). Timing reduction		Opt Link
5 MHz	**2 MHz**	64 MB/s. → 512 MB/s	8 GB/s → 64 Gbps	1	10 Gbps
300 kHz	300 kHz	9,6 MB/s. → 76,8 MB/s	1,2 GB/s → 9,8 Gbps	1	10 Gbps
300 kHz	300 kHz	9,6 MB/s. → 76,8 MB/s	1,2 GB/s → 9,8 Gbps	3	**3,3 Gbps**
5 MHz	500 kHz	16 MB/s. → 64 MB/s	1,0 GB/s → 8 Gbps	1/0.92	**7,4 Gbps**

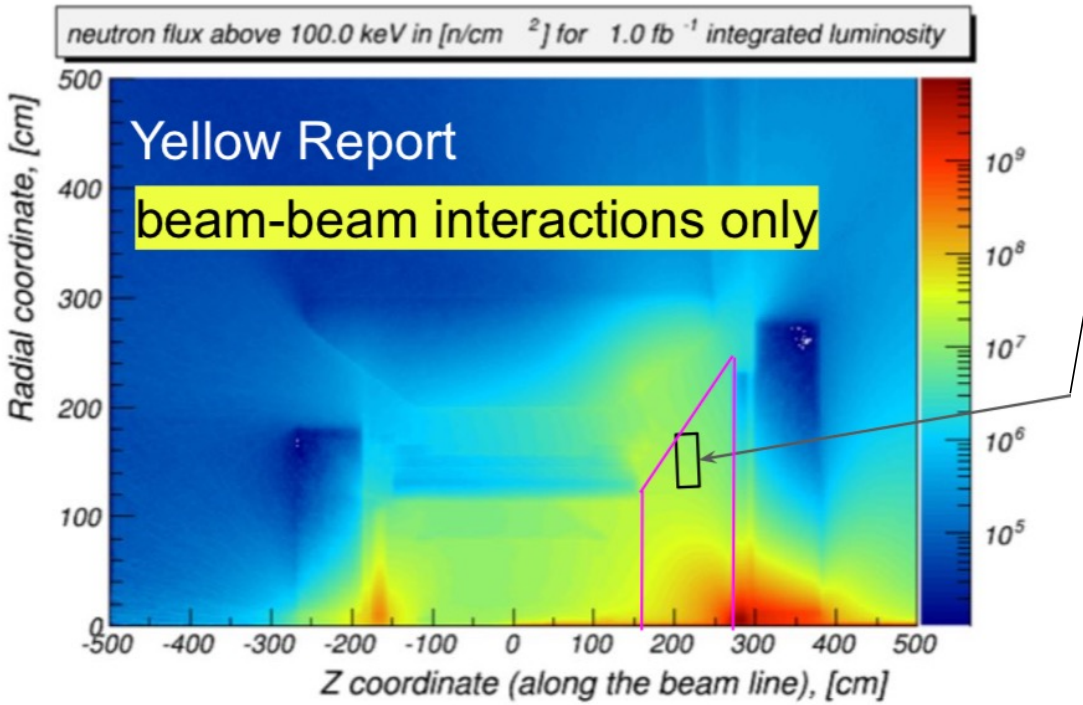
Hardware shutter reduces by factor 10

Orbit gap

The implementation of the shutter might reduce annealing cycles by a factor 10
Question for ASIC experts: will it really work this way?
Question for ALL: we will might have in 1 ns a 5 MHz DCR but… we will then still see the rings?
→ simulation with flat noise is a must!!

Work underway in TS-SA+Duke on noise → RM2/GE

How much radiation? (the usual plot)



potential location of photosensors:
≈ **1-5 10^7 n/cm^2 every 1 fb^{-1}**

10^{11} n/cm^2 1-MeV n_{eq} is a ”true maximum”

- 30 weeks @ 10^{34} cm^{-2} s^{-1}= 100 fb^{-1} → 1-5 10^9 n/cm^2
- 10^{11} n/cm^2 would be reached in O(10+) years at full $\mathcal{L}$!

A moderately hostile environment:
10^9 1-MeV n_{eq}/cm^2 → most of the key physics topics
10^{10} 1-MeV n_{eq}/cm^2 → GPD and more statistically eager topics
10^{11} 1-MeV n_{eq}/cm^2 → may be we will never go here…

Can we use SiPM for a Cherenkov detector up to 10^{11} 1-MeV n_{eq} /cm^2 fluence?

Radiation is finally computed in ePIC

Finally with ePIC geometry

Best thing we had in the past (ATHENA)

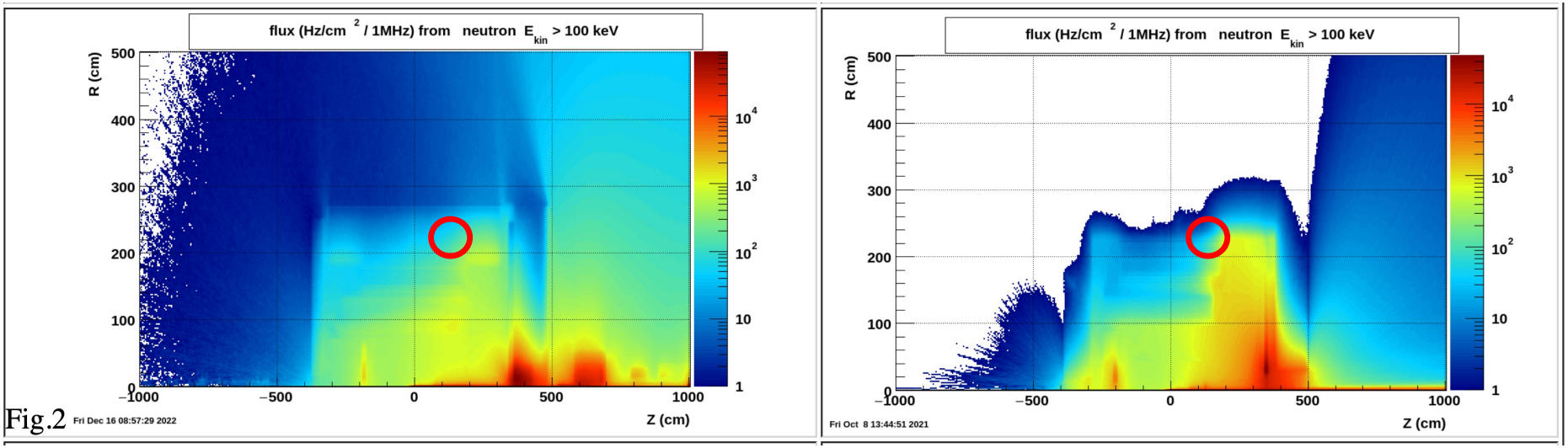


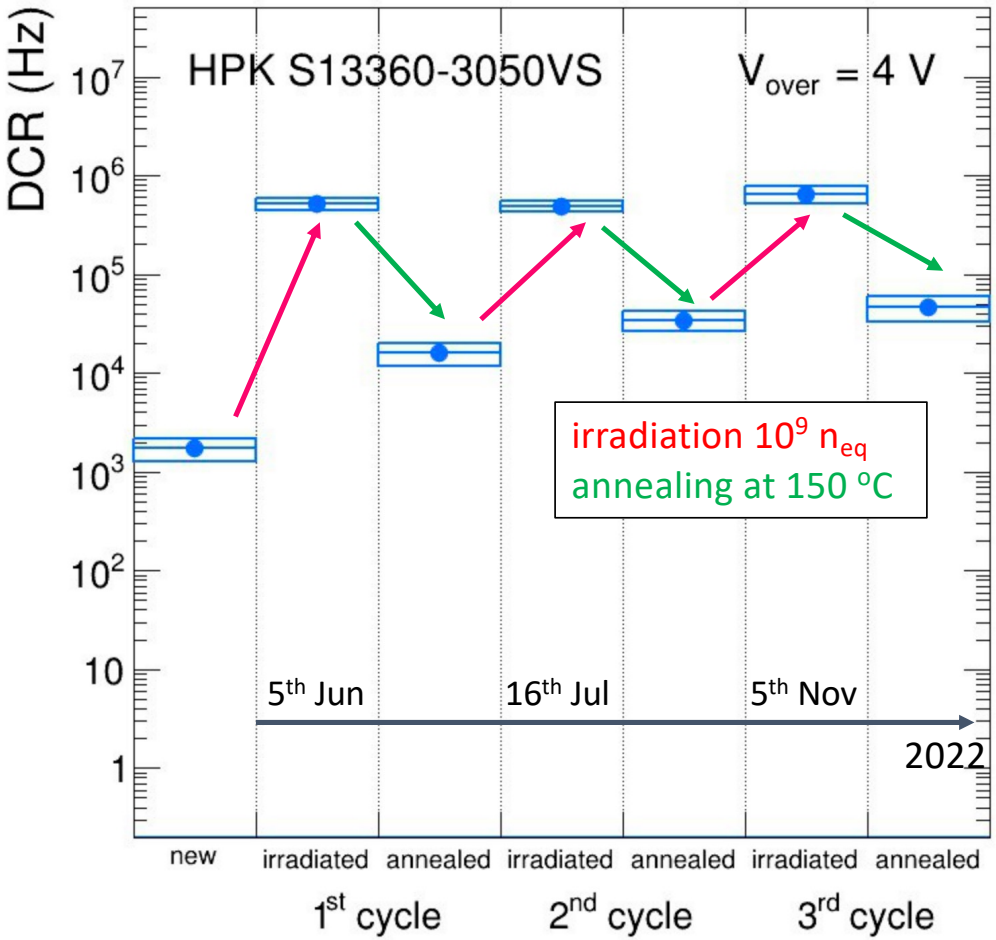
Fig.2

Results from (new) background task force

Current position of sensors: z = 100 cm R ~ 235 cm (higher than in my usual estimate…)

2022 campaign: irradiation + annealing cycles

See Luigi's talk



"getting closer to the experimental setup"

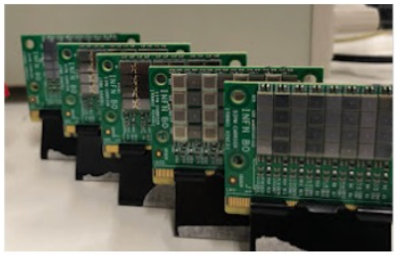
- test reproducibility of repeated irradiated/annealing cycles on the same sensors. **On-going campaign**: next shot 3rd December!
- each shot is 10^9 n_{eq} (remember: 0.2/1 year EIC at max lumi)
- extract parameters (sensor and V_{over} specific!) to shape annealing cycles in the experiment:
  - f_d : every 10^9 n_{eq} increases by 500 kHz DCR pixel rate (3x3 mm^2)
  - f_a : each annealing leaves 15 kHz of additional DCR rate

$$DCR_r\,(k) = DCR_0 + f_d + (k-1)f_a$$

DCR after k irradiation and k-1 annealing cycles

- damage and recovery remain additive
- annealing repairs f_a/f_d of a given sensor (97% here)

Total of 134 sensors under test

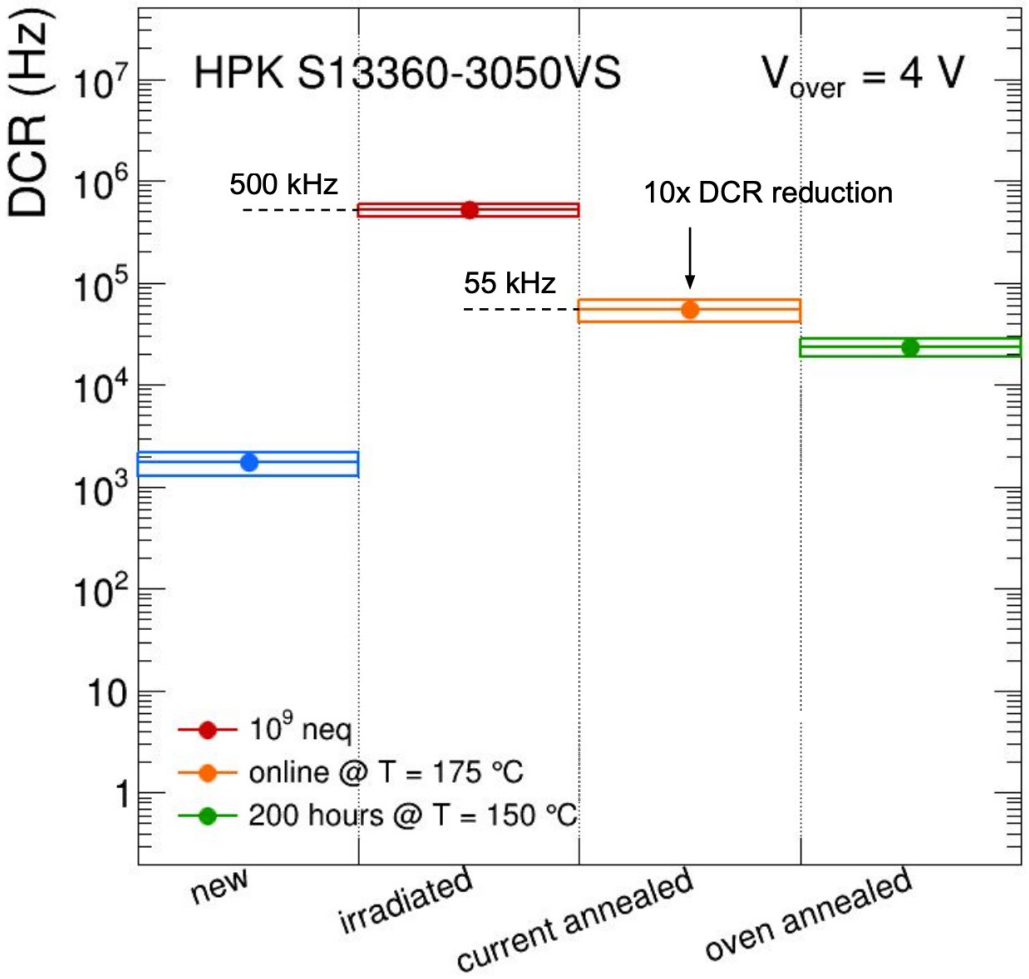


Electrically induced annealing techniques

The sensors current-annealed found at 55 kHz

Residual DCR not good as in oven (15 kHz) but:

- 100 times faster!! (2.5 hours vs 200 hours!)
- can be done in-situ
- can be done more frequently -→ we reach “critical” 300 kHz after more time (more irradiation)



Specific R&D planned for 2023 on this item

How mitigate it? (II)

cooling

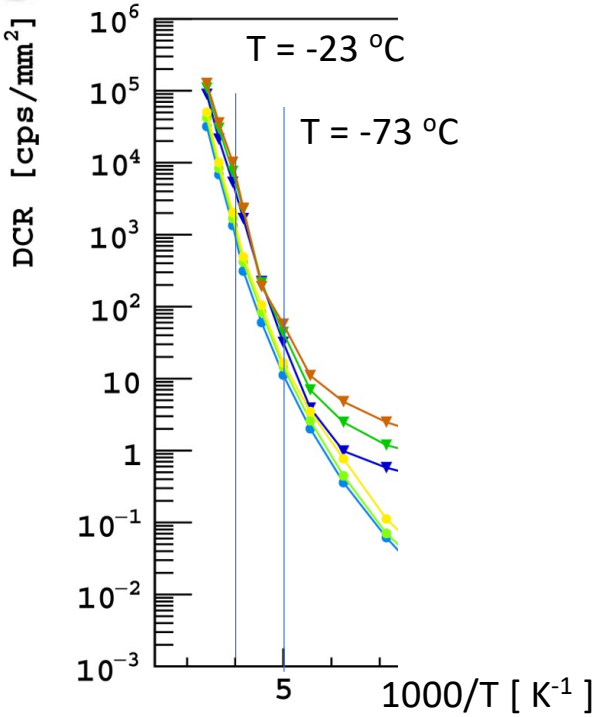
"DCR decreases by a factor 2-2.5 every 10 degrees"

annealing

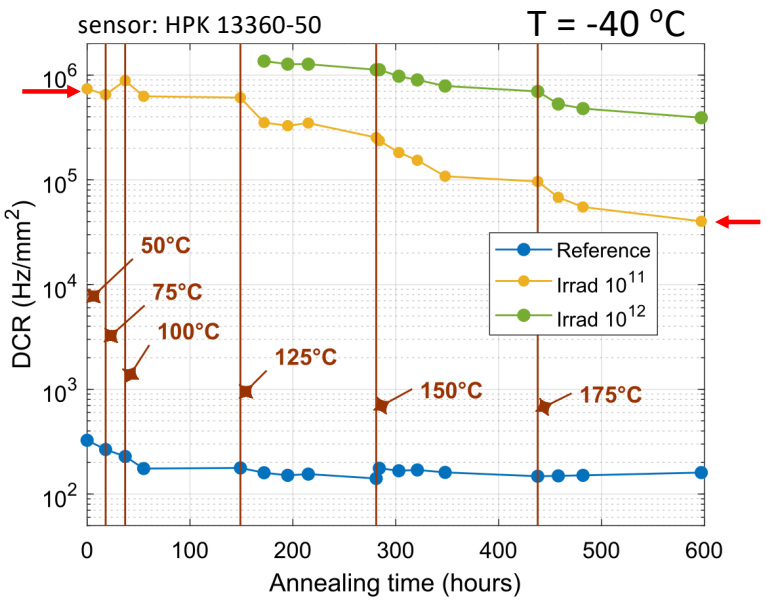
"DCR decreases by a **factor 20** after an annealing cycle up to 175 °C"

timing

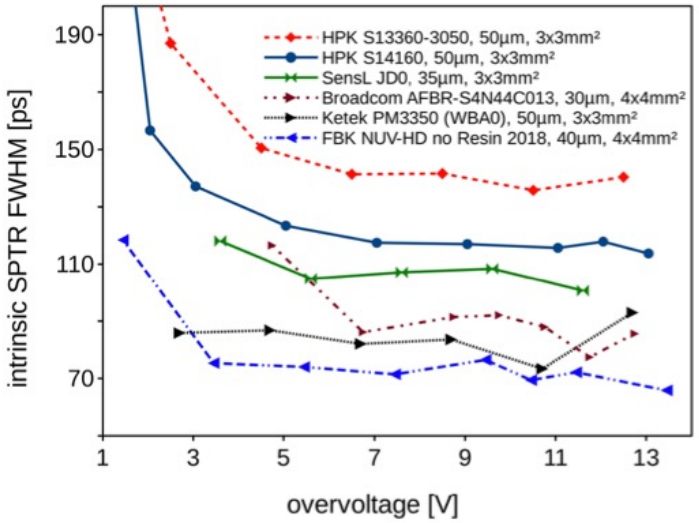
- Timing resolution below 100 ps are nowadays achieved by SiPM
- A 3σ cut based on interaction time will further reduce DCR in a RICH



Acerbi F. et al., IEEE Trans. On El. Devices 64 (2017) 521



M. Calvi et al., NIMA 922 (2019) 243



S. Gundacker et al., Phys. Med. Biol. **65** (2020) 025001

How to mitigate DCR/how impact on ALCOR?

- Cooling
- Annealing → in-situ… ”high” temp + current
- Timing: shutter. → new feature of ALCOR see Giulio’s talk
- Timing: coarse (FPGA)
- Timing: further cuts (see next slides) DAM or Online level (PC) → ALCOR time resolution
- Aggregation algorithms (not based on AI, and moderately on time resolution)
- AI/chatGPT at DAM level ;-)

ALCOR time resolution:
is really 150 ps (even if LSB 25 ps)?

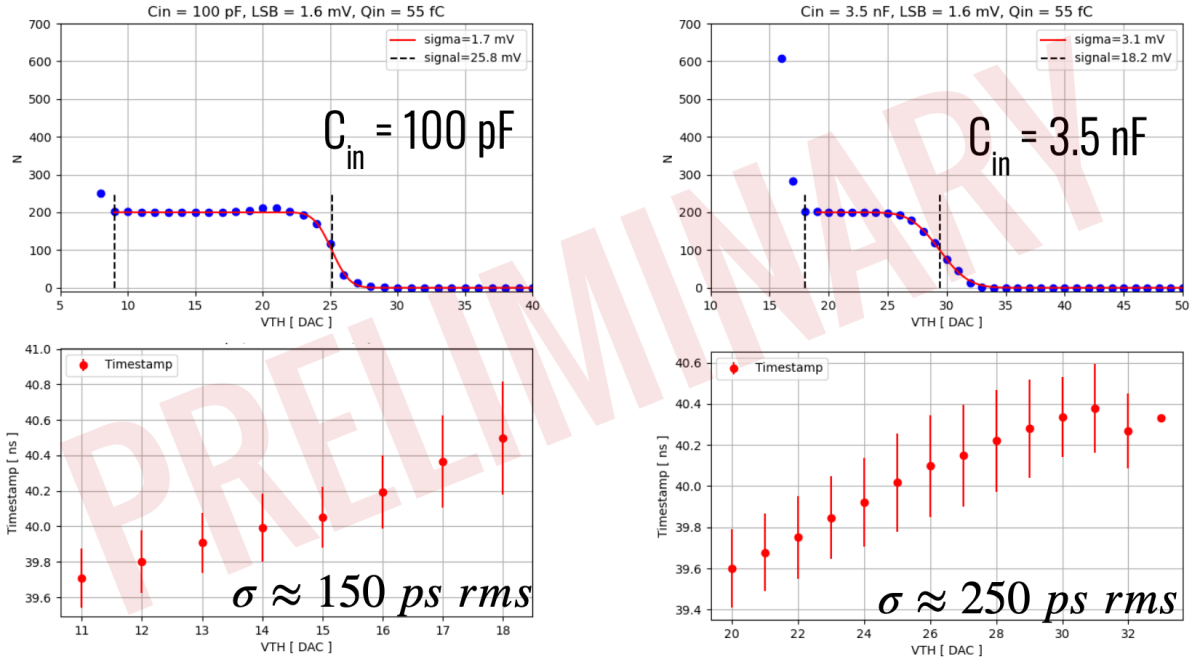
To further gain in background rejection (with respect to shutter)
ALCOR+SIPM resolution must be able to cut **within 1 ns**

→ σ ~ 150 ps → 3 σ-cut (right/left)= 900 ps

but if we could have 100 ps -→ 600 ps

Intrinsic time resolution

- Repeated test-pulses (N=200) using on-chip calibration circuit, external capacitor mounted on one ALCOR channel
- Vth scan to evaluate noise and time resolution
- Note: contribution to noise and time resolution from test-pulse generator still to be disentangled. Room temperature.



Manuel & Fabio, giornate nazionali EIC 2021 (Dicembre)
https://agenda.infn.it/event/28762/contributions/146408/attachments/87284/116576/20211121_ALCOR4EIC.pdf

Punti per discussione / "desiderata" / requirements / misure da fare per ALCOR

- test operations at 98 MHz * 3 and 98 MHz * 4
- shutter a 1 ns + time alignment
- timing: misure caratterizzazione risoluzione intrinseca + σ < 100 ps?
- bandwidth improvements?
- 64 ch + packaging
- […]