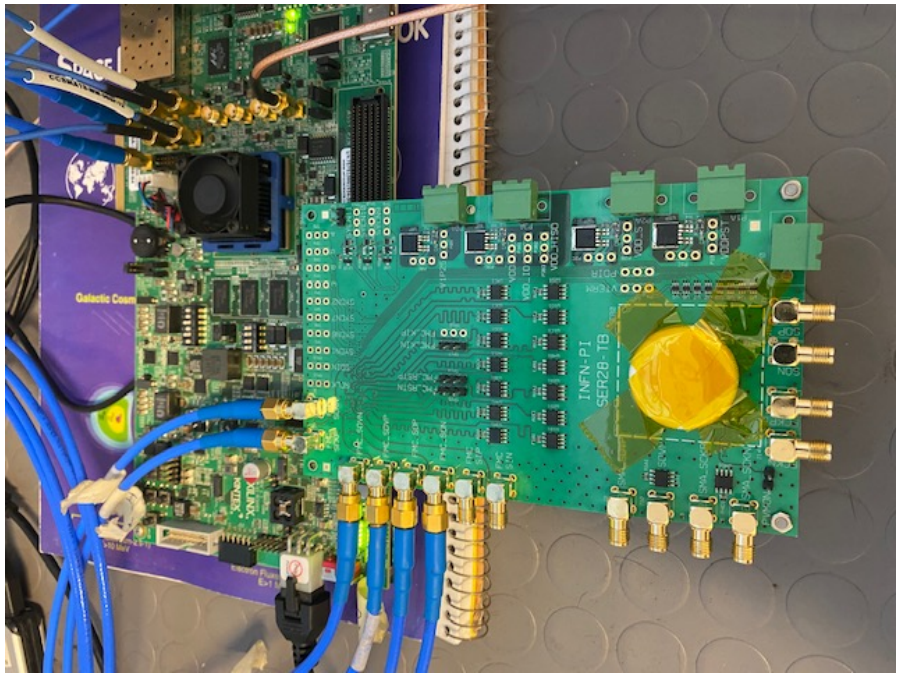
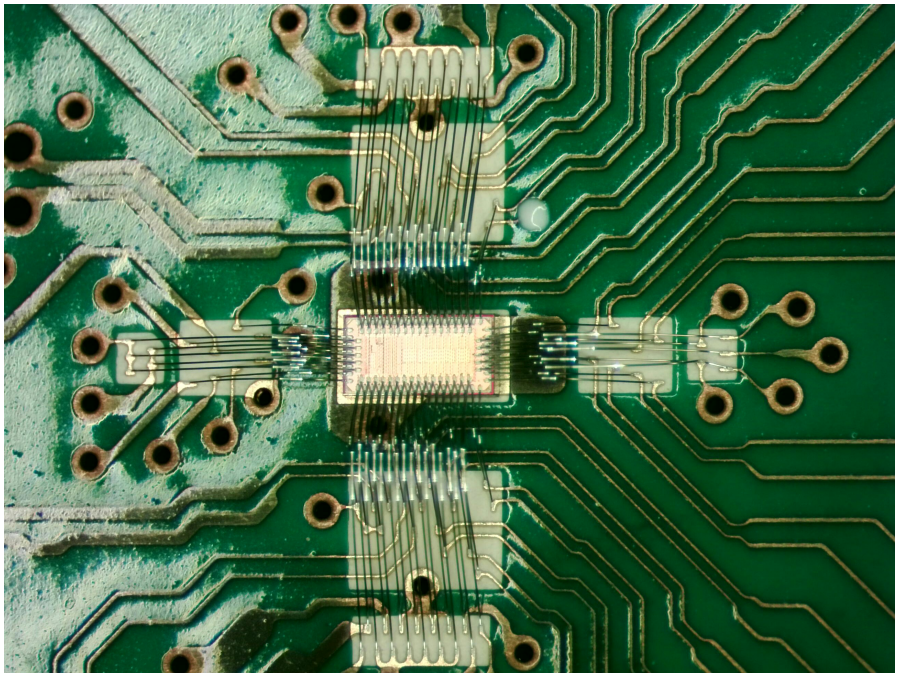
SER28: Test Setups and First Test Results

Guido Magazzù – INFN Pisa

Falaphel Collaboration meeting – February 15th 2023

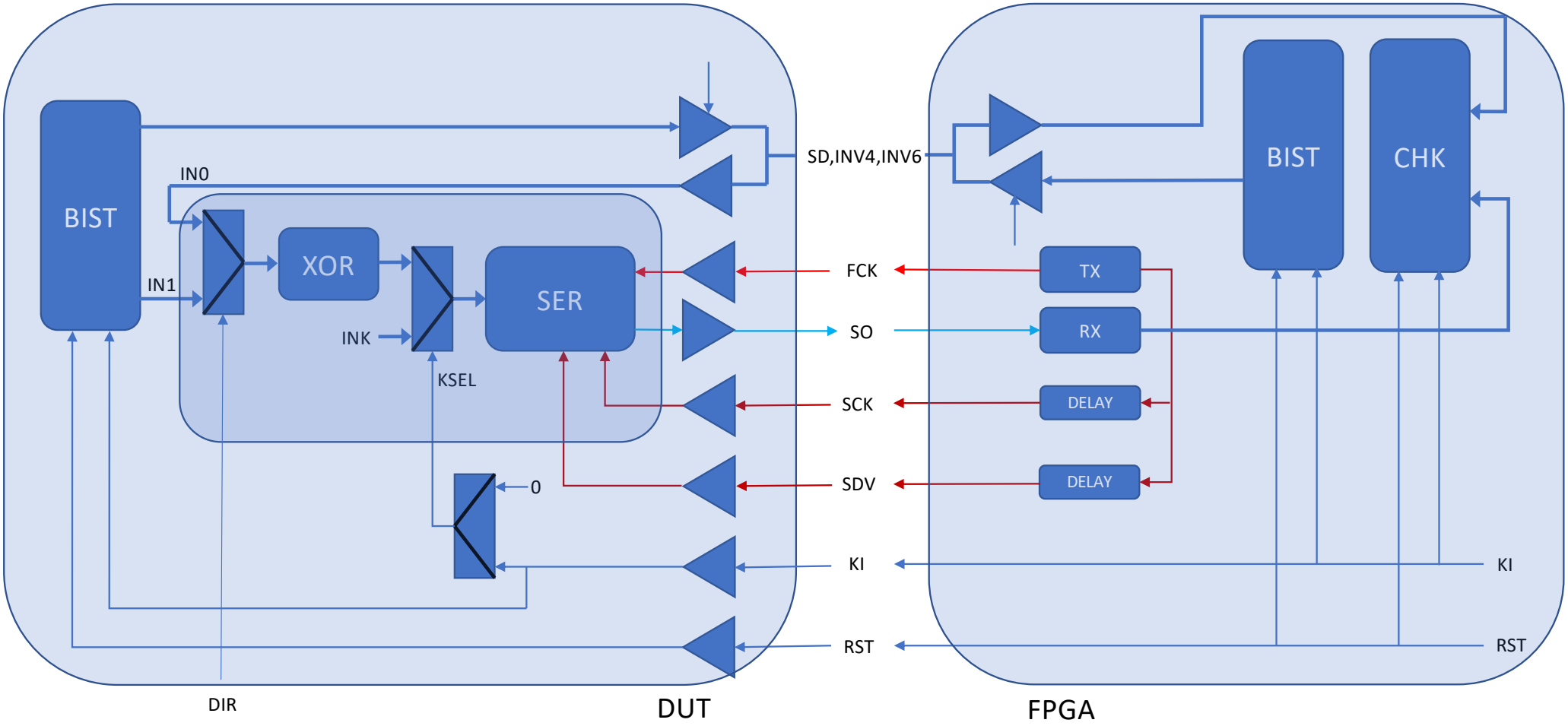
SER28 Test Board



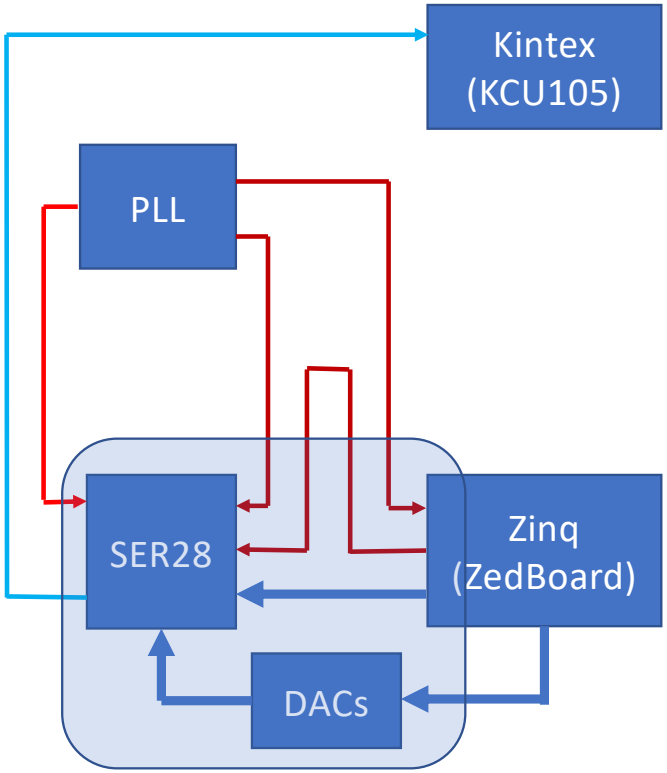


- **SER28 Test Boards delivered the 25th of November (three weeks delay)**
- **5 PCBs assembled**
  - **3 type TOP (FPGA mode) => SER parallel port (input) controlled by FPGA**
  - **2 type BOTTOM (BIST mode) => SER parallel port (output) controlled by on-chip BIST**

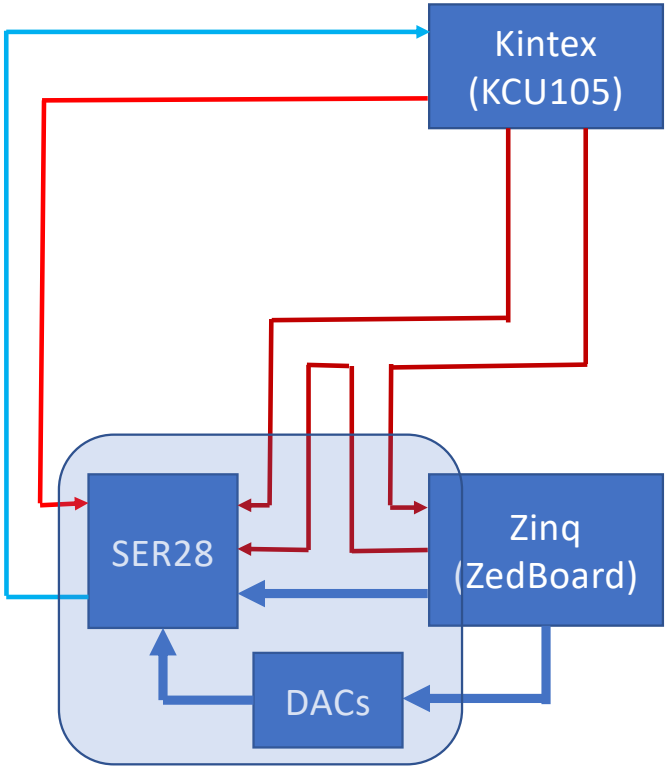
SER28 Test Setup (I/O)



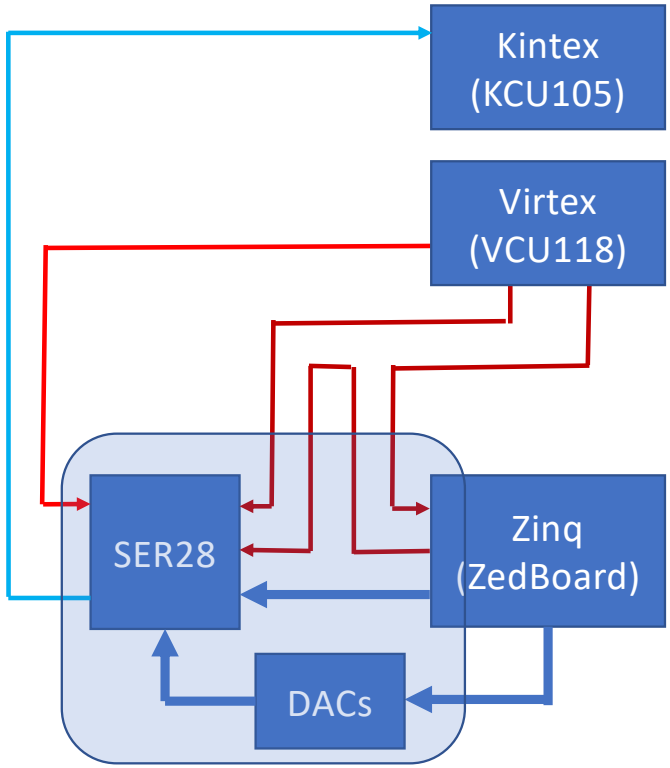
SER28 Test Setup (Configurations)



Setup 1 => 1Gbps – 2Gbps

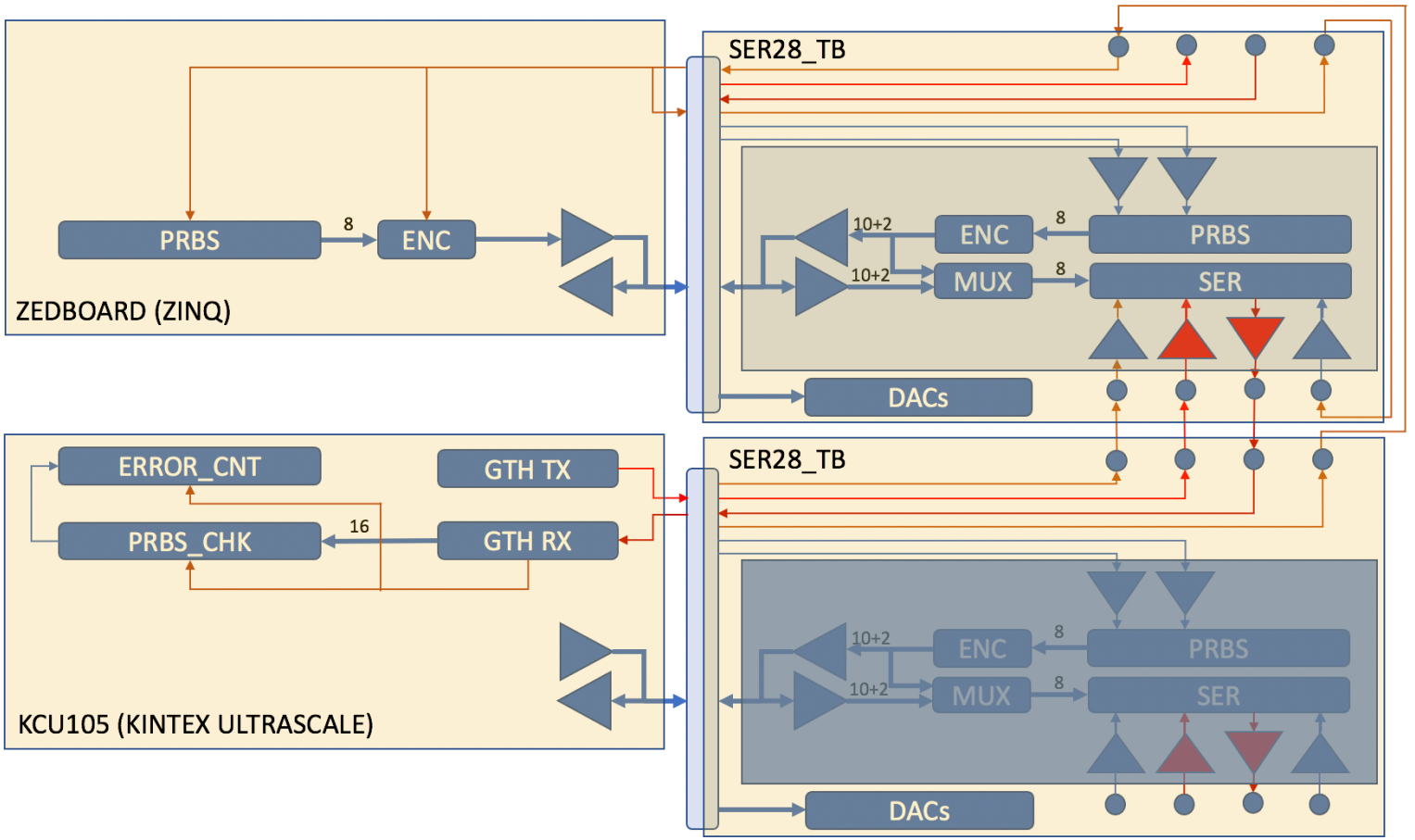


Setup 2 => 1Gbps – 5Gbps

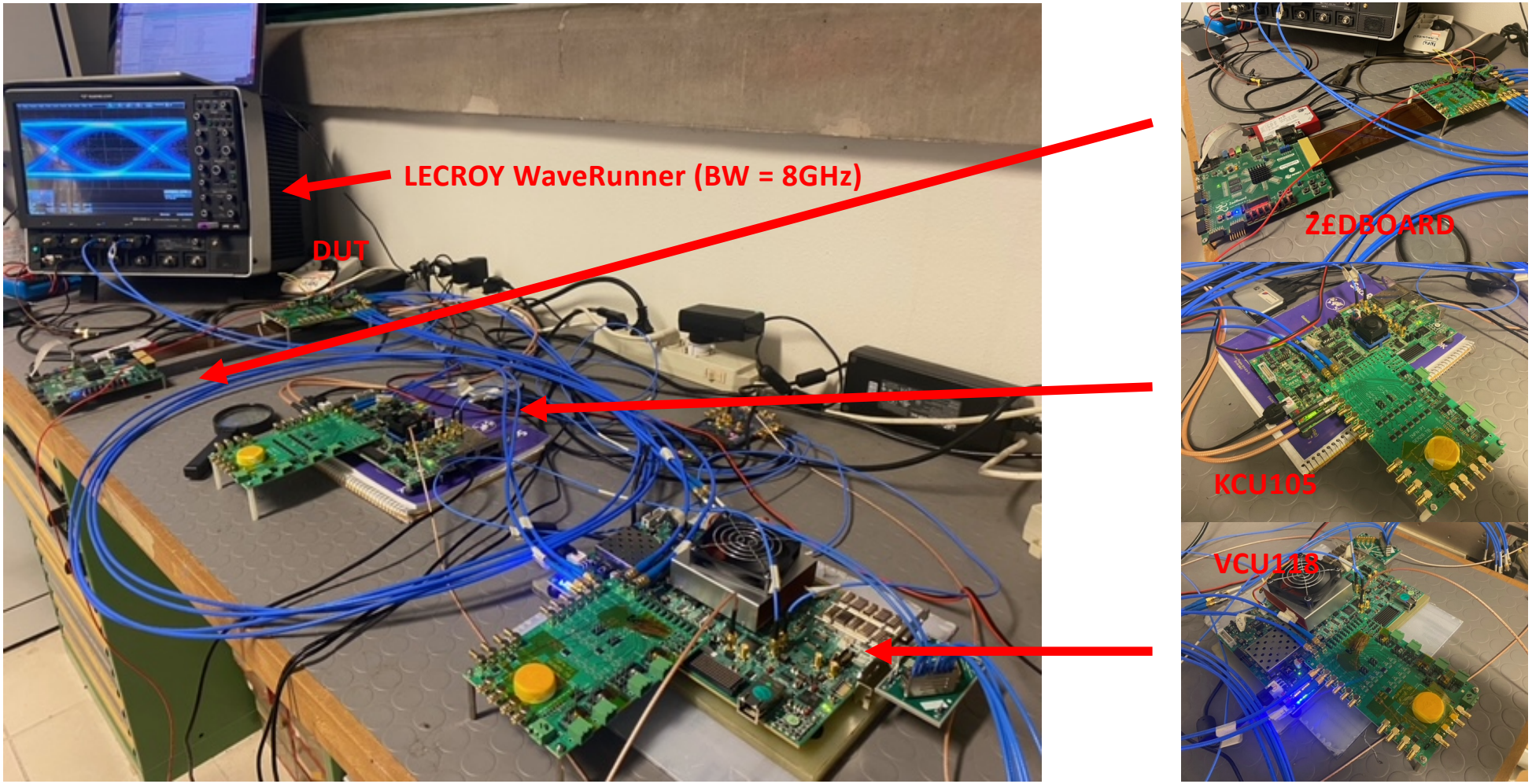


Setup 3 => 5Gbps – 10Gbps

SER28 Test Setup (Setup 2 architecture)



SER28 Test Setup (Setup 3 in action)



Main issues

- PCB issues (we required the production of a second PCB batch!)
  - Wrong final bonding diagram => The pad ring simmetry helped a lot but we needed some patches (thanks Fabio!)
  - Reduced size of wire bonding pads on the PCB (thanks Mirko and Alessandro!)
- Power issues
  - The current absorbed by the SER (ca. 400mA) generates voltage drops that must be compensaded providing a higher voltage at the PS (ca. 120mV on the cable, X between the power connector and the IC core)
- Noise issues
  - Noise has been detected (20-25MHz) on the power supply voltage provided by on-board regulators – extra capacitors have been added (thanks Massimo!)
- Cabling issues
  - Cable losses become critical at high frequency (> 5GHz)

Clock Amplitude vs. Cable type

Test Setup Output

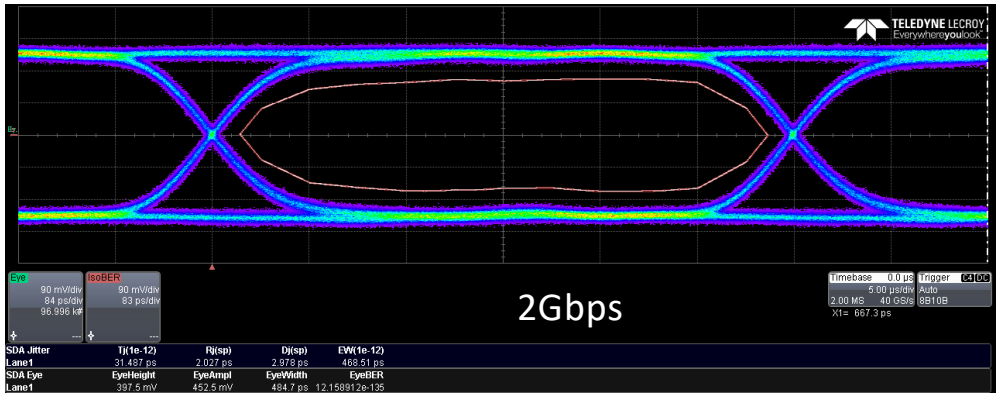
CODE	Low	High	Peak2Peak
Short Metallic	308 mV	463 mV	155 mV
Short Blue	298 mV	468 mV	170 mV
Long Blue	320 mV	447 mV	127 mV

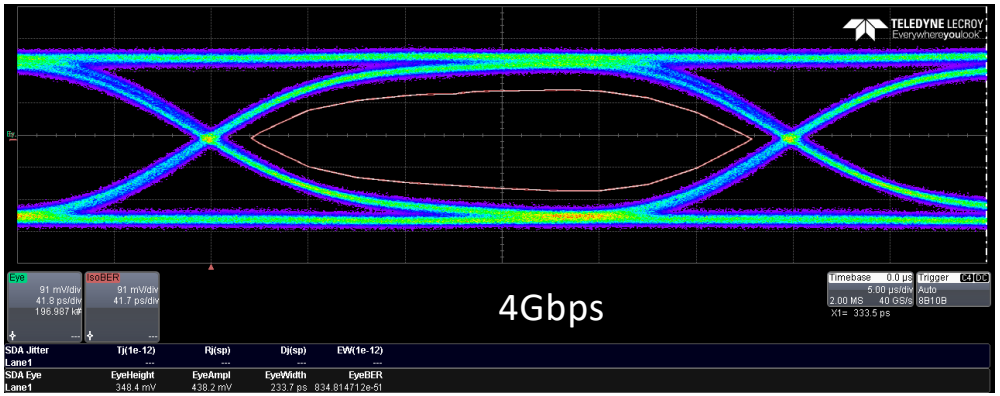
KCU105 Output

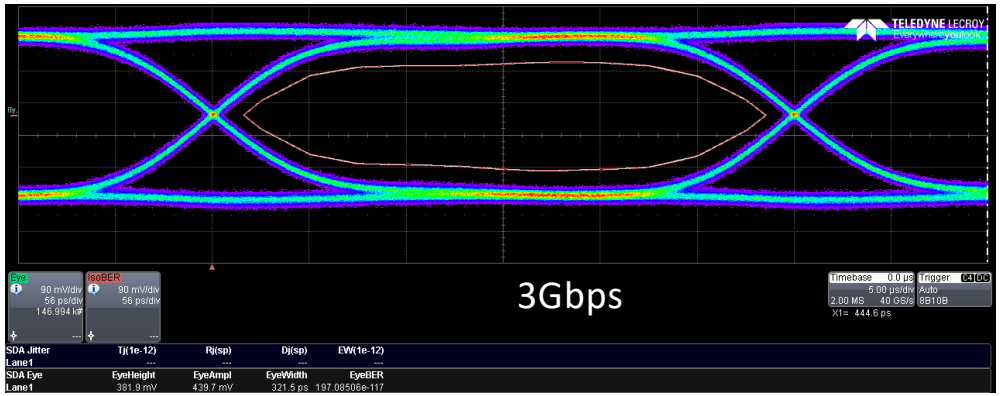
CODE	Low	High	Peak2Peak
Short Metallic	233 mV	563 mV	330 mV
Short Blue	223 mV	570 mV	347 mV
Long Blue	262 mV	536 mV	274 mV

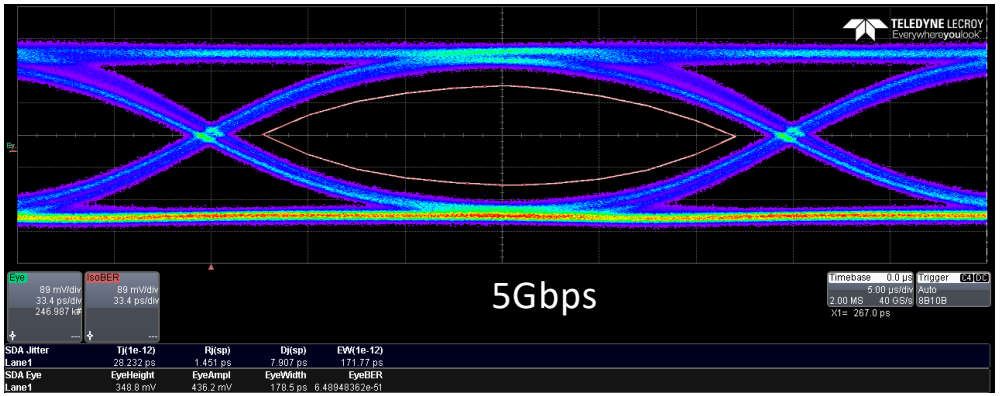
Different cabling configurations have been characterized in order to select the “optimal” one

Eye Diagrams (Test Setup 2)

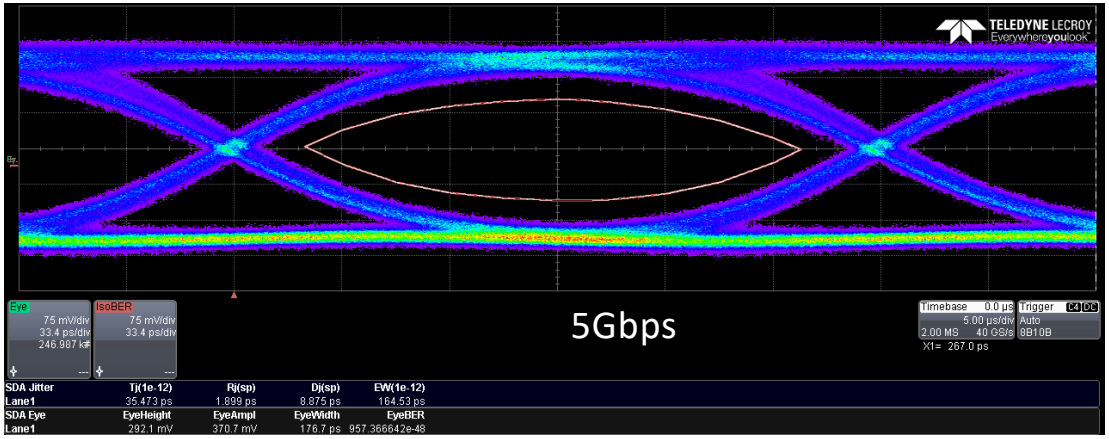


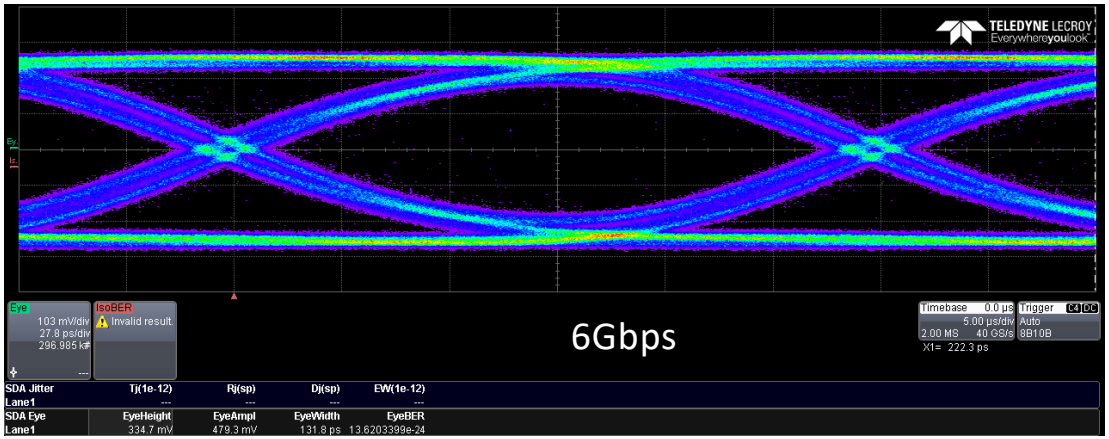




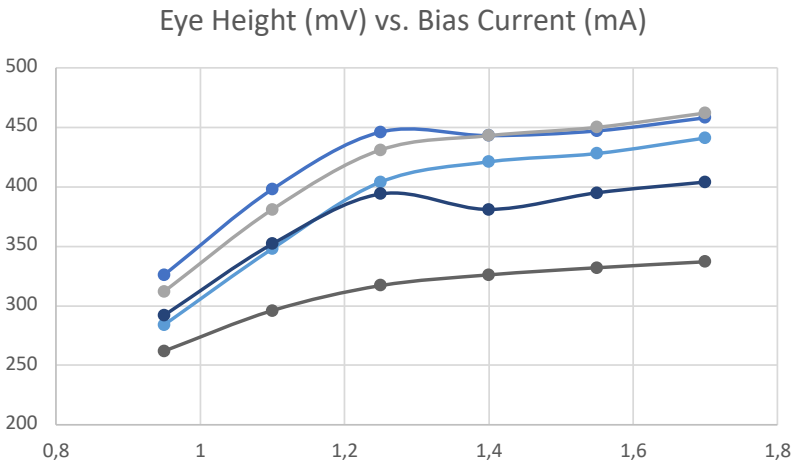


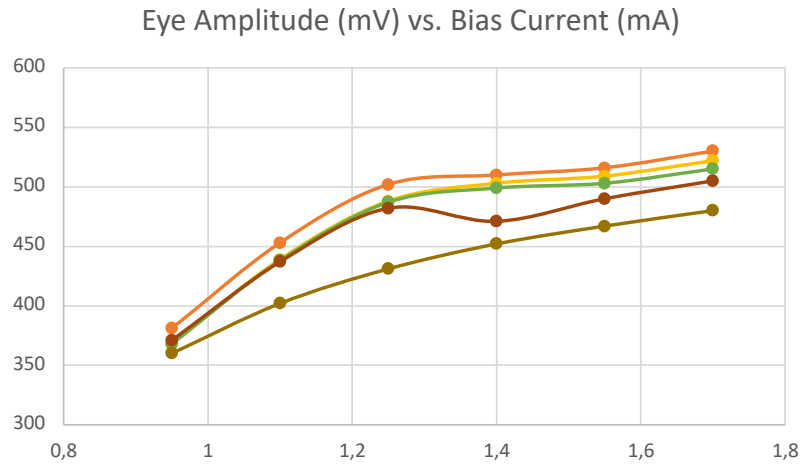
Eye Diagrams (Test Setup 3)





Eye Height & Amplitude vs. Bias current





Test Setup 2 => 2,3,4 Gbps - Test Setup 3 => 5,6 Gbps

Test Status

FPGA MODE (Boards T1 & T2)

Test	Eye Characterization	Error Counters
Setup 1 (1-2 Gbps)	K Mode => 1,2 Gbps	K,1P,4P Modes => 2Gbps PRBS Mode => ?
Setup 2 (2-5 Gbps)	K Mode => 2,3,4,5 Gbps	K,1P,4P Modes => 5Gbps PRBS Mode => ?
Setup 3 (5-10 Gbps)		

Test	Eye Characterization	Error Counters
Setup 1 (1-2 Gbps)	K Mode => 1,2 Gbps	K,1P,4P Modes => 2Gbps PRBS Mode => ?
Setup 2 (2-5 Gbps)	K Mode => 2,3,4,5 Gbps	K,1P,4P Modes => ? PRBS Mode => ?
Setup 3 (5-10 Gbps)	K Mode => 5,6 Gbps	K,1P,4P Modes => ? PRBS Mode => ?

BIST Mode (Boards B1 & B2)

Test	Eye Characterization	Error Counters
Setup 1 (1-2 Gbps)	K Mode => ?	K,1P,4P Modes => ? PRBS Mode => ?
Setup 2 (2-5 Gbps)	K Mode => ?	K,1P,4P Modes => ? PRBS Mode => ?
Setup 3 (5-10 Gbps)	K Mode => ?	K,1P,4P Modes => ? PRBS Mode => ?

Test	Eye Characterization	Error Counters
Setup 1 (1-2 Gbps)	K Mode => ?	K,1P,4P Modes => ? PRBS Mode => ?
Setup 2 (2-5 Gbps)	K Mode => ?	K,1P,4P Modes => ? PRBS Mode => ?
Setup 3 (5-10 Gbps)	K Mode => ?	K,1P,4P Modes => ? PRBS Mode => ?

Future Plans

- Characterize the SER performance w.r.t SER Bias Voltage and VDD (February)
- Perform BER tests using the error counters in the Kintex FPGA (February)
- Test and Characterize the SER28 in the BIST mode (February)
- Perform test at the CrossLab with higher BW Oscilloscope (February)
- Perform Irradiation test at the INFN-Pisa X-Ray facility (March)

Acknowlegments

Thanks to

- Fabio Morsani
- Massimo Minuti
- Paolo Prosperi
- Alessandro Profeti
- Mirko Brianzi