Lo «strano» caso del progetto

IGNITEd

INFN Ground-up iNITiative for µElectronics developments

INFN Istituto Nazionale di Fisica Nucleare

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What's ?

IGNITEd

INFN Ground-up iNITiative for µElectronics developments

INFN Istituto Nazionale di Fisica Nucleare

- Beneath the ash always brace is hatching…
- **Ignite !**

The 2021 ECFA detector research and development roadmap – 10.17181/CERN.XDPL.W2EX

"Technical" Start Date		< 2030			2030 -2035	2035 -2040	2040 - 2045		> 2045	
		ALICE LS3	Belle II CBM	NA62	LHCb, ATLAS, CMS (≳ LS4)[7]	ALICE 3 - EIC	ILC	FCC-ee	CLIC	FCC-hh	Muon Collider
MAPS	technology node[1]	65 nm - stitching	65 nm - stitching			28 nm		≲ 28 nm		≃ 10 nm	≲ 28 nm
	pitch	10 - 20 μm	10 - 20 μm			pitch ≲ 10 μm for σ_{hit} ≲ 3 μm in VD					
						Reduce z-granularity in TK - pad granularity in analog Cal.					
	wafer size[2]	12"	12"			12"					
	rate[3]			O(100) MHz/cm^2					5 GHz/cm^2	30 GHz/cm^2	
	ultrafast timing[4]					σ_t ≲ 100 ps				σ_t ≲ 20 ps	
	radiation tolerance				3 x 10^{15} neq/cm^2					10$^{18(16)}$ neq/cm^2 VD/Cal.(Trk)	
Planar/3D/Passive CMOS	technology node[1]				ASIC 28 nm	ASIC 28 nm		ASIC ≲ 28 nm		ASIC ≃ 10 nm	ASIC ≲ 28 nm
	pitch				≲ 25 μm in VD	≲ 10 μm for σ_{hit} ≲ 3 μm in VD					
						≲ 50 μm for σ_{hit} ≲ 10 μm in Trk					
	wafer size[2]					12"					
	rate[3]				6 GHz /cm^2					30 GHz/cm^2	
	ultrafast timing[4]			σ_t ≃ 50 - 100 ps		σ_t ≲ 100 ps				σ_t ≲ 20 ps	
	radiation tolerance				6 x 10^{16} neq/cm^2					10$^{18(16)}$ neq/cm^2 VD/Cal.(Trk)	
LGADs	technology node[1]						ASIC 28 nm	ASIC ≲ 28 nm		ASIC ≃ 10 nm	
	pitch			≃ 300 μm (100% fill facor)	≲ 50 μm (100% fill facor)	same as for other technologies with ultimate pitch ≲ 10 μm for σ_{hit} ≲ 3 μm in VD					
	wafer size[2]				> 3"	12"					
	rate[3]				6 GHz /cm^2					30 GHz/cm^2	
	ultrafast timing[4]				σ_t ≲ 30 ps	σ_t ≃ 20 ps (PID)	σ_t ≲ 20 ps VD/Trk/Cal.	σ_t ≲ 10 ps PID	σ_t ≲ 20 ps VD/Trk/Cal.	σ_t ≲ 20 ps VD/Trk/Cal.	
	radiation tolerance				≳ 5 x 10^{15} neq/cm^2					10$^{18(16)}$ neq/cm^2 VD/Cal.(Trk)	
backend processing	sensor thickness[5]	< 50 μm MAPS	< 50 μm MAPS		< 150 μm Plan/3D/Pas. < 50 μm LGADs	< 50 μm MAPS, Planar/3D/Passive CMOS, LGADs					
	3D integration[6]										

Crucial requirements for 4D-Tracking

A High-Statistics-Discovery tool for Physics at High Intensity, in the next generation of upgrades in experiments at colliders (and beyond):
LHCb Upgrade-II (run5), **HIKE** (NA62 Upgrade), CMS endcap (run5), CMS-PPS (run4), ATLAS AFP (run5?), Pioneer (proposal at PSI, π rare decays), ν–tagging (proposal) … FCC-hh (far perspective)

1. Space Resolution $\sigma_s \approx 10$ μm
2. Time Resolution $\sigma_t \leq 30$ ps per hit
3. Radiation hardness to high fluences $\Phi = 10^{16} \div 10^{17}$ 1 MeV n_{eq}/cm^2
4. Detection efficiency $\varepsilon > 99\%$ per layer tipically required (high fill factor)
5. Material budget must be kept below 1 ÷ 0.5 % radiation length per layer

Fast and rad-hard sensors

Key requirements for read-out electronics:

1. Pixel pitch ≈ 50 μm (unless amplitude information for CoG techniques is used)
2. Time Resolution $\sigma_t \leq 50$ ps on the full chain ($\sigma_t = \sigma_{sensor} \oplus \sigma_{FE} \oplus \sigma_{TDC}$)
3. Radiation hardness TID > 1 Grad
4. Power budget per pixel ≈ 25 μW (referred to the case of 55 μm pitch, 1.5 W/cm²)
5. Data BW ≈ 100 Gbps/cm²

CMOS 28-nm electronics

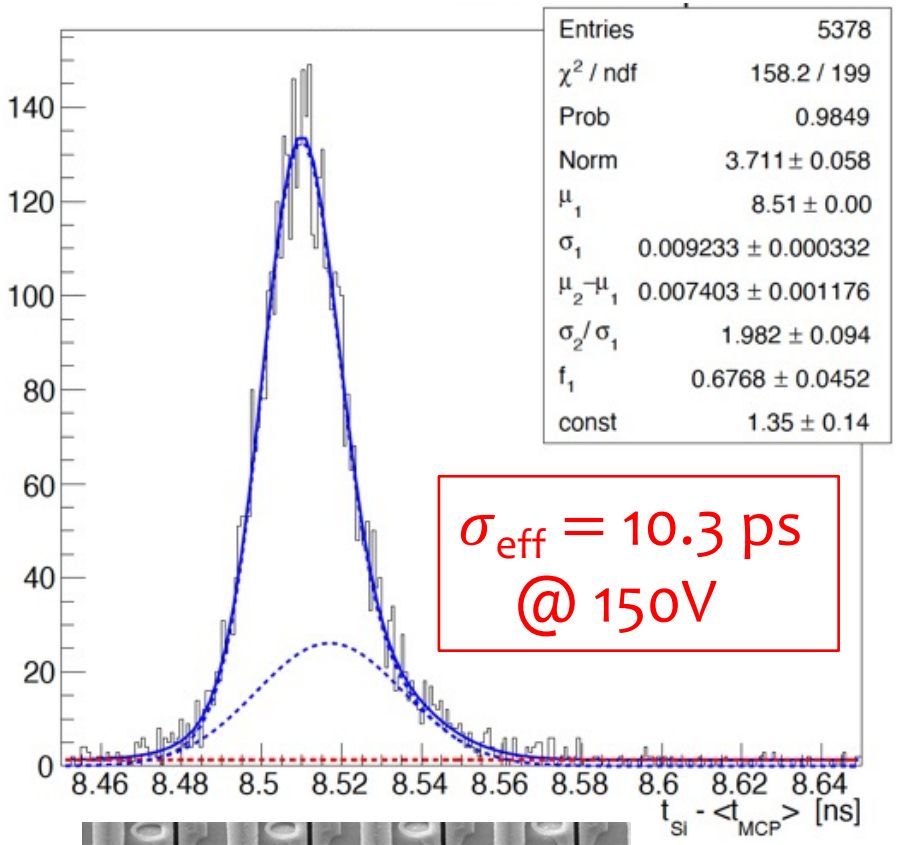
Results on Sensors and Electornics

2018 - 2021

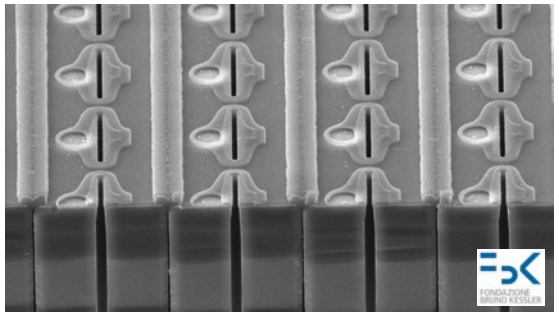
AM-xx 28nm
Associative Memories

Scaltech28
28nm rad hardness

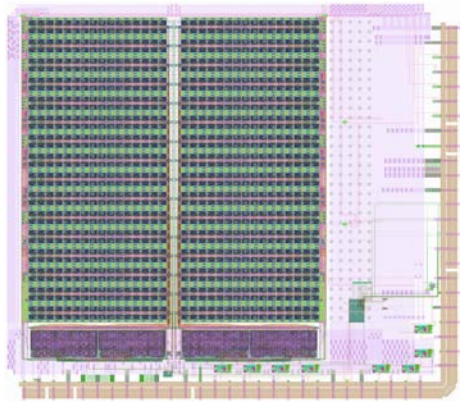
Irradiated @ 2.5 10^{16} n_{eq}/cm^2 , $\alpha_{tilt} = 0°$

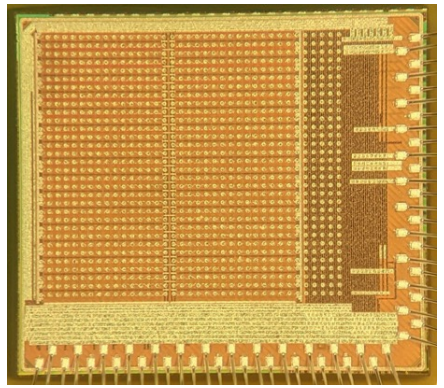


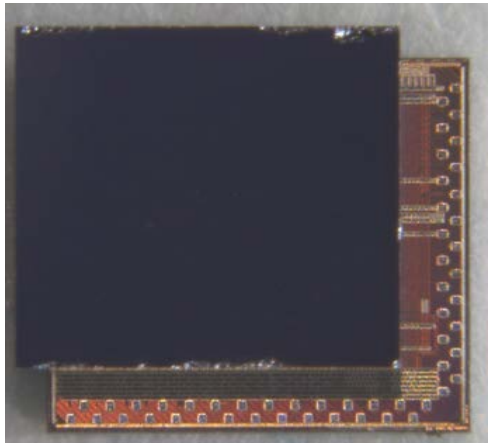
$\sigma_{eff} = 10.3$ ps
@ 150V



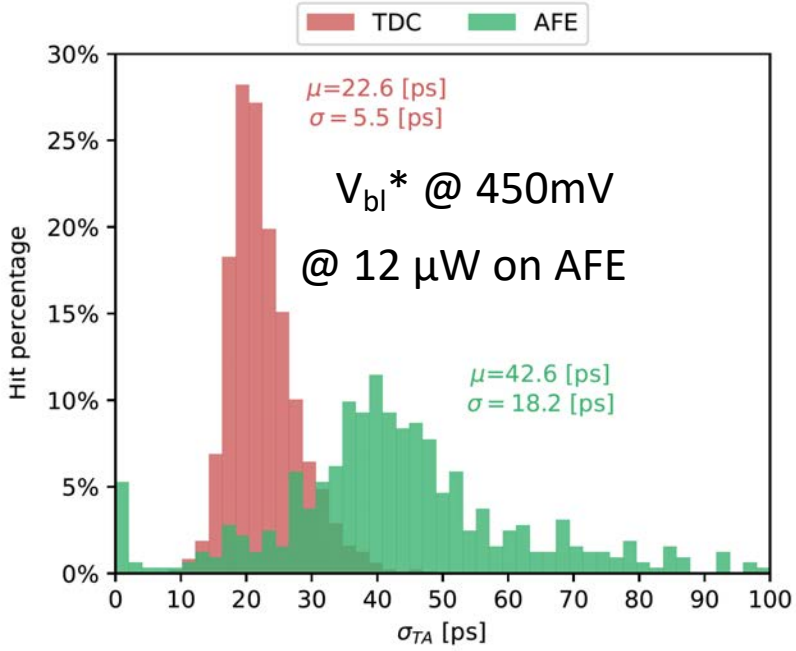
3D-trench Silicon sensors







CMOS 28-nm Timespot1 ASIC



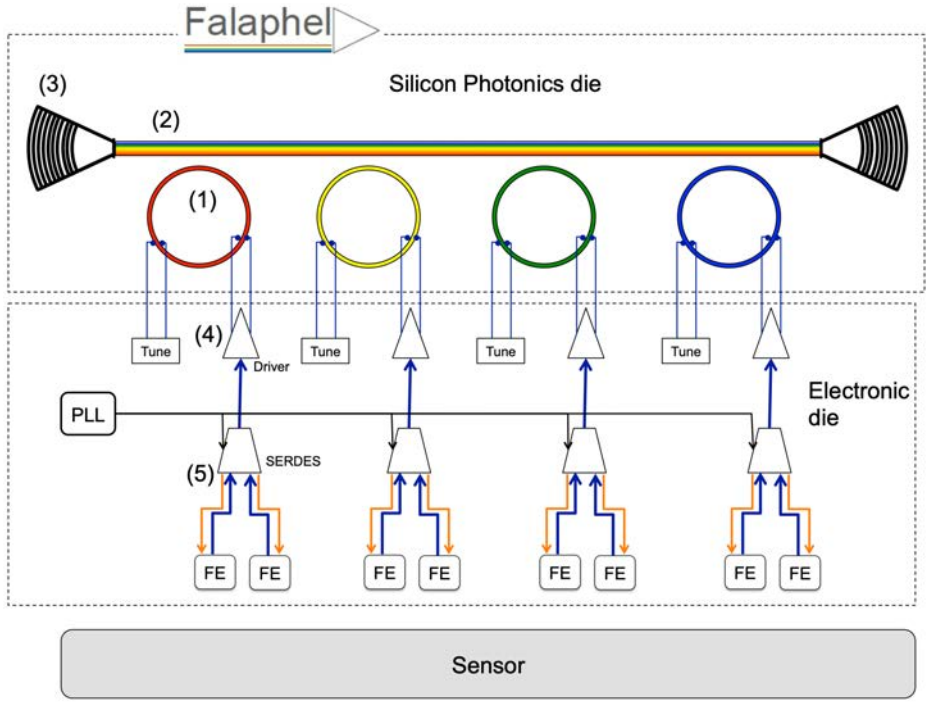
Distribution of the TA standard deviation across 1024 channels and 7 clock phases.
Each point is computed from **100** repeated measurements.

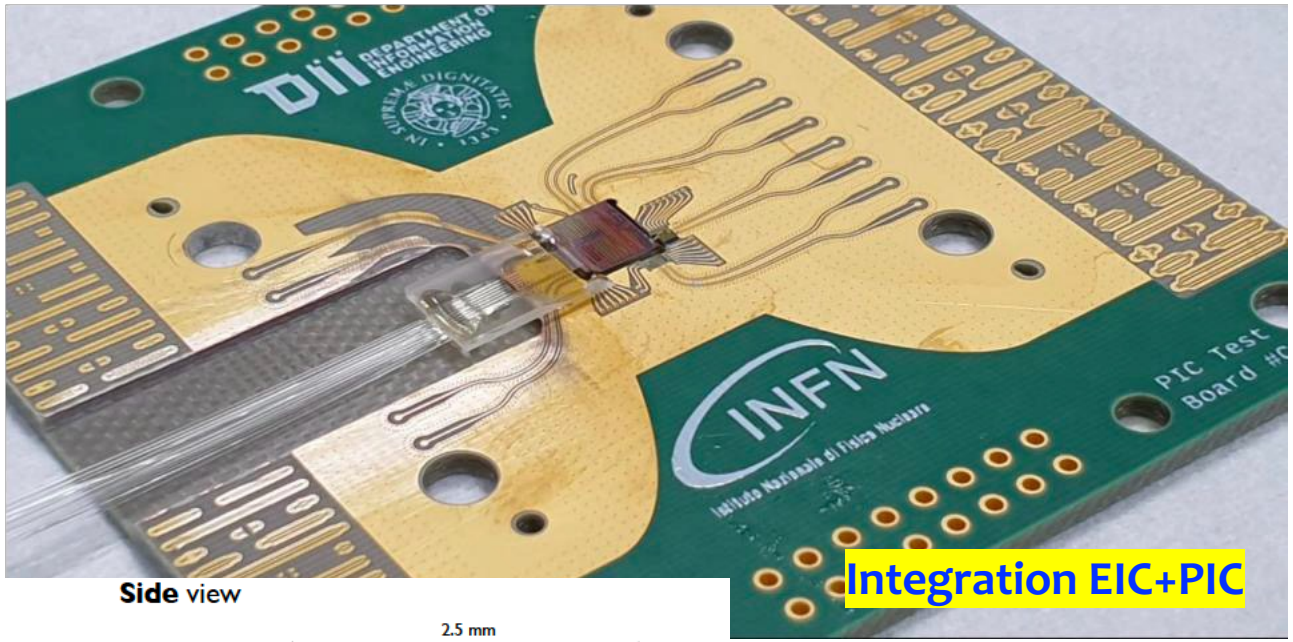
Falaphel

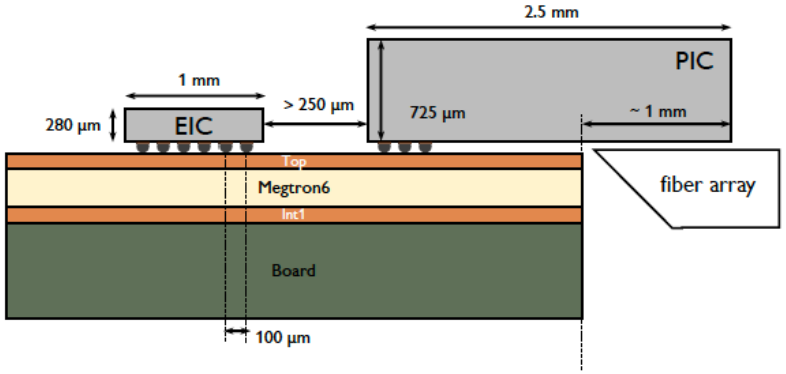
2021 – 2023 (24)

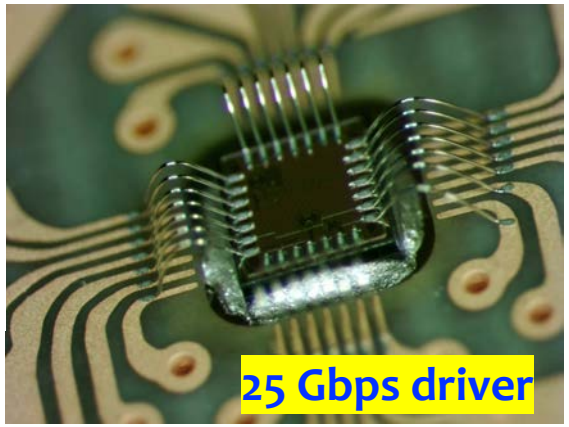
R&D in Silicon Photonics for High BW data transmission

CMOS 28-nm (EIC) + Photonic IC (PIC)









Falaphel developments:

- Chip FE (TSMC 28-nm)
- Serializer 12.5 Gbps (TSMC 28-nm)
- Driver 25 Gbps (TSMC 28-nm)
- Ring Modulator (Silicon Photonics)
- Integration

IGNITE R&D Program (2023–2027):

- Development of a new ASIC in CMOS 28nm technology with full specifications in terms of size, pitch, resolution, data rate etc.
- Development of a suitable/matched Integrated-Photonics device (PIC)
- Development of an integrated module (size ≈ 10 cm²), satisfying the system specs and comprising:
  - The sensors (3D TimeSPOT)
  - One or more IGNITE readout ASICs and their matched PICs
  - Cooling plate/system
- All the above with minimum material budget (target: 0.5 % X_0 ≈ 500 μm of Si)

Activity	2023				2024				2025				2026			
	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
Study and definition of ASIC1 design specs																
Study and definition of PIC1 design specs																
ASIC1 design and verification																
PIC1 design and verification																
ASIC1 submission and production																
PIC1 submission and production																
Design and integration of ASIC/PIC1 system																
ASIC1 & PIC1 test and characterization																
ASIC1 Hybridization																
ASIC1/PIC1 (IGNITE1) system testsbeams																
ASIC2 design and verification																
PIC2 design & verification																
ASIC2 submission and production																
PIC2 submission and production																
Design of IGNITE2 system																
Integration of IGNITE2 system																
ASIC2 test and characterization																
PIC2 test and characterization																
ASIC2 Hybridization																
ASIC2/PIC2 testbeams on system components																
IGNITE2 system full tests																

Obiettivi cardine del progetto

1. Realizzare **soluzioni tecnologiche** per la prossima generazione di esperimenti ai collider (fisica ad alta intensità)

2. Mantenere e **far crescere le competenze** di elettronica e rivelatori a stato solido nell'INFN, portando al massimo compimento possibile il lavoro già fatto da noi tutti negli anni passati, specialmente recenti

3. Assicurare un futuro a queste conoscenze facendo **rete e scuola** e facendo crescere la nuova generazione di ricercatori e tecnologi, di nuovo dando **continuità ed esito** al loro lavoro di ricerca

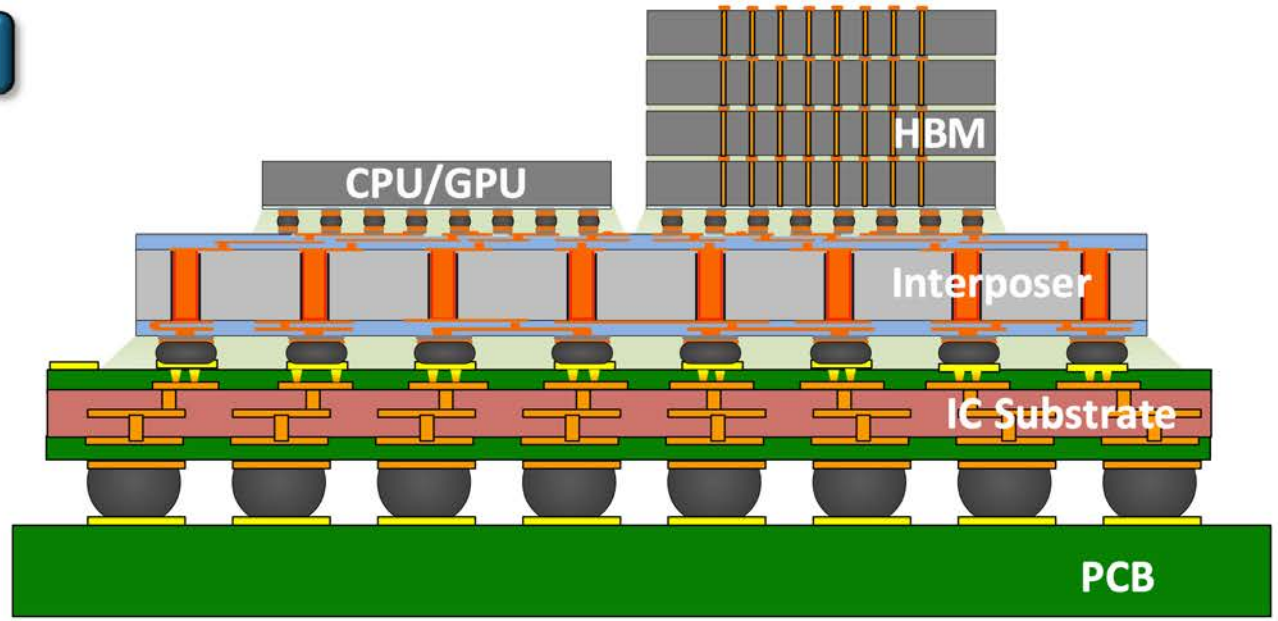
Advanced Electronic Packaging

3D/2.5D Package for High-End Performance Applications

TSVs

HBM TSV:
Diameter 6µm
Height: 55µm
Pitch: 50µm

Interposer TSV:
Diameter 10…15µm
Height: ~100µm
Pitch: 75…225µm



Interconnects

HBM stack
Diameter 20µm
Pitch 48µm

CPU/GPU/HBM to Interposer
Diameter ~25µm
Pitch 95µm

Interposer to IC substrate:
Diameter 100µm
Pitch 200µm

Datacenter Networking | **High-Performance Computing** | **Autonomous Vehicles**

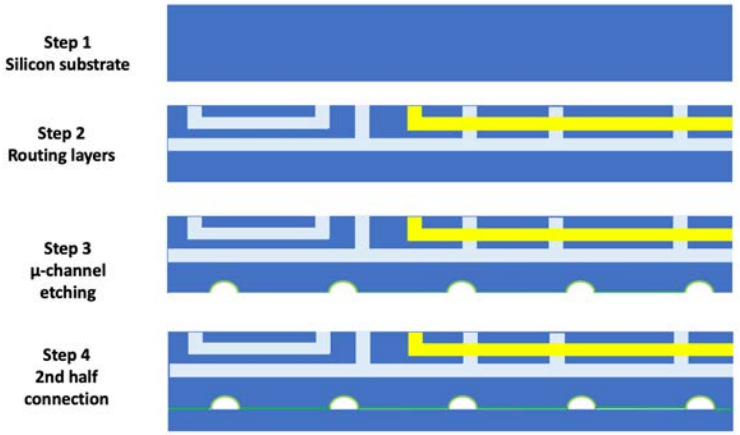
Developed by global players like SAMSUNG, INTEL, AMD, TSMC

Numbers according to High-End Performance Packaging: 3D/2.5D Integration 2022 | Report | www.yole.fr

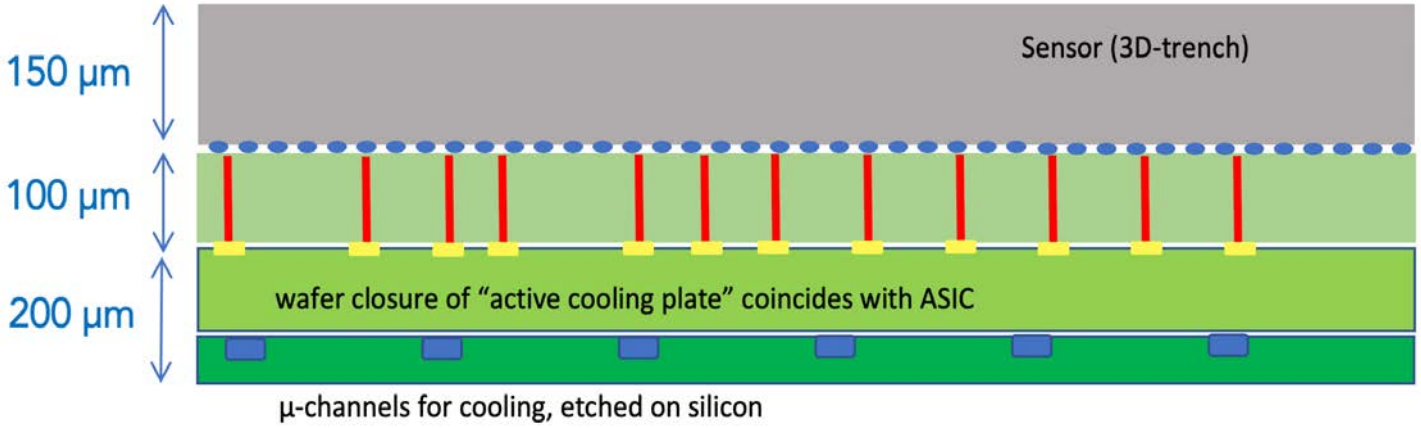
Source: T. Fritzsch, IZM, talk given at Pixel2022 workshop

System Integration concept: daring one step further

An «active cooling plate» instead of an interposer?



< 0.5 % X_0



Optical read-out (PIC) would be outside this block (see next slide)

- Hybrid (bump) bonding
- CMOS 28-nm rout ASIC (thinned, 100 µm) with TSV (red)
- Bonding (W2W?, W2D?, D2D?)
- CMOS 28-nm ASIC mainly acting as a router, could integrate data serializers and drivers separately from readout ASIC

Complications on implementing connections with refrigerant capillaries…

Assegnazioni nei 4 anni

2400 k€ a fronte dei 2680 k€ richiesti (90%)

- **Budget:**
  - **1.2 M€ su consumi per sviluppi (≈300k€/year)**
  - **1.2 M€ SJ per submission di ASIC CMOS 28-nm**
  - **PhD, AdR & tecnologi a T.D. (modalità in fase di definizione)**
- **Anni: 2023–2026**

Da considerarsi cifra media per anno

Per "vincere" questa cifra occorrerà arrivare pronti ad un Engineering run in tempo (fine 2025 max ?)

La discussione su questo punto cruciale è in corso con la GE.
≈ 3 Art36, 4 AdR, 3 PhD

Una proroga di un anno è ragionevole (a budget costante)

Sezioni coinvolte e personale 2023

INFN site	Main expertise in IGNITE	CSN1 experiment affiliations	Local responsible
Bari	Analog IPs, ASIC integration	CMS, LHCb	F. Licciulli
Bologna	ASIC verification, HDL design	ATLAS	D. Falchieri
Cagliari	TDC, Analog F/E, fast signal distribution, system design and verification, photonics	LHCb	A.Lai (R.N.)
Firenze	System integration and test, HDL design	CMS, LHCb, NA62	G. Passaleva
Genova	System integration and tests, TID characterization	ATLAS	C. Gemme
L.N. Frascati	Complex PCB design	ATLAS, LHCb, NA62	P. Ciambrone
Milano	Fast signal distribution and R/O, analog IPs	ATLAS, LHCb	A.Stabile
Milano B.	Analog IPs, TID modeling	CMS	M. De Matteis
Padova	TID studies, Analog F/E	LHCb, CMS	P. Giubilato
Pavia	Analog F/E, TID studies on Analog F/E, fast output stages, advanced interconnectivity	CMS	G. Traversi
Perugia	Analog F/E	CMS	M. Menichelli
Pisa	Advanced interconnectivity, photonics, fast output stages	CMS, NA62	F. Palla
TIFPA	System integration and test, photonics	ATLAS	G-F. Dallabetta
Torino	Analog F/E, ASIC integration, TID characterization	CMS	L. Demaria

Compagine:

14 sezioni
≈ 75 Ricercatori,
di cui 18 designer
≈ 20 FTE

Formata in 2 settimane (7-24 luglio 2022), quando in molte sezioni i preventivi erano stati già chiusi

Work Packages
dal proposal

IGNITE, Cagliari – CdS 31 gennaio 2023

WP	Development	Sites (preliminary)	WPR (preliminary)
1	Pixel design (Front-end, ADC, TDC, Logic)	Cagliari, Torino, Pavia, Milano, Perugia, Bologna	S.Cadeddu
2	Readout logic & Output stages	Pisa, Pavia, Milano	R. Beccherle
3	ASIC design Integration & verification	Bologna, Bari, Cagliari, Milano, Torino, Pisa, Pavia	F.Loddo
4	Silicon Photonics	Pisa, Cagliari, Trento	S. Faralli
5	TID study and modeling	Milano B, Torino, Cagliari, Pavia, Padova, Genova	A.Baschirotto
6	HDI techniques	Pisa, Pavia, Cagliari, TIFPA, Genova, Firenze	V. Re
7	Cooling, system Integration and tests	Cagliari, Padova, Pavia, Genova, TIFPA, Firenze, Torino	A.Lai

Conclusioni

1. Partendo da risultati consolidati, abbiamo costruito e attrezzato una palestra per i futuri sviluppi high-tech in fisica delle alte energie, intercettando un forte bisogno sia dal punto di vista dei requisiti sperimentali degli esperimenti di prossima generazione che dell'interesse di una parte importante della comunità di fisici sperimentali

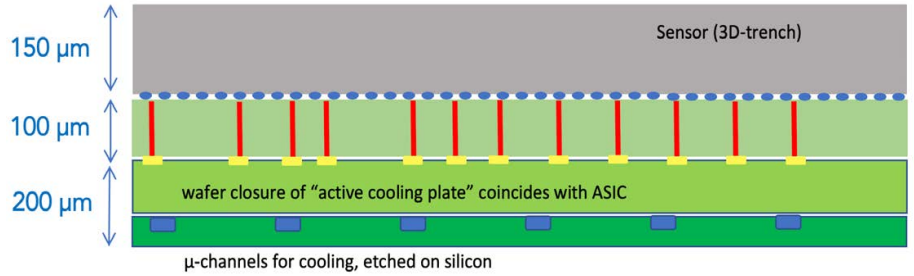
2. Si tratta di una iniziativa nuova, trans-esperimento, trans-commissioni che ha trovato grandi entusiasmi (molti) e forti perplessità (poche)

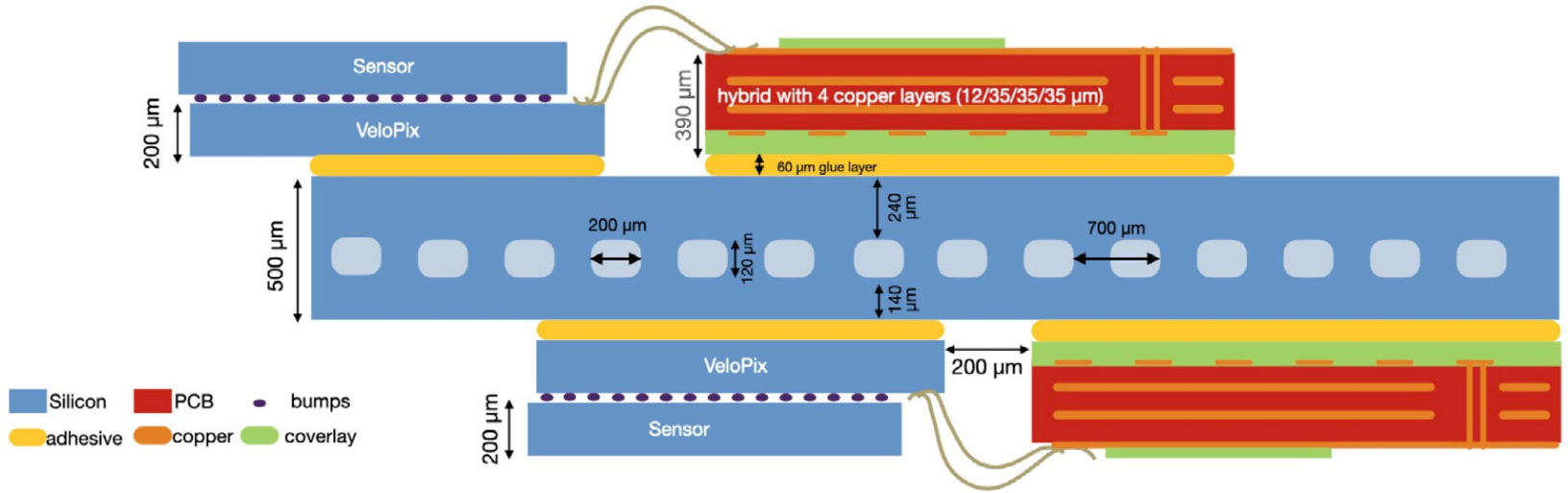
3. Il fuoco è acceso, qualcuno cerca di spegnerlo, è nostro dovere e volontà tenerlo vivo!

Insights

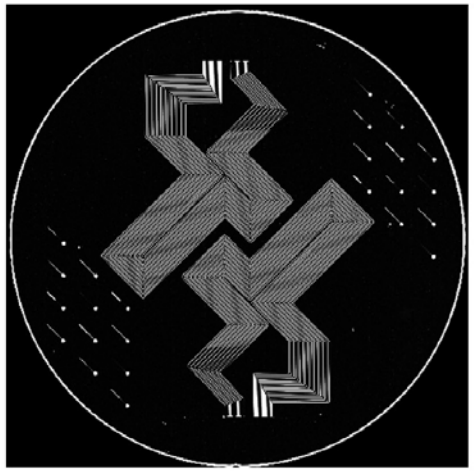
Cooling

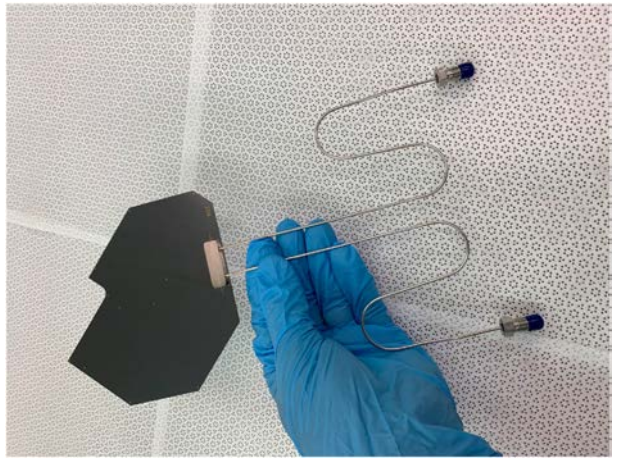
System integration

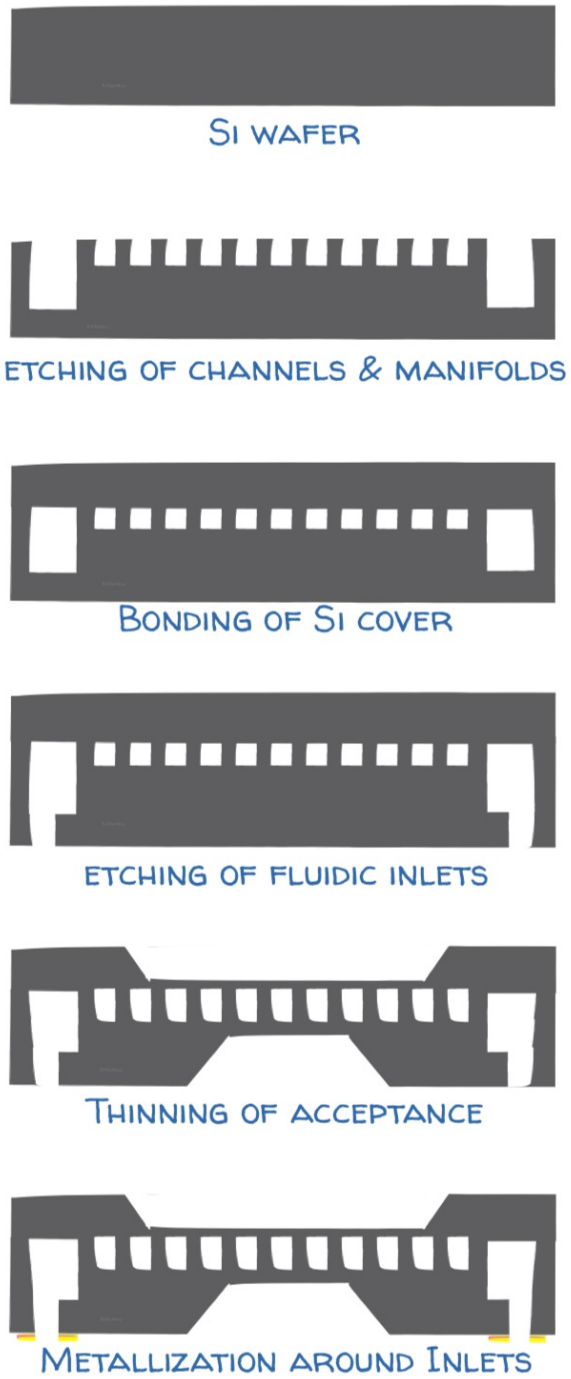




Microchannel cooling for the LHCb VELO Upgrade I
Nuclear Inst. and Methods in Physics Research, A 1039 (2022) 166874

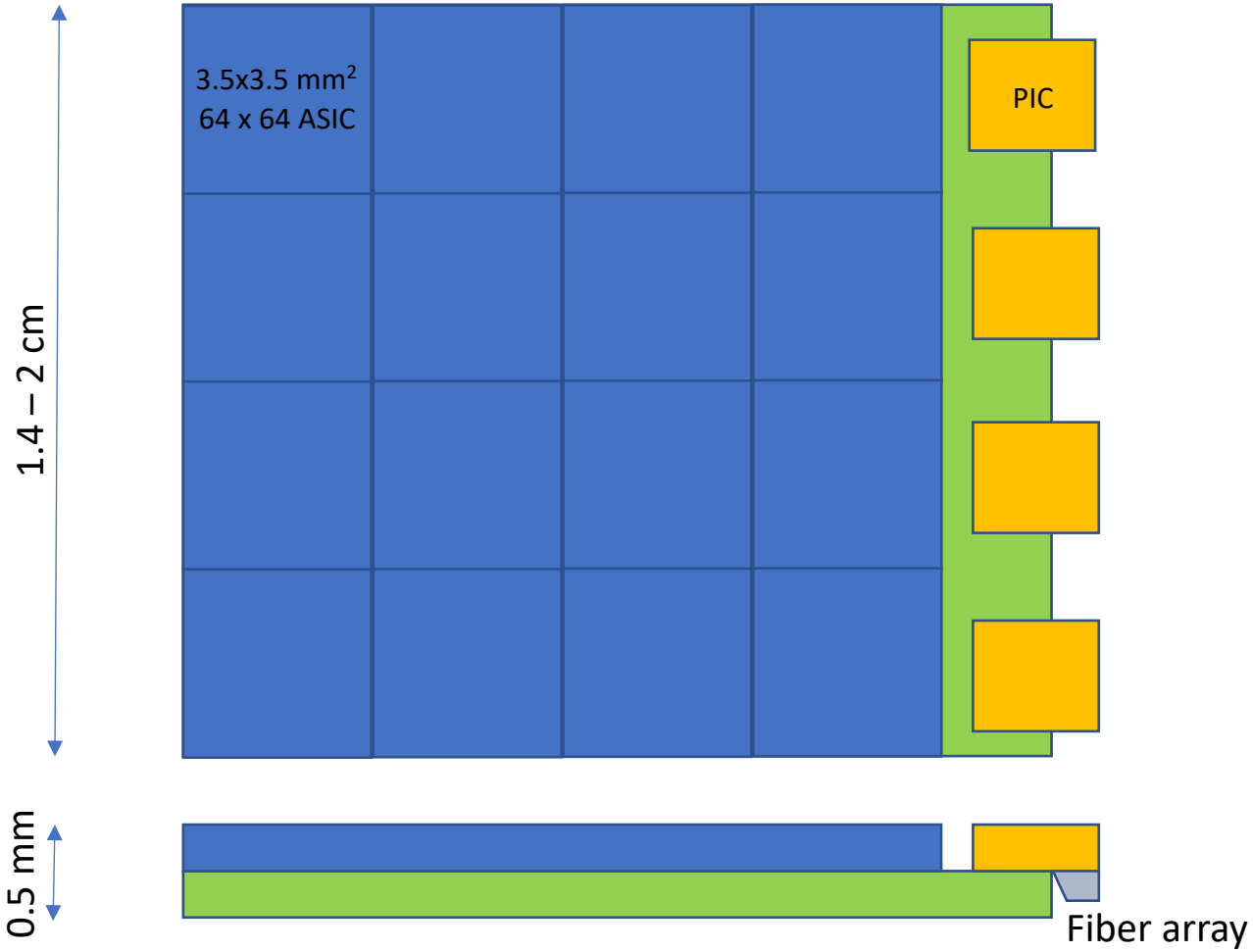




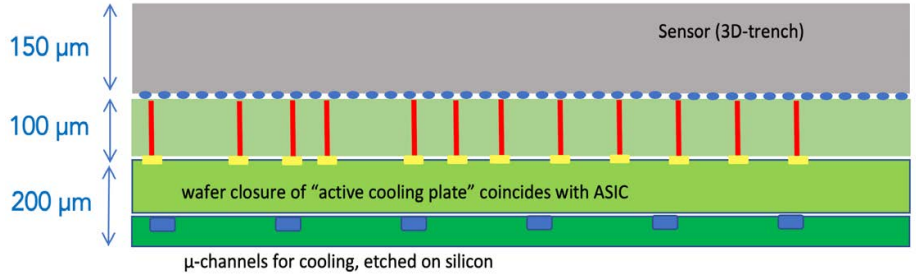


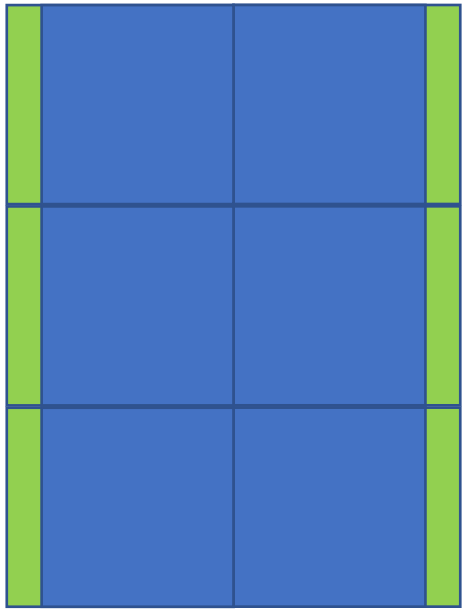
NA62 GTK Vertex 2017 talk

256x256 super-ASIC ~ 1.4x1.4 cm^2, same size of router ASIC
Performing also the role of cooling plate



Basic module.
The size of the ASIC(s) can in principle be larger

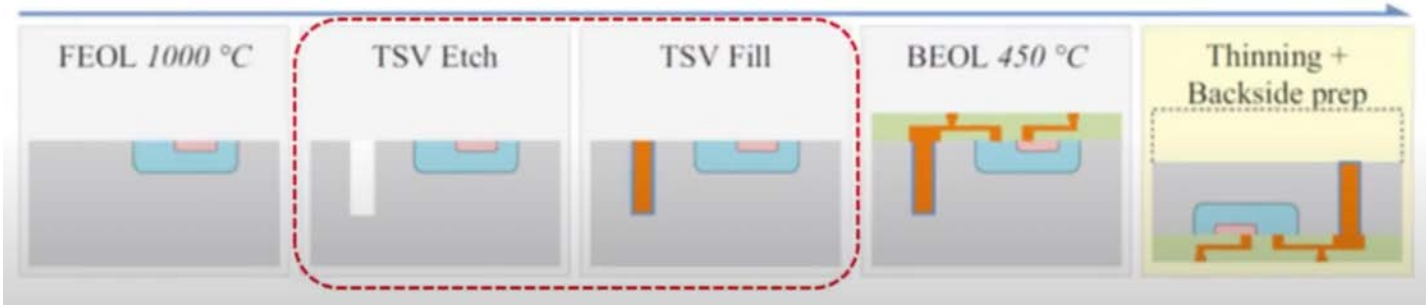




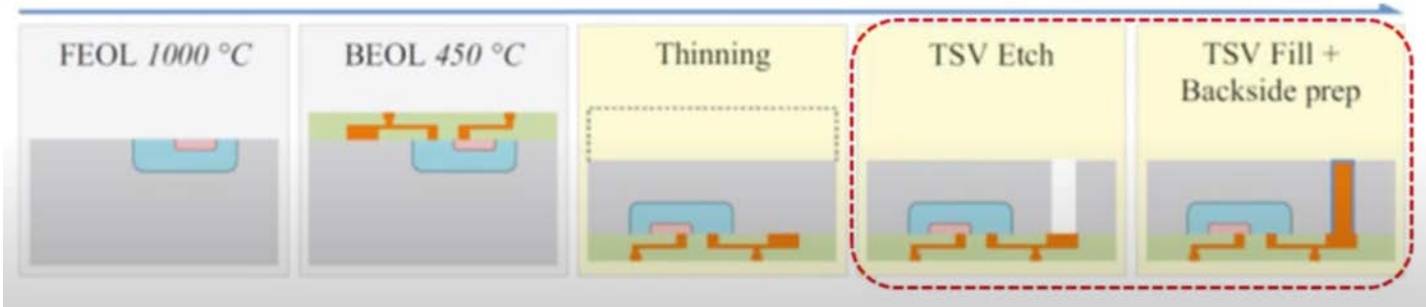
This geometry is not 100% 4-side buttable, but can cover large-enough areas

- Abbiamo programmato una visita ad IZM il 9 febbraio per esplorare questioni di fattibilità e costi
- IZM è un istituto di ricerca, potrebbe essere un partner/fornitore adatto (per es. piccole quantità) ma è sicuramente opportuno e urgente esplorare altre strade
- È urgente verificare anche la fattibilità delle TSV a livello di fonderia per soluzioni via-first/via-middle (TSMC)
- Penserei opportuno provare soluzioni TSV già dal primo prototipo, su integrazioni più semplificate
- È possibile?

Via First (before FEOL process steps)



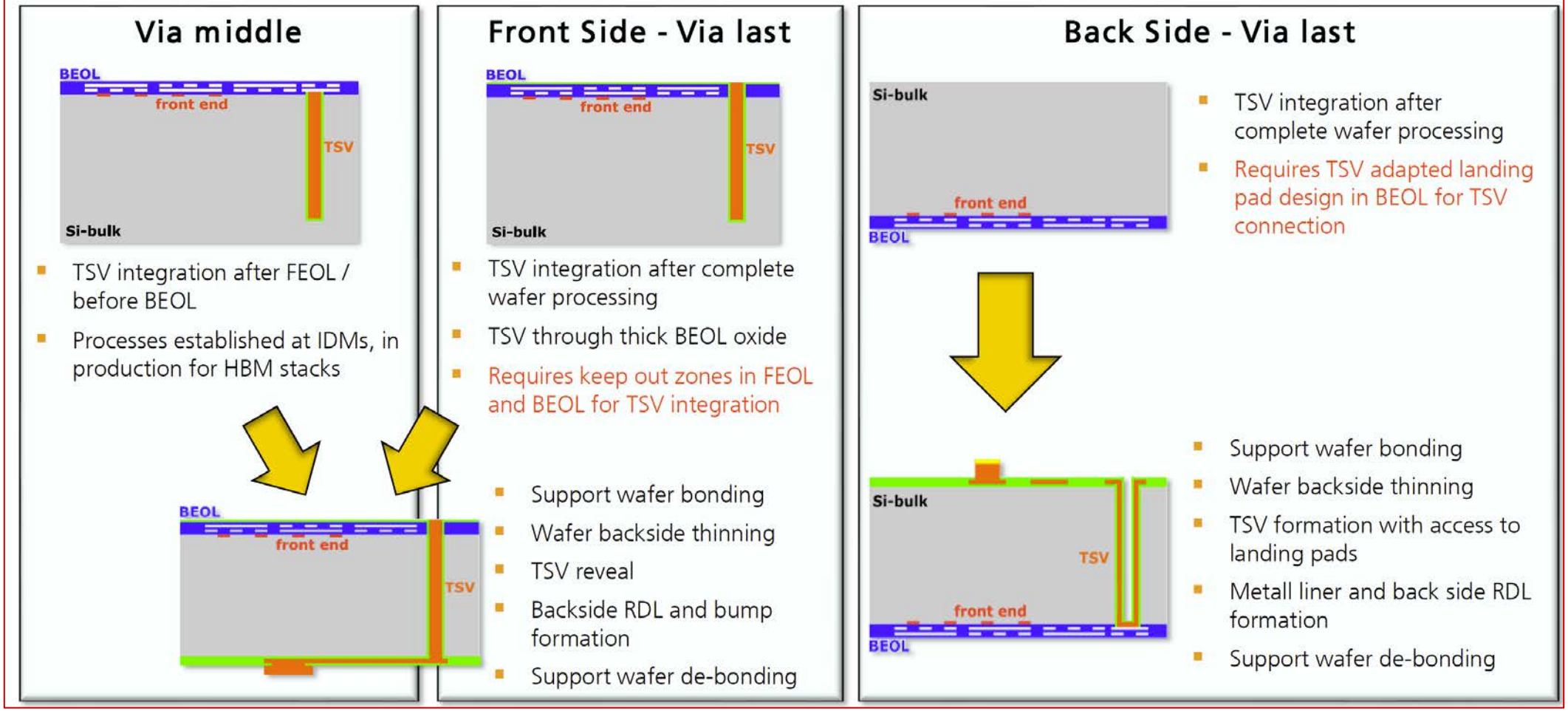
Via Middle (after FEOL, before BEOL process steps)



Via Last (post process steps)

TSV aspect ratio ≈ 10:1

TSV Integration Schemes

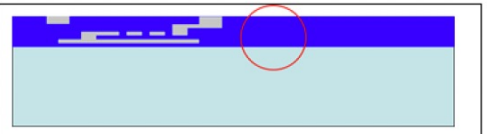


Source: T. Fritzsch, IZM, talk given at Pixel2022 workshop

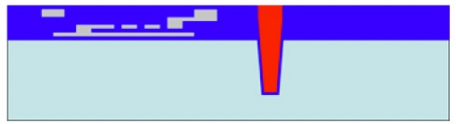
- TSV techniques usually require W2W bonding
- Via first/via middle must be implemented on layout (foundry fabrication). They “reveal” by thinning
- Via Last are implemented after fabrication. They require to be foreseen at layout level (“wide” landing zone) and allow only coarser pitch

Front and Back Side Processes for TSV, RDL and IO formation

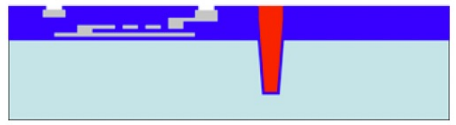
1. **Original wafer condition**
   - Original IO pads opened
   - keep out zones in FEOL and BEOL (red circle)



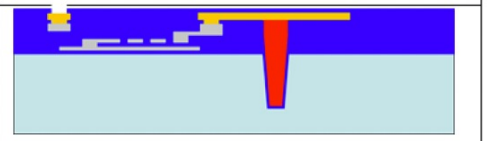
2. **TSV process**
   (Litho mask required-->layer 10 in current TRX8 layout)
   - original IOs pads are covered with passivation layer after TSV process



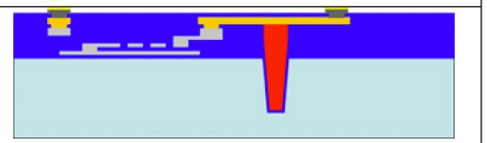
3. **Passivation opening over original IO pads**
   (Litho mask required-->layer 8 in current TRX8 layout)



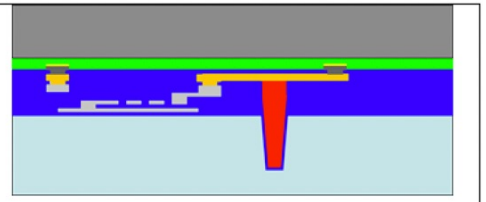
4. **Front side RDL formation (1µm Al)**
   (Litho mask required-->layer 11 in current TRX8 layout)
5. **RDL passivation (1µm CVD Oxide / Nitride)**
   (Litho mask required-->not foreseen in TRX8 layout)



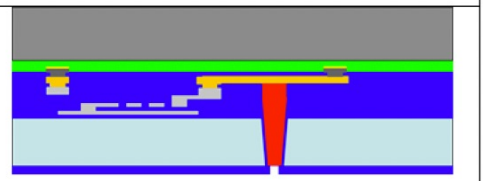
6. **Front side pad metallization**
   (Litho mask required-->not foreseen in TRX8 layout)
   - original IOs can be covered with pad metallization
   - pad metallization to be located at all positions were passivation is opened
   - pad formation on top of TSVs not allowed



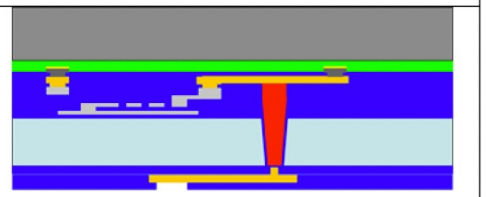
7. **Temporary carrier bonding**



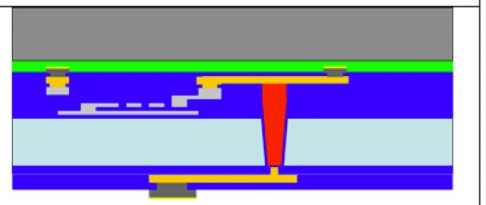
8. **Back grinding / TSV reveal**
9. **Back side passivation (1µm CVD Oxide / Nitride)**
   (Litho mask required-->layer 9 in TRX8 layout)



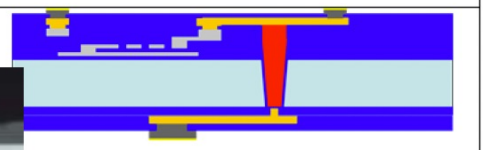
10. **Back side RDL (1µm Al)**
    (Litho mask required-->layer 21 in TRX8 layout)
11. **RDL passivation (1µm CVD Oxide / Nitride)**
    (Litho mask required-->not foreseen in TRX8 layout)



12. **Back side pad metallization deposited**
    (Litho mask required-->not foreseen in TRX8 layout)

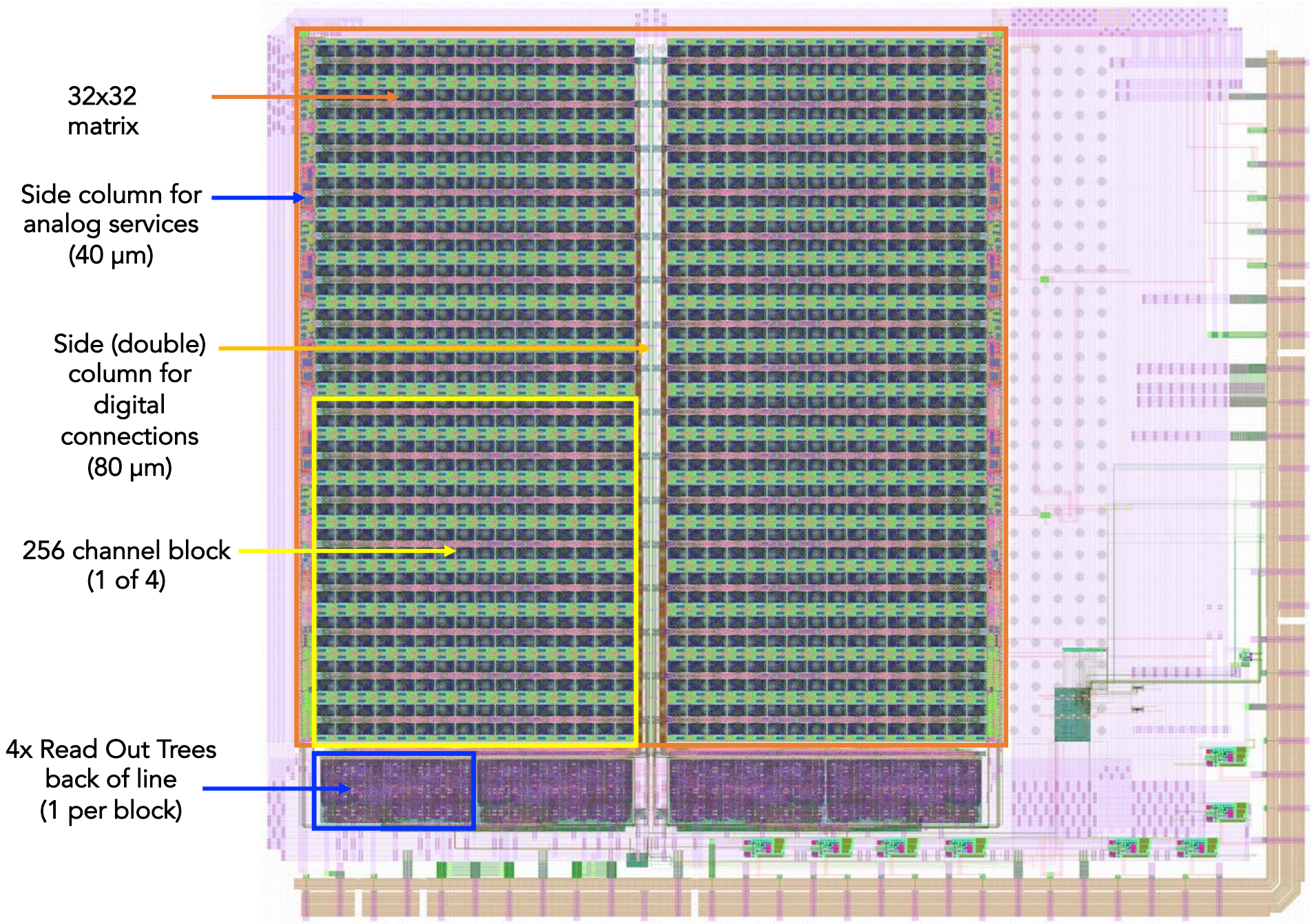


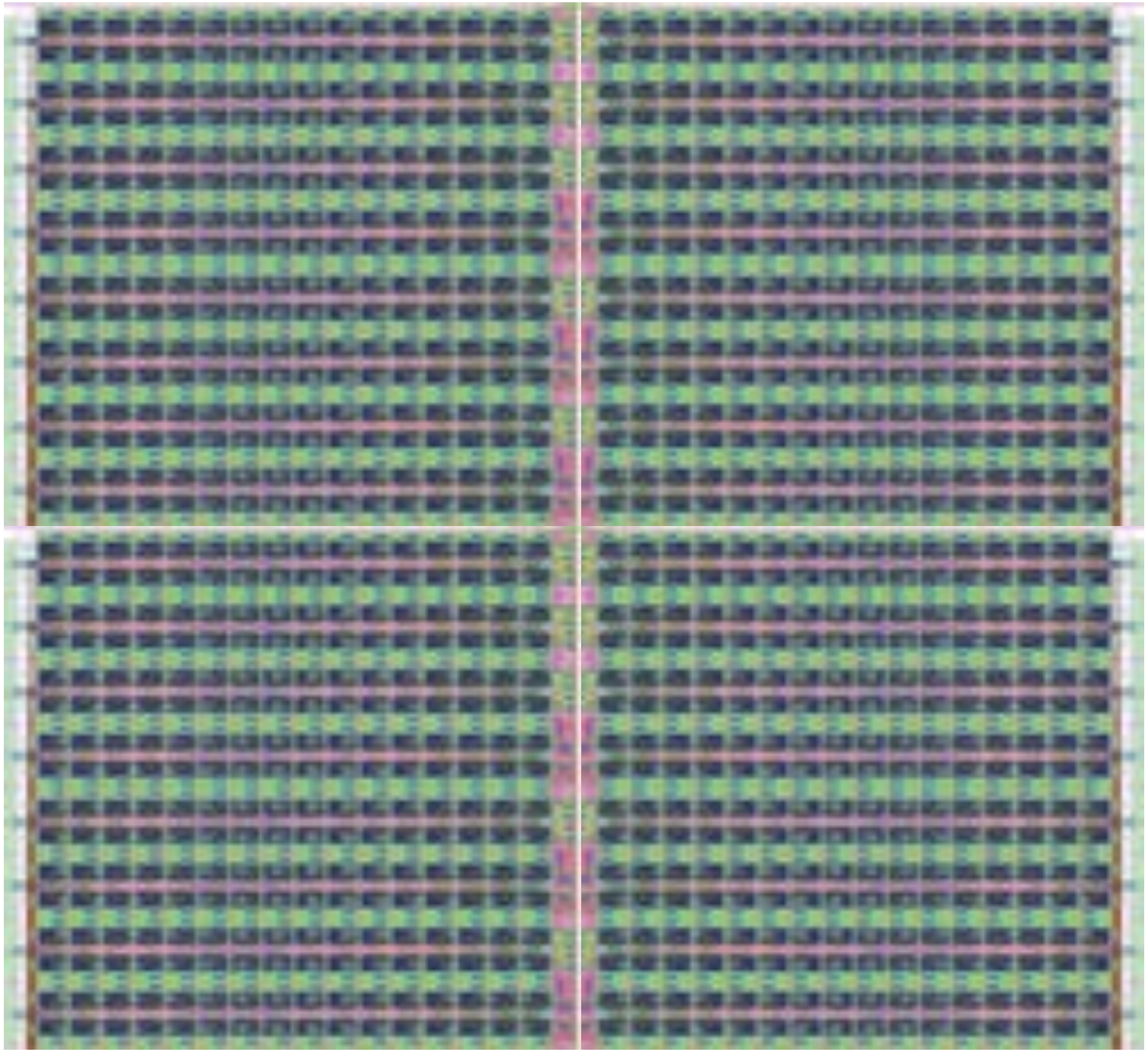
13. **Temporary carrier de-bonding**



Source: T. Tekin, IZM, talk given at EPIC 2022 workshop
See: https://epic-assoc.com/events/epic-meeting-on-cmos-compatible-integrated-photonics-at-imec/

Fraunhofer IZM


32x32
matrix
Side column for
analog services
(40 µm)
Side (double)
column for
digital
connections
(80 µm)
256 channel block
(1 of 4)
4x Read Out Trees
back of line
(1 per block)



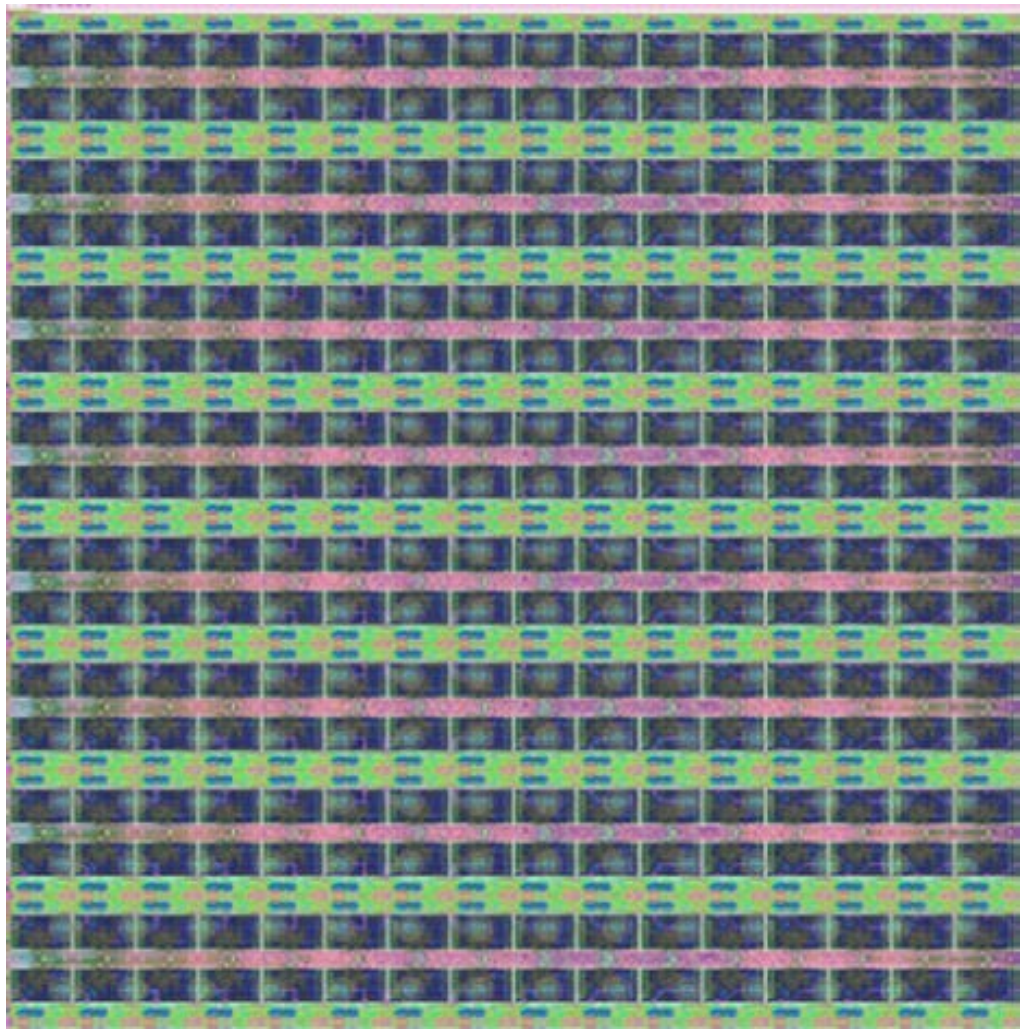
32x32
x&y pitch ≤ 50 µm

In una ottica LHCb-U2, questo blocco produce (stima su **rate medio**, Scenario A):

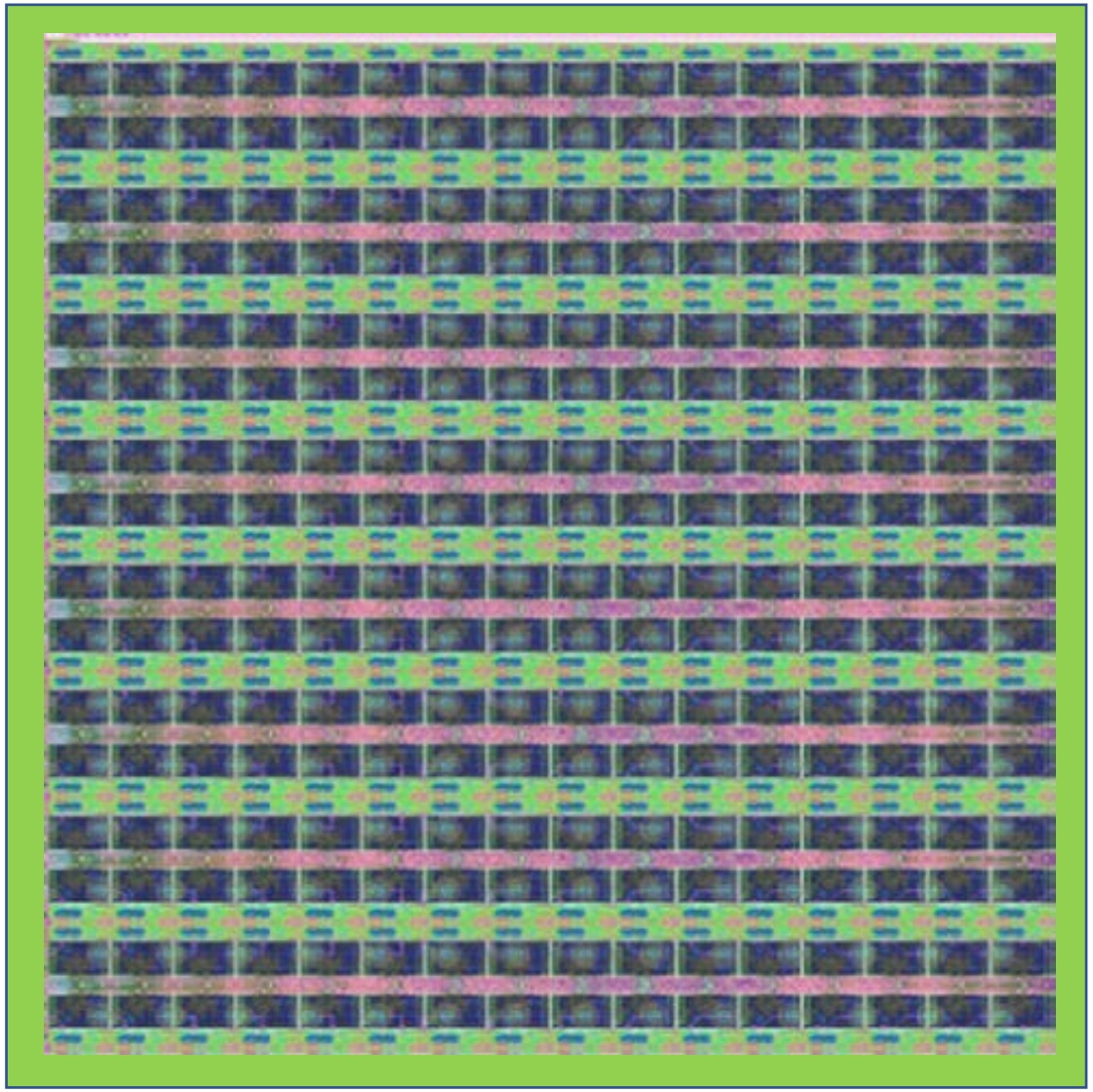
1 hits/BX x 2 (cluster size) x 30 MHz (BX) x 44 bits/hit = 2.64 Gbps

Margine di sicurezza 1.5 (rate fluct.)
→ **≈ 4 Gbps**

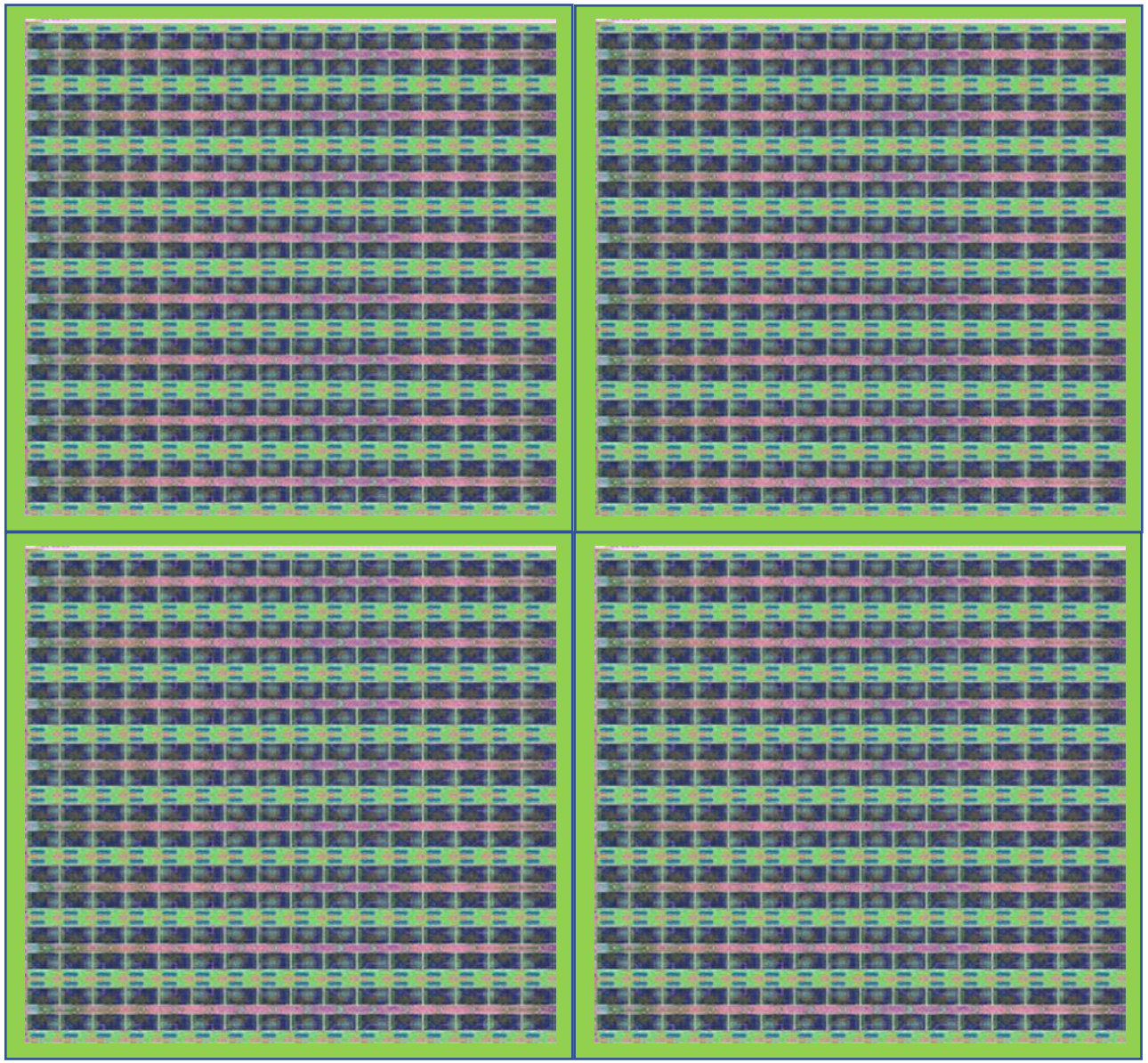
44 bit:
16 address (si può diminuire)
9 Bxid
10 TDC
6 (8) ToT
3 spare/additional info (e.g. cluster size)



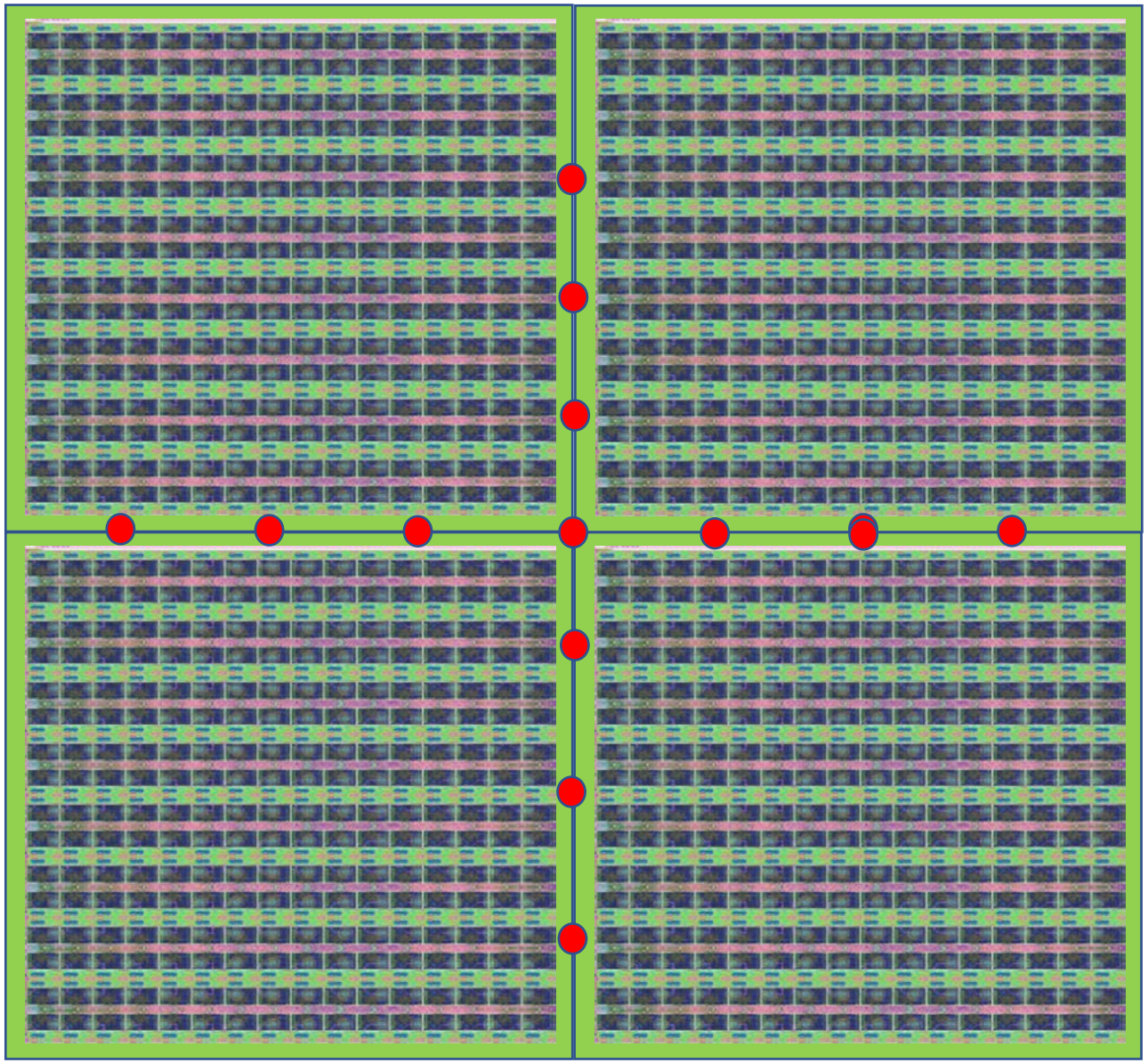
16x16 50x50 pixel pitch
Possible different size (match with 0.9 shrinking?)



Possible 40 µm-wide framework



80 µm lanes (x & y)

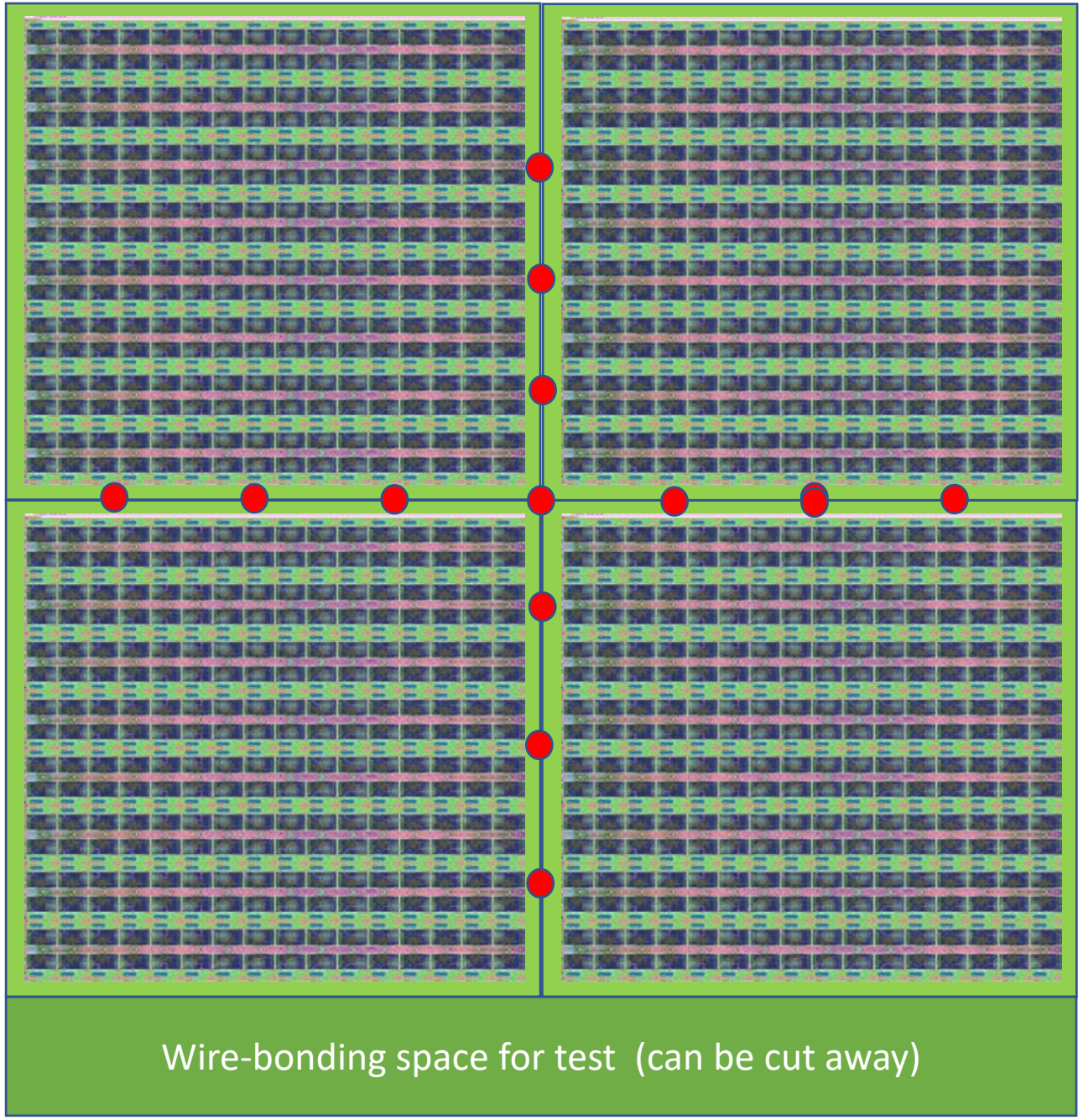


- TSV via last? (can they be large enough?)

80 µm lanes (x & y)

Clock
Power
Data output
Slow controls
Analog services?

Packaged in this version on an interposer to implement a SiP?

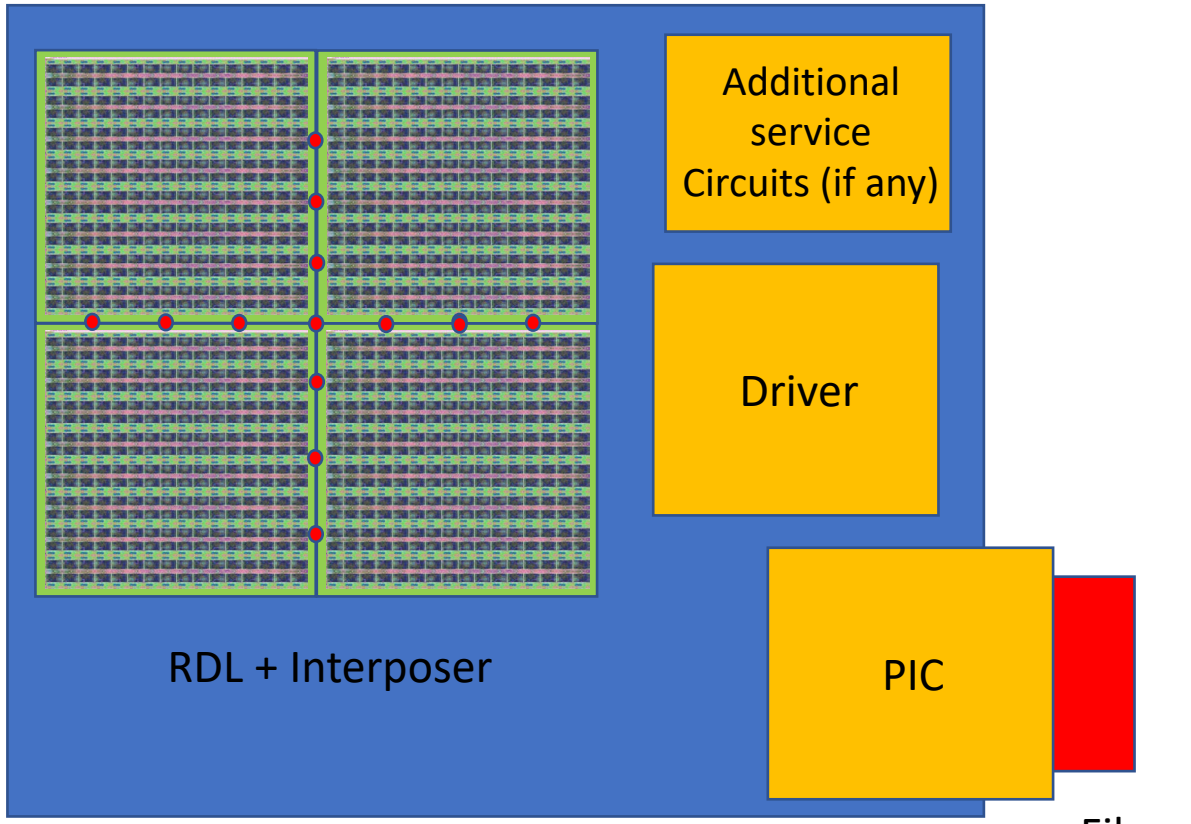


- TSV via last? (can they be large enough?)

80 µm lanes (x & y)

Clock
Power
Data output
Slow controls
Analog services?

- **Packaged in this version on an interposer to implement a SiP?**
- **A version for preliminary tests (before integration)**



System in Package
One package (BGA ?)

Advantages:

- Minimum work possible with respect to an already–developed ASIC (Timespot1)
- Lower ASIC cost
- Feasibility within 2023/24
- Compactness

It tests:

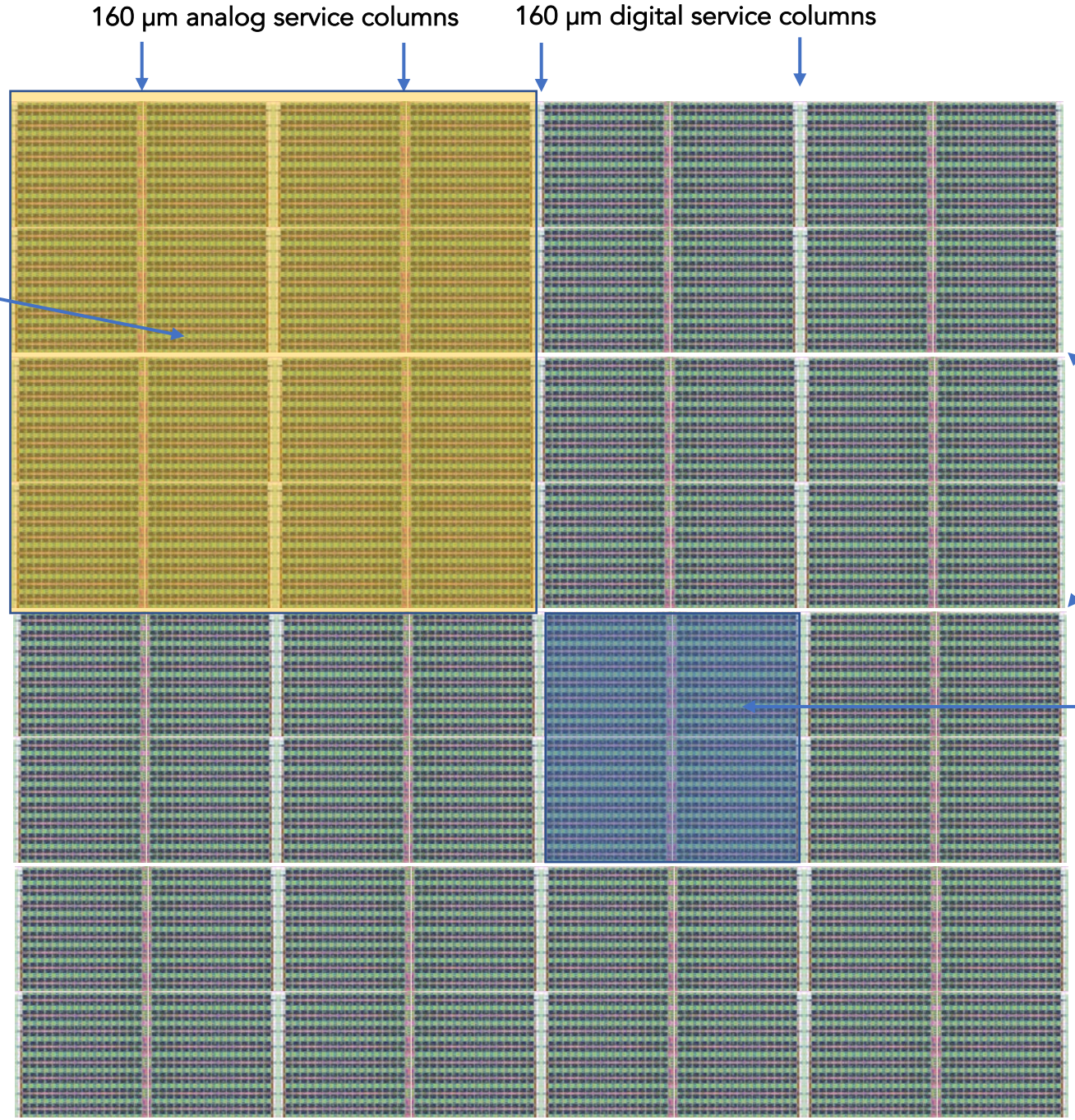
- Modularity of pixel matrix
- Global line distribution
- Use of TSV in I/O connection
- Interface with Driver and PIC

Moreover:

- We profit to correct bugs and re-test it

It does not test:
Solutions for final integration especially concerning :

- ASIC vs Driver and PIC
- Cooling system



128x128 7x7 mm² ≈ 300 k€

or

64x64 3.5x3.5 mm² ≈ 75 k€

?

The whole structure is 4-side buttable 128x128 pixels corresponds to a ≈ 7x7 mm² on the sensor side