1.1 Silicon Vertex Tracker

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1.1.1 Electronic Readout

The front-end processing of the signals from the silicon strip detectors will be performed by custom-designed ICs mounted on hybrid circuits that distribute power and signals, and thermally interface the ICs to the cooling system. As discussed below, the very different features of inner (Layer 0 and 1) and outer layers of the SVT set divergent requirements to the readout chips, which most probably makes it necessary to develop two distinct integrated circuits. Generally speaking, both types of ICs will consist of 128 channels, each connected to a detector strip. The signals from the strips, after amplification and shaping will be compared to a preset threshold. If a signal exceeding the threshold is detected, a 3-4 bit analog information about the signal amplitude will be provided by an ADC: this will mostly serve for calibration and monitoring purposes in the innermost layers, whereas in outer layers it will be essential for dE/dx measurements**.** The dimensions of the readout IC are expected to be about 7.5 x 4.5 mm^2, and the power dissipation will be about 1 mW/channel. For each channel with a signal above threshold, the strip number, the amplitude information, the chip identification number and the related time stamp will be stored inside the chip waiting for a trigger signal for a time corresponding to the trigger latency (about 10 us). When a trigger is received, data will be read out and transmitted off chip, otherwise they will be discarded. The data output from the microstrip detector will be sparsified, i.e. will consist only of those channels generating a hit. The readout integrated circuits must remain functional up to 5 times nominal background

1.1.2 Readout chip

Requirements

The microstrip electronics must ensure that the detector system operates with adequate efficiency, but also must be robust and easy to test, and must facilitate testing and monitoring of the microstrip sensors. AC coupling is assumed between the strips and the readout electronics.

- **Mechanical Requirements:** 128 channels per chip, with 50 um channel and input bonding pads pitch (limits on chip size?)
- **Operational Requirements:**

  Operating temperature: < 40 °C

  Radiation tolerance: > 5 Mrad/year

  Power dissipation: < 1 mW/channel

- **Analog Resolution:** The front-end chips have to provide a 3-4 bit analog information about the charge collected in the detector, which will be also used for calibrating and monitoring the system.
- **Dynamic range:** The front-end chips must accept signals from either P and N-side of the strip detectors. A linear response of the analog processing section is required from a minimum input charge of 0.75 fC to a maximum input charge of 5 fC.
- **Efficiency:** At design luminosity, the microstrip readout must have a hit efficiency of at least 99% **(or 95 % ???)** during its entire operational lifetime. This includes any loss of data by readout electronics or readout dead time.
- **Readout bandwidth:** Data coming out of the chip will be substantially reduced by operating in a triggered mode.
- **Radiation Tolerance:** All the components of the microstrip readout system must remain operational up to 10 years of SuperB running at the nominal luminosity.
- **Peaking Time:** The constraints for the peaking time of the signal at the shaper output are dictated by different needs in inner and outer layers. In Layer 0, the high occupancy due to background and the need to avoid pulse overlap and consequent hit inefficiencies set the maximum peaking time at t_P = 25 ns, which also allow for a high timing resolution (see below). In the external layers, where background hit frequency is much smaller and where strips are longer and have a larger capacitance, the peaking time will be mostly determined by the need of reducing series noise contributions and has to be in the range of 1 μs.
- **Signal-to-Noise Ratio**: Concerning the signal, this requirement has to take into account the different thickness of silicon detectors in inner (200 um) and outer (300 um) layers, as well the signal spread among various strips that depends on the track angle inside detectors and that, again, may vary in different SVT layers. Noise–related parameters (strip capacitance and distributed resistance) also sizably vary across the SVT. A signal-to noise ratio of 20 has to be ensured across the whole SVT and should not increase significantly after irradiation. Here are the two extreme cases:

  Layer 0 striplets: ENC ~ 700 e^- at C_D = 10 pF and at t_P = 25 ns

  Layer 5 strips: ENC ~ 1000 e^- at C_D = 30 pF and at t_P = 1 us
- **Threshold and Dispersion:** Each microstrip channel will be read out by comparing its signal to a settable threshold around 0.2 MIP**.** Threshold dispersion must be low enough that the noise hit rate and the efficiency are degraded to a negligible extent. Typically, this should be 400 electrons at most and should be stable during its entire operational lifetime.
- **Comparator Time Resolution:** The comparator must be fast enough to guarantee that the output can be latched in the right time stamp period.
- **Time Stamp:** 50 ns time stamp resolution is required for the inner layers, increasing to a maximum of 1 us in the outer layers to match the pulse shaping times
- **Chip clock frequency:** Two main clocks will be used inside the readout chip, the time stamp clock (20 MHz) and the readout clock (100 MHz).
- **Masking, Kill and Inject:** Each micro-strip channel must be testable by charge injection to the front-end amplifier. By digital control, it shall be possible to turn off any micro-strip element from the readout chain.

- **Maximum data rate:** Simulations show that machine-related backgrounds dominta the overall rates. At nominal background levels, the maximum hit rate per strip is…
- **Deadtime limits:** The maximum total deadtime of the system must not exceed….
- **Trigger specifications:** The trigger has a nominal latency of 10 us, a maximum jitter of 0.5 us, and the minimum time between triggers is….The maximum Level 1 Trigger rate is ….
- **Cross-talk:** Must be less than 2 %
- **Control of Analog Circuitry on Power-Up:** Upon power-up, the readout chip shall be operational at default settings.
- **Memory of Downloaded Control of Analog Circuitry:** Changes to default settings shall be downloadable via the readout chip control circuitry, and stored by the readout chip until a new power-up cycle or additional change to default settings.
- **Read-back of Downloadable Information:** All the data that can be downloaded also shall be readable. This includes data that has been modified from the default values and the default values as applied on each chip when not modified.
- **Data Sparsification:** The data output from the microstrip detector shall be only of those channels that are above the settable threshold.
- **Microstrip output data content:** The microstrip hit data must include the time stamp, chip identification number, and the microstrip hits (strip number and relevant signal amplitude) for that time stamp.

Readout Chip Implementation

The SuperB SVT readout chips are mixed-signal integrated circuits in a 130 nm CMOS technology and are being designed to comply with the requirements discussed above. Each chip comprises 128 analog channels, each consisting of a charge-sensitive preamplifier, a unipolar semi-Gaussian shaper and a hit discriminator. A symmetric baseline restorer is included to achieve baseline shift suppression. When a hit is detected, a 3-4 bit analog-to-digital conversion will be performed by a Flash ADC or by means of a Time-Over-Threshold (TOT) detection. The hit information will be buffered until a trigger is received; together with the hit time stamp, it will be then transferred to an output interface, where data will be serialized and transmitted off chip on output LVDS lines. An n-bit data output word will be generated for each hit on a strip. A programming interface accepts command and data from a serial input bus and programmable registers are used to hold input values for DACs that provide currents and voltages required by the analog section. These registers have other functions, such as controlling data output speed and selecting the pattern for charge injection tests.
Given the very different requirements of inner and outer layers, in terms both of detector parameters and hit frequency, two different chips will be designed; they will be based on a same data protocol, but will be optimized for operation at different clock frequencies.
Fig. 1.1.1 shows the chip block diagram. The block diagram of the analog channel is shown in Fig. 1.1.2.

Fig. 1.1.1 Chip block diagram. Arrows represent control and data flow.

Fig. 1.1.2 Analog channel block diagram.

R&D

The R&D to support the development of the SuperB strip readout chips has begun in 2011. The chosen technology for integration is a 130 nm CMOS process: this has an intrinsically high degree of radiation resistance, which can be enhanced with some proper layout prescriptions such as enclosed NMOS transistors and guard rings. There is a large degree of experience with mixed-signal design in this CMOS node that was gained in the last few years inside the HEP community.

The readout architecture was tested with realistic data created by Monte Carlo analysis of the interaction region. Verilog simulations indicate the chip will be able to operate with the required 99% (or 95 % ???) efficiency.

The analog section of the chip is optimized from the standpoint of noise, comparator threshold dispersion and sensitivity to variations of process parameters. It is possible to select the peaking time of the signal at the shaper output (25 - 100 ns for inner layers, 400 ns – 2 us for outer layers) by changing the value of capacitors in the shaper. In this way the noise performances of the chip can be optimized according to the signal occupancy, preserving the required efficiency.

The first prototype was submitted in December 2011. This prototype contains analog channels with the same structure as the final chip. Figures 1.1.3 and 1.1.4 show the simulated signal waveforms at the shaper output and the Equivalent Noise Charge ENC as a function of the detector capacitance C_D. Table 1 shows the main simulated parameters of the analog section.

In 2012, the submission of a prototype including a small scale version of the readout architecture is foreseen.
The submission of a full-scale, 128-channels chip prototype is scheduled in late 2013. This version will have the full functionality of the final production chip.

Fig. 1.1.3 Waveforms at the output of the shaper at a peaking time setting t_P = 25 ns.

Fig. 1.1.4 Equivalent Noise Charge ENC as a function of the detector capacitance C_D at a peaking time setting t_P = 25 ns.

Power dissipation
Preamplifier input device
Charge sensitivity
Comparator rms threshold dispersion
Signal peaking time at the shaper output
Equivalent Noise Charge at C_D = 20 pF

Table 1. Parameters of the analog section of the first prototype.

References

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