TRIGGER module

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CYGNO DAQ meeting
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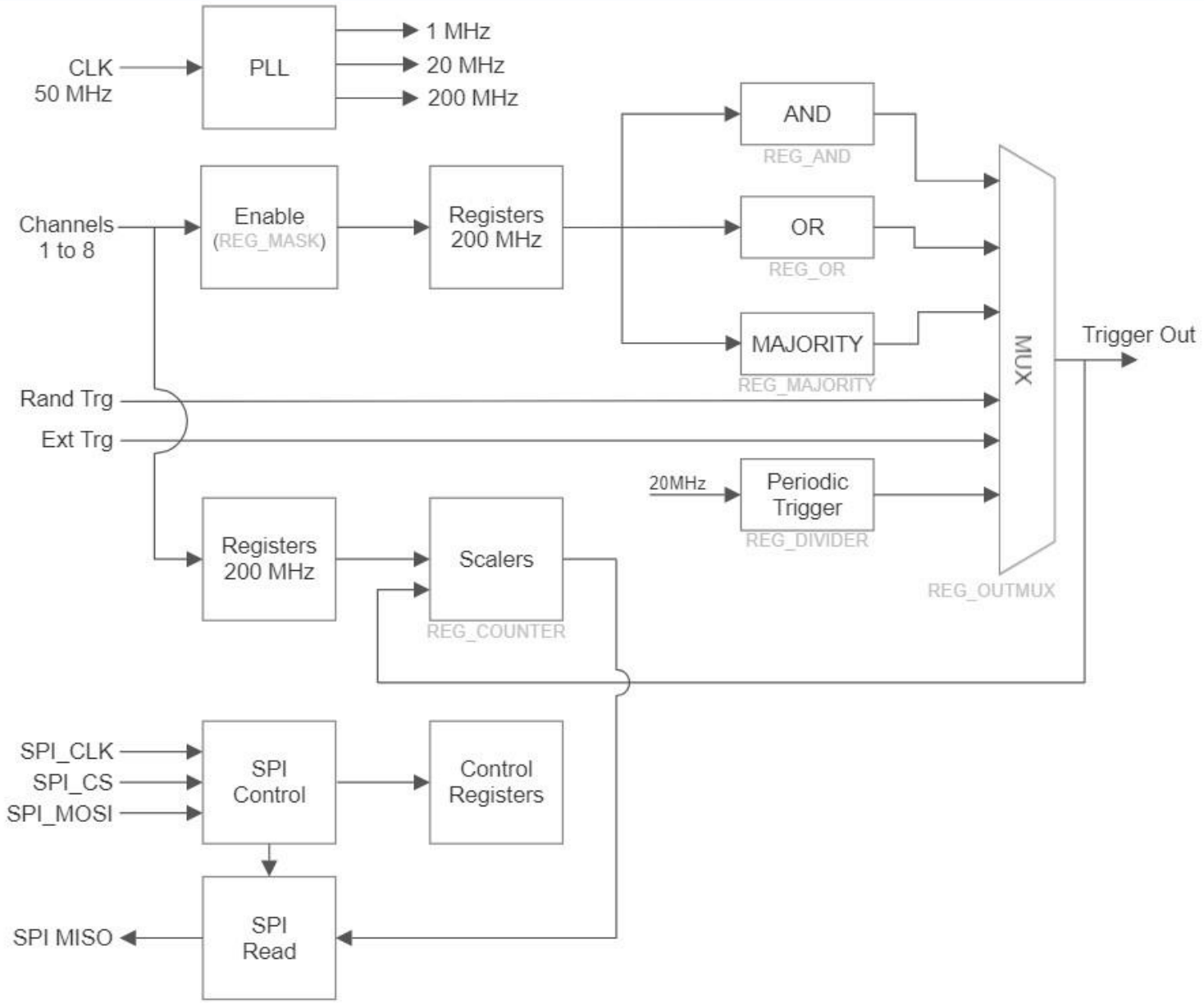
FPGA design overview



What need to be done?

- **Inputs:**
  - ✓ 4 PMT channels (expected rate 1 kHz, with some tolerance 0.2-50 kHz)
  - ✓ External clock (needs to use a specific pin, hardware modification needed in Rome's module)
  - ✓ Gate DAQ server (signal 'gate_in' - pin allocated but how the signal should be used?)
  - ✓ Camera exposure (signal 'camera_in' - pin allocated, but how the signal should be used?)
  - ✓ External Trigger input (signal 'trigger_in', selected when REG_OUTMUX=5)

- **Trigger logic:** the trigger is in AND with (Gate DAQ server) AND (Camera exposure)
  - ✓ Majority
  - ✓ And
  - ✓ Or
  - ✓ Periodic (10 - 100 Hz)
  - ✓ Random

- **Outputs:**
  - ✓ Trigger (~5-13 Hz at LIME/LNGS, 14/02/23)
  - ✓ Busy
  - ✓ Clock (either the external or an internal one)

** In BLUE: to be implemented*

What need to be done?

- **Trigger Veto**: configurable time window in the FPGA to block any trigger in a given time after the previous trigger (in the range of microseconds). Starting design with options: 10us, 25us, 50us, 100us (by Herman).
  IN PROGRESS…

- **Counters**: with a configurable time base (in the range of 0.1-10 Hz), for each input, output, and trigger logic. We should keep track of all signals in a run. Ideally, the FPGA counts in a given time base, stops, sends the data to the raspberry pi, resets the counter, and starts again. Firmware done. Tested and working for 16 bits counters on PMT channels 1 to 4 and 8 bits on Trigger output. Four configurable time bases:
  - ✓ 0.5 s (REG_COUNTER=0),
  - ✓ 1.0 s (REG_COUNTER=1),
  - ✓ 10.0 s (REG_COUNTER=2),
  - ✓ 100.0 s. (REG_COUNTER=3).

- Data payload: counters and time stamp

** In BLUE: to be implemented*

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New FPGA module under study: **DE10-Nano**

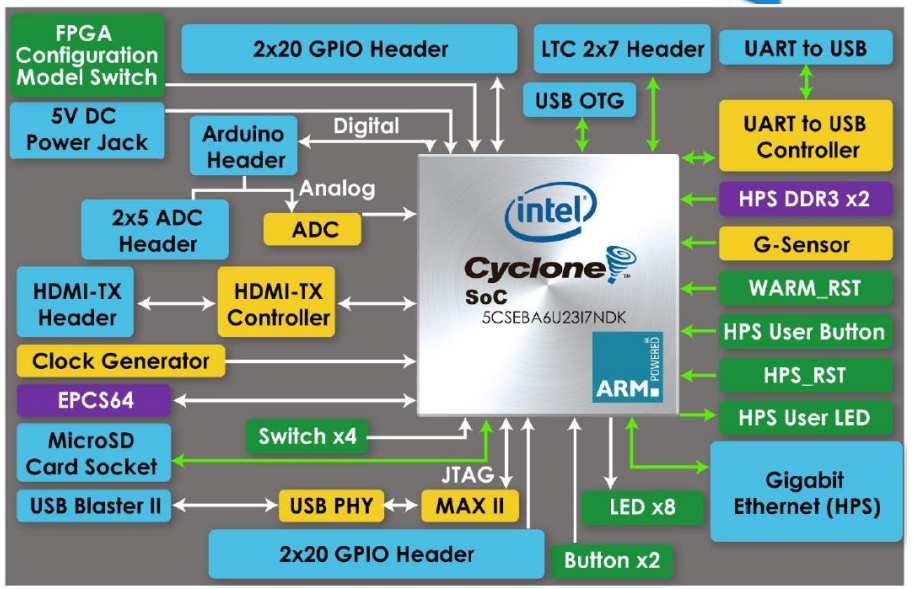
■ FPGA

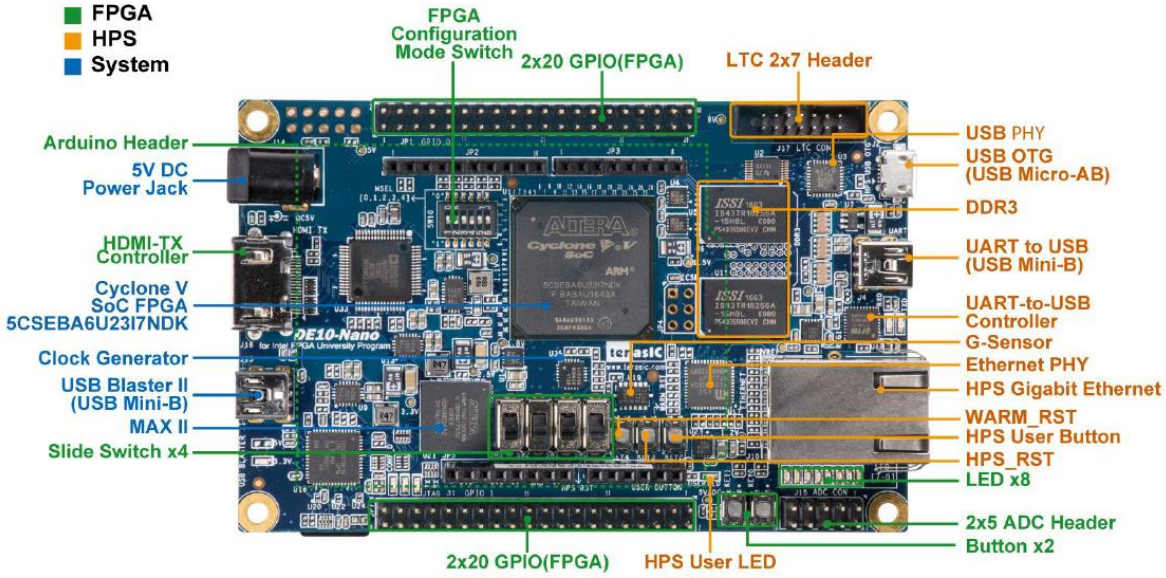
- Cyclone® V SE 5CSEBA6U23I7NDK device
- Serial configuration device – EPCS64
- USB-Blaster II onboard for programming; JTAG Mode
- 2 push-buttons
- 4 slide switches
- 8 green user LEDs
- Three 50MHz clock sources from the clock generator
- Two 40-pin expansion header ⟶ up to 36 I/Os
- One Arduino expansion header (Uno R3 compatibility), can connect with Arduino shields.
- One 10-pin Analog input expansion header. (shared with Arduino Analog input)
- A/D converter, 4-wire SPI interface with FPGA
- HDMI TX, compatible with DVI v1.0 and HDCP v1.4

■ HPS (Hard Processor System)

- 800MHz Dual-core ARM Cortex-A9 processor
- 1GB DDR3 SDRAM (32-bit data bus)
- 1 Gigabit Ethernet PHY with RJ45 connector
- port USB OTG, USB Micro-AB connector
- Micro SD card socket
- Accelerometer (I2C interface + interrupt)
- UART to USB, USB Mini-B connector
- Warm reset button and cold reset button
- One user button and one user LED
- LTC 2x7 expansion header

no need of Raspberry Pi





New FPGA module under study: **DE10-Nano**

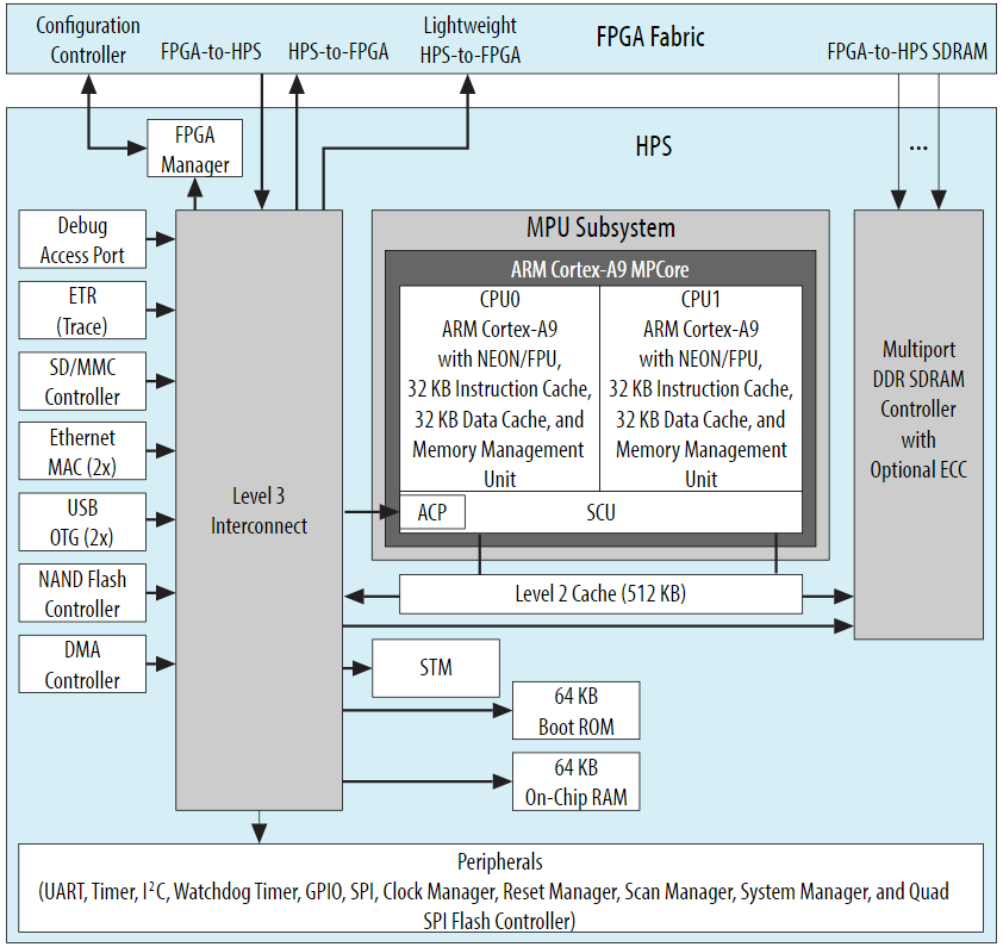
HPS-FPGA AXI Bridges

The HPS–FPGA bridges, which support the Advanced Microcontroller Bus Architecture (AMBA®) Advanced eXtensible Interface (AXI™) specifications, consist of the following bridges:

- FPGA-to-HPS AXI bridge - a high-performance bus supporting 32, 64, and 128 bit data widths that allows the FPGA fabric to issue transactions to slaves in the HPS.
- HPS-to-FPGA AXI bridge - a high-performance bus supporting 32, 64, and 128 bit data widths that allows the HPS to issue transactions to slaves in the FPGA fabric.
- Lightweight HPS-to-FPGA AXI bridge - a lower latency 32 bit width bus that allows the HPS to issue transactions to slaves in the FPGA fabric. This bridge is primarily used for control and status register (CSR) accesses to peripherals in the FPGA fabric.

The HPS–FPGA AXI bridges allow masters in the FPGA fabric to communicate with slaves in the HPS logic, and vice versa. For example, the HPS-to-FPGA AXI bridge allows you to share memories instantiated in the FPGA fabric with one or both microprocessors in the HPS, while the FPGA-to-HPS AXI bridge allows logic in the FPGA fabric to access the memory and peripherals in the HPS.

Each HPS–FPGA bridge also provides asynchronous clock crossing for data transferred between the FPGA fabric and the HPS.



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New FPGA module under study: **DE10-Nano**

Linux Xfce Desktop
(kernel 4.1.33-ltsi-altera)
running on Dual-core ARM