WP2 status & activities: MiniASIC Design

Haspide General Meeting

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03/02/2023

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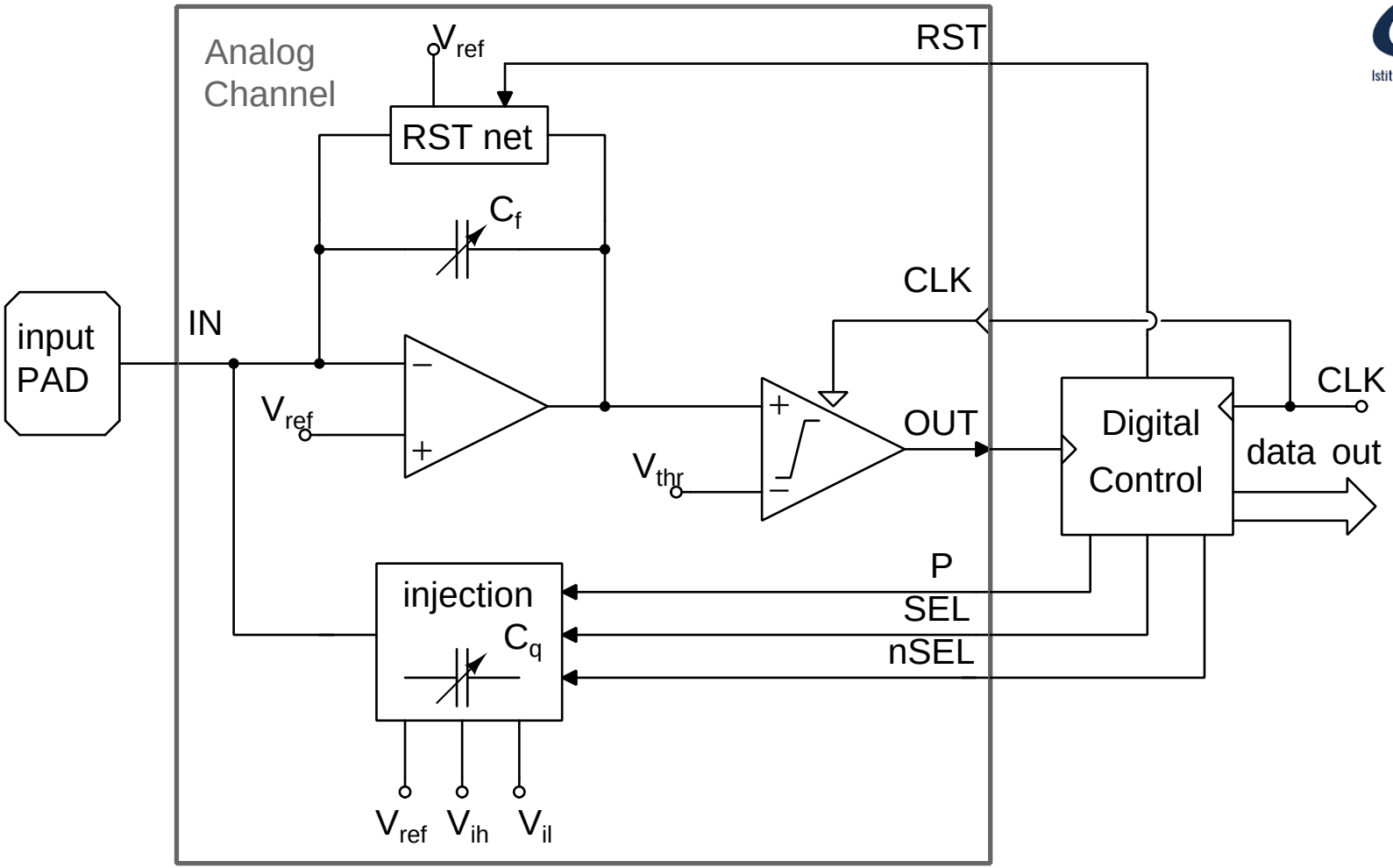
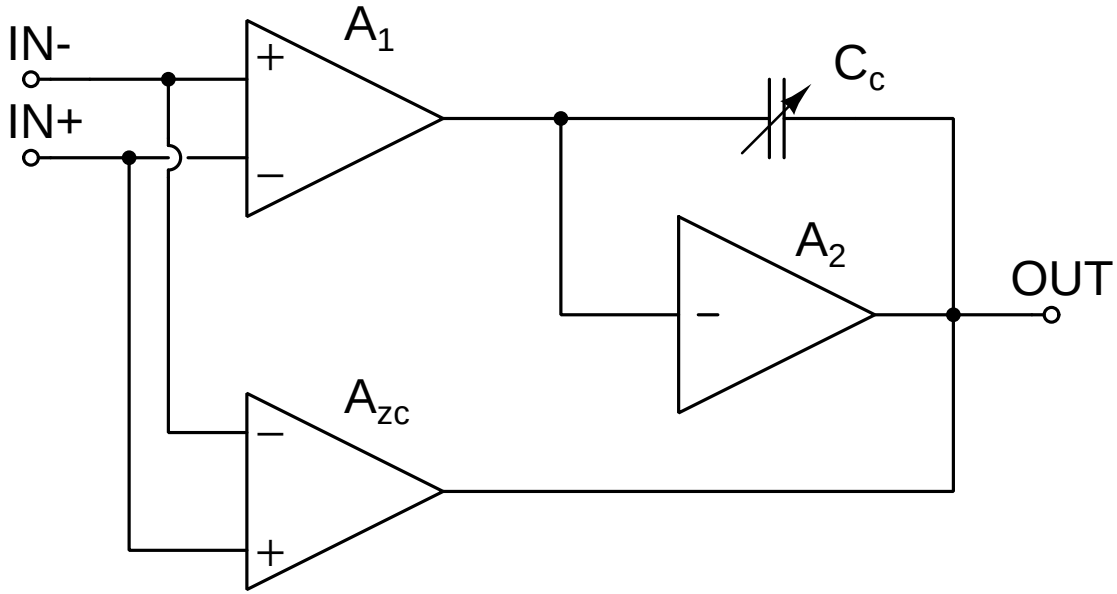
Reminder: Channel Architecture



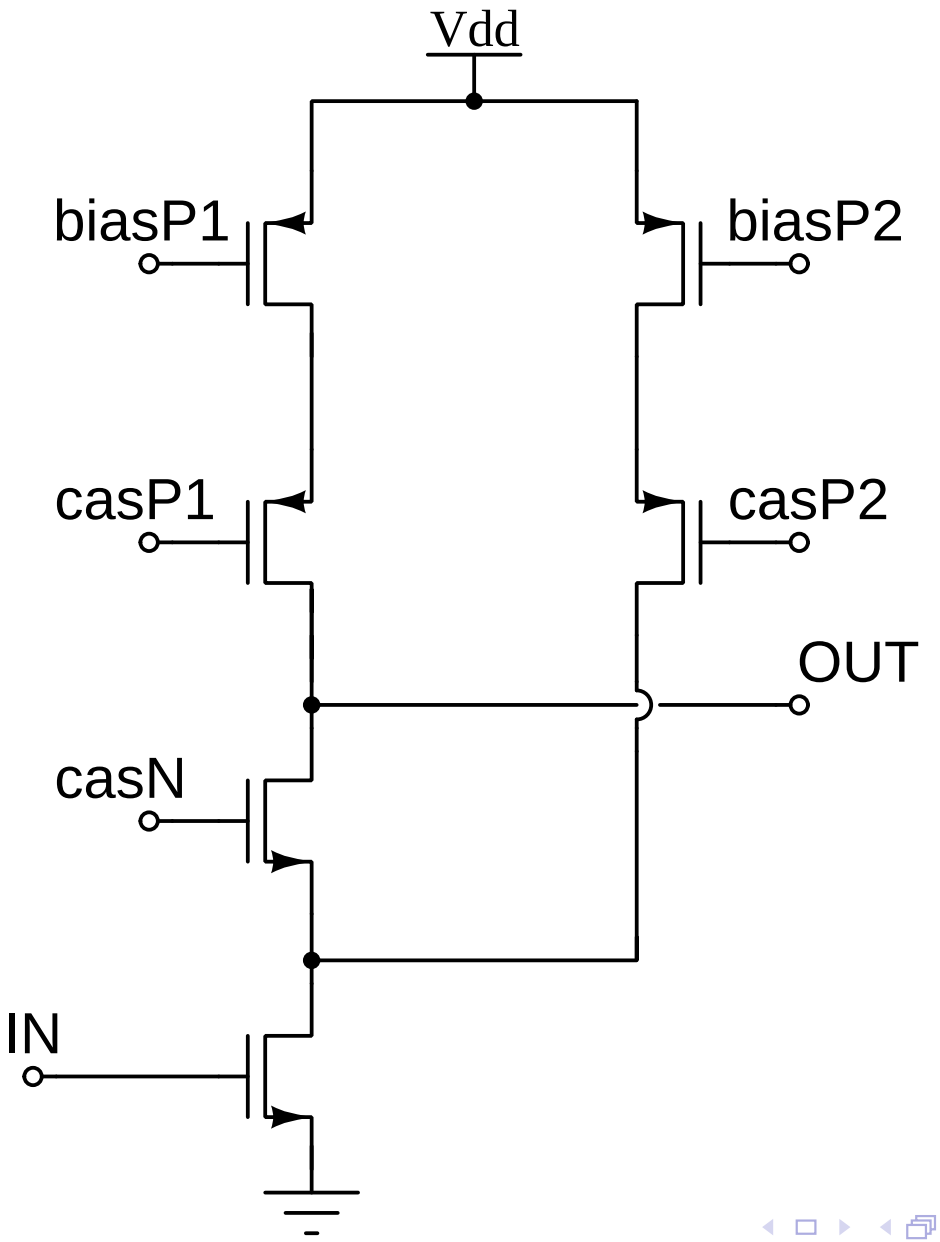
- **3 versions** of the CSA core amplifier
  → cover various sensor scenarios.
- **Design and Implementation** completed → **verification** (50 %).

Opamp with active feed-forward current compensation (ZC)

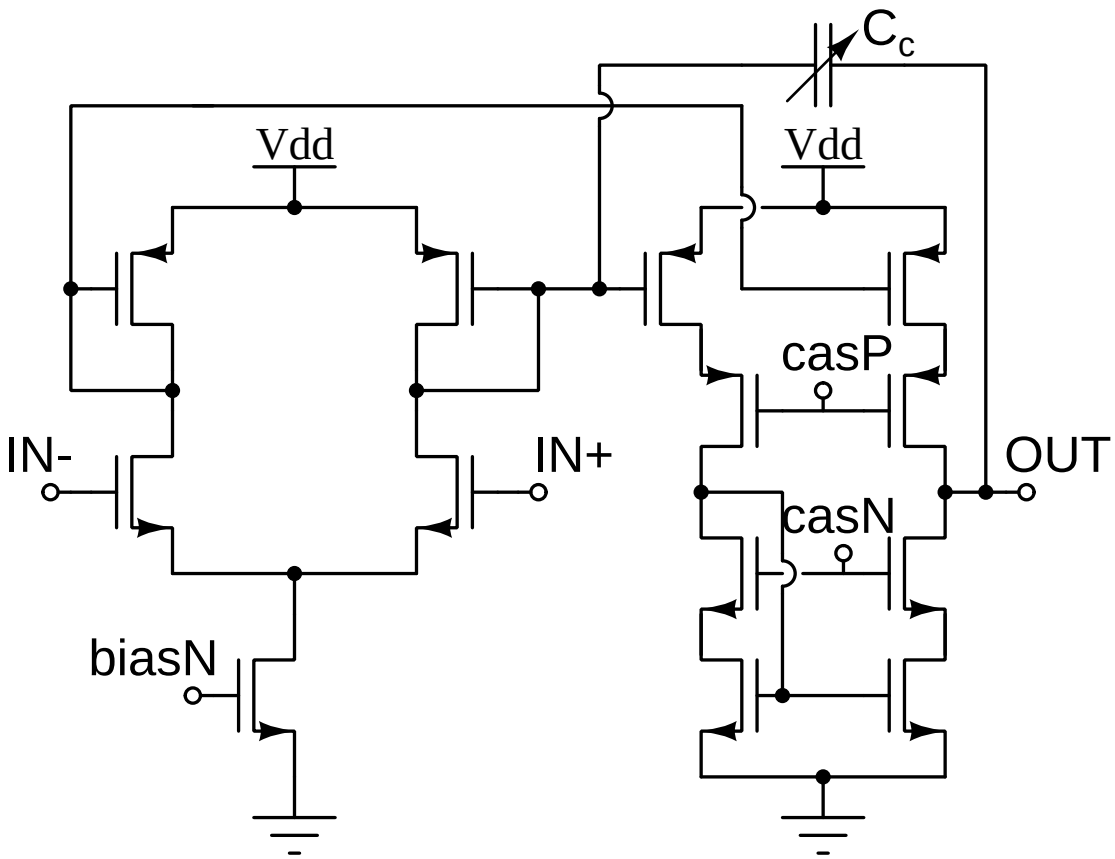


- Two stages.
- Output stage with split bias current to increase gain.
- ZC amplifier to **compensate feedforward current** $\rightarrow$ **increase phase margin**.
- Power $\rightarrow$ 97 µW.

Telescopic Cascode Amplifier with Split Bias Current

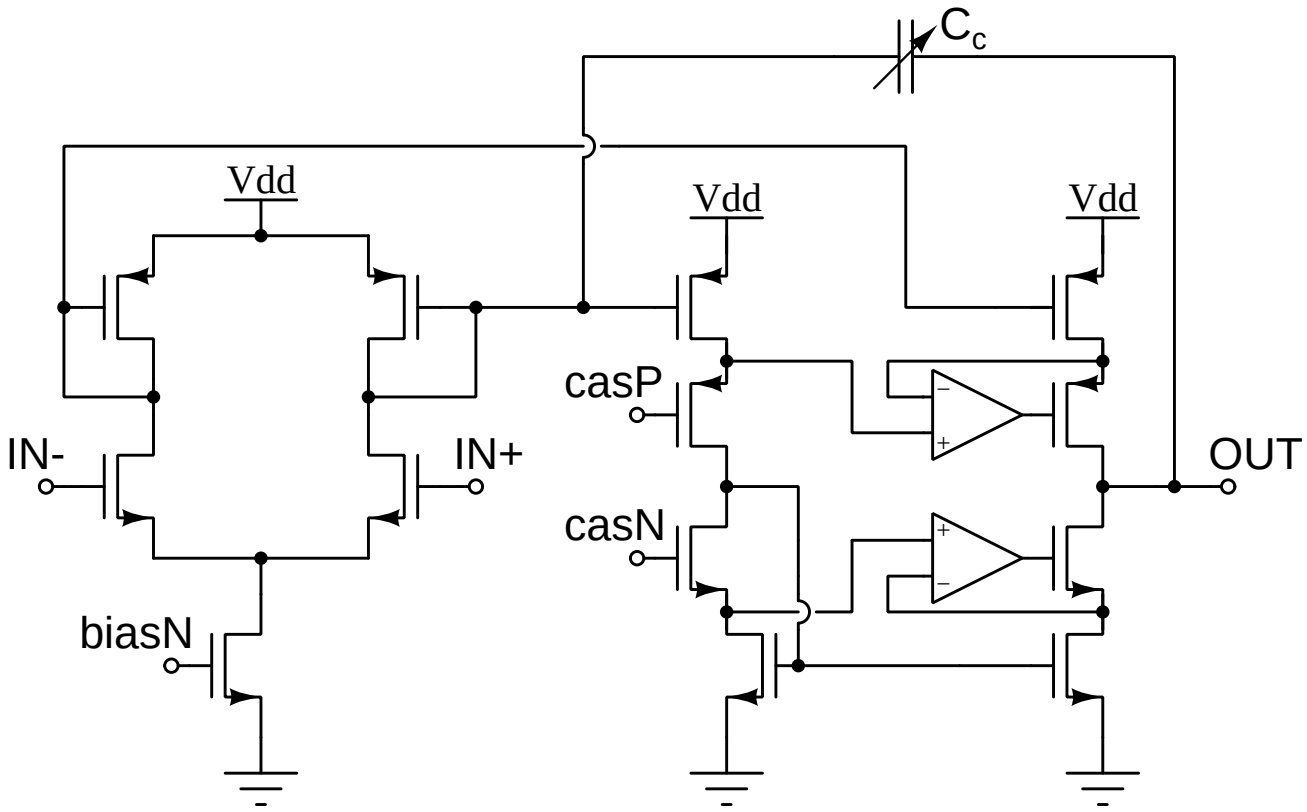


Two stage Opamp class AB (G)



- Two stages.
- Output stage cascoded.
- **Lower gain, higher band-width**.
- Power $\rightarrow$ 30 µW.

Two stage Opamp class AB with Gain Boosting (GB)



- Two stages.
- Output stage cascoded.
- **Gain Boosting → increases gain, decreases band width.**
- Power → 90 µW.

Amplifiers Perormance

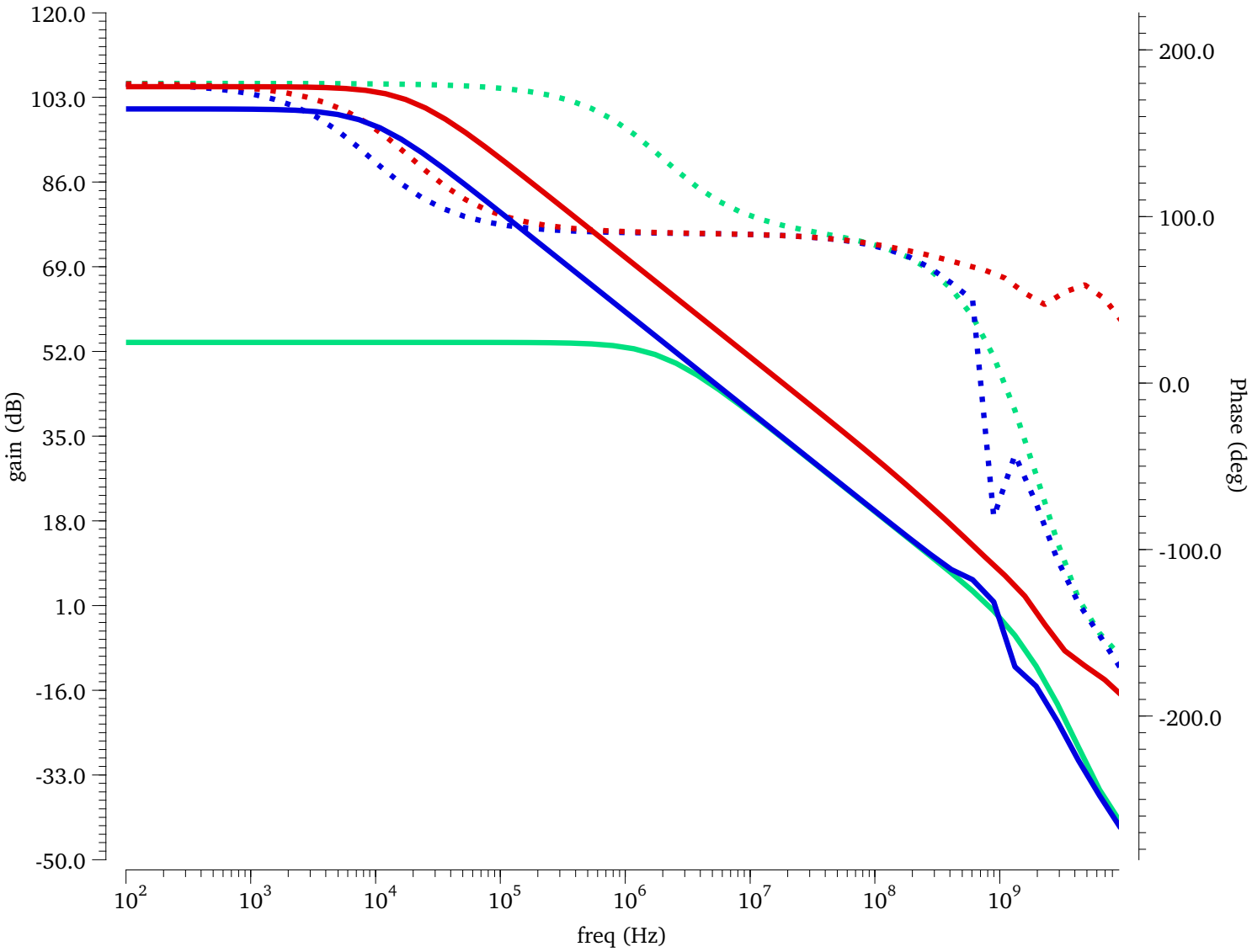


Figure: solid gain, dotted phaseZC G GB

BW and Phase Margin versus C_c

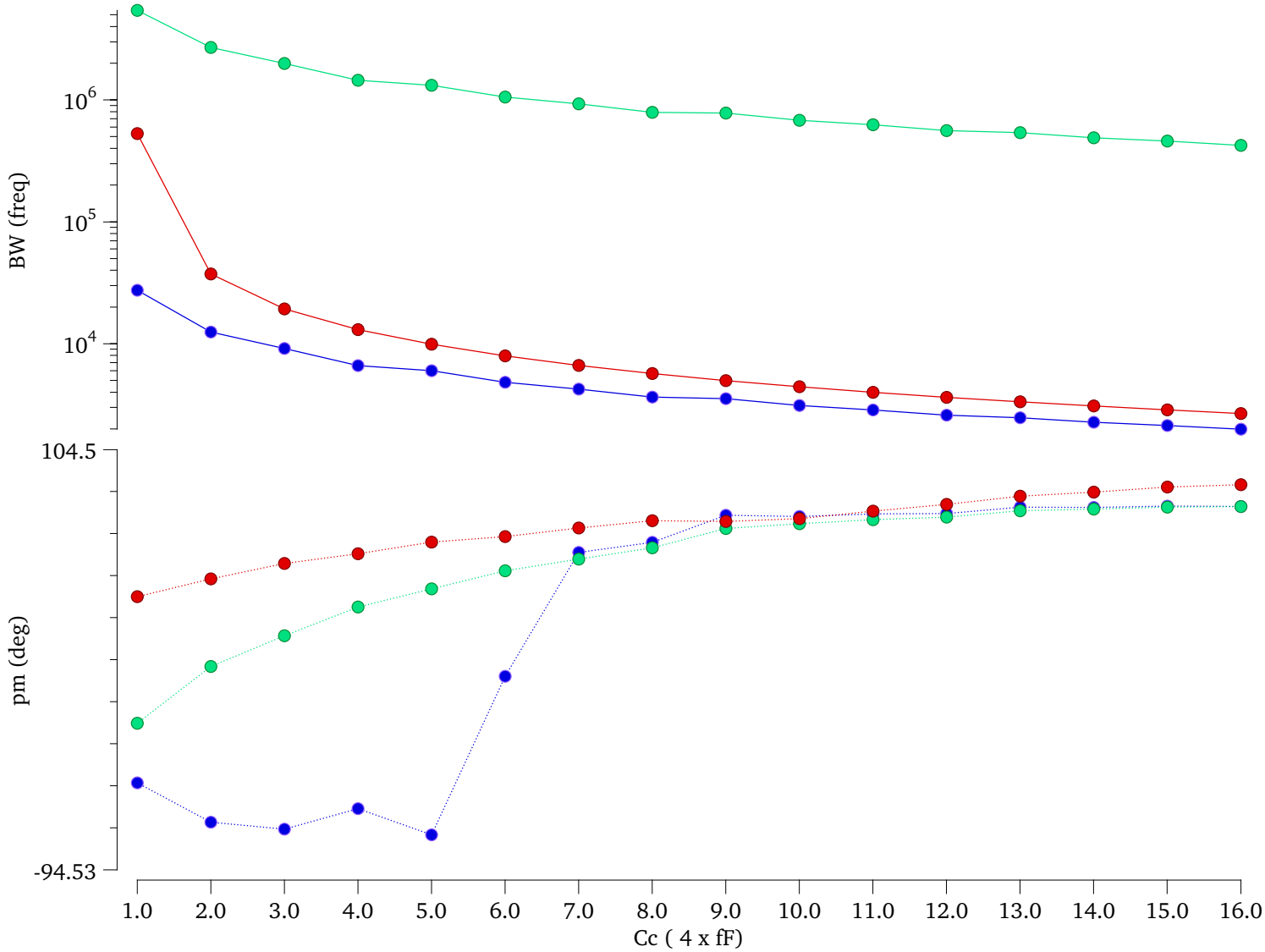
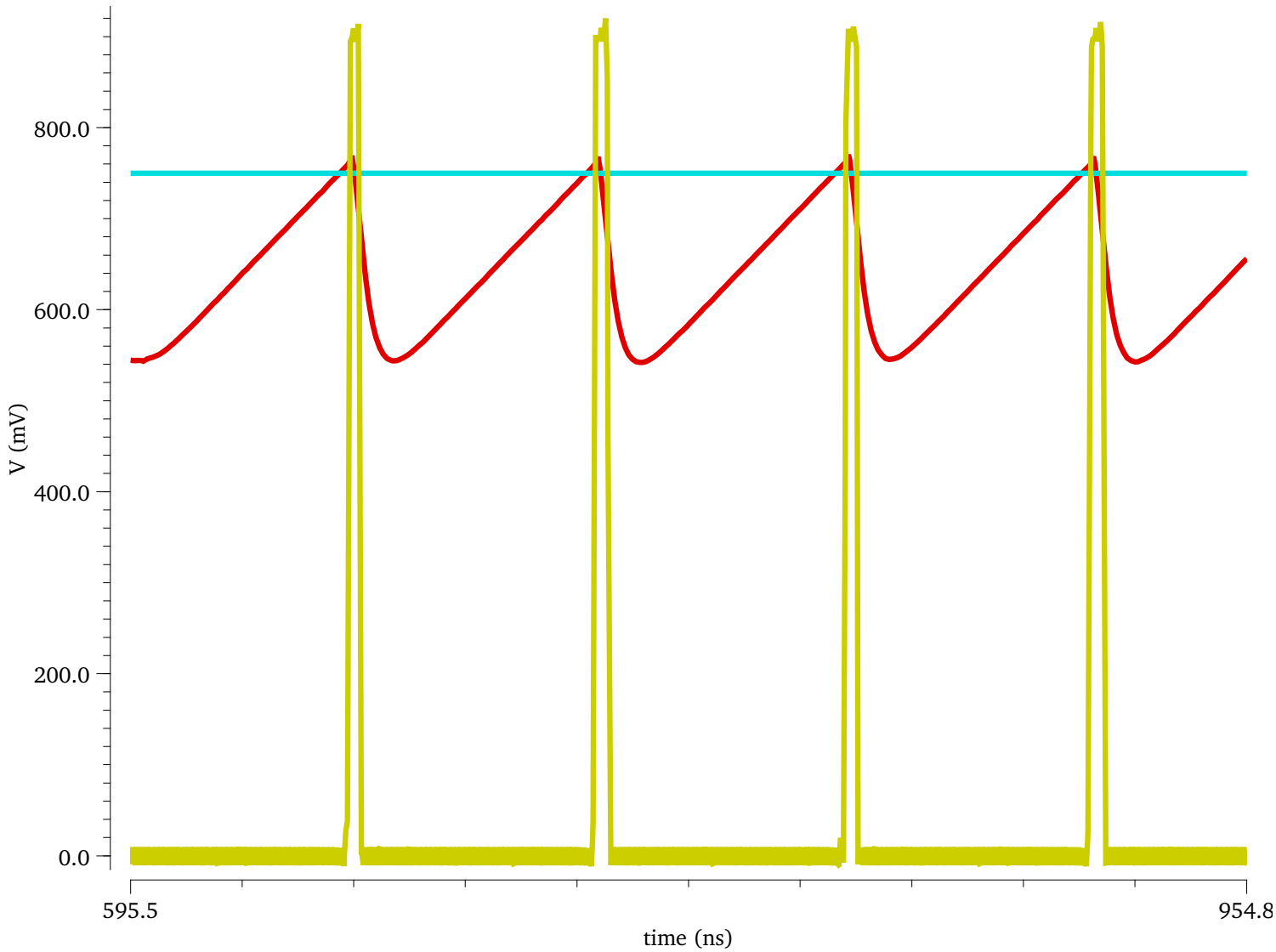


Figure: ZC G GB

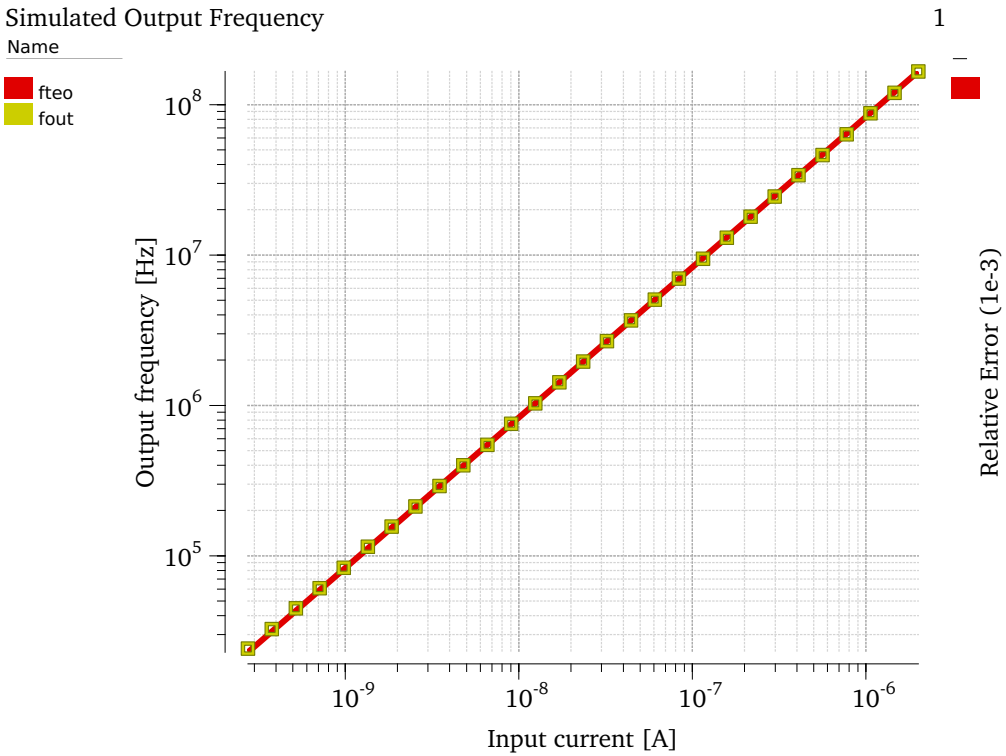
Programmable Capacitors

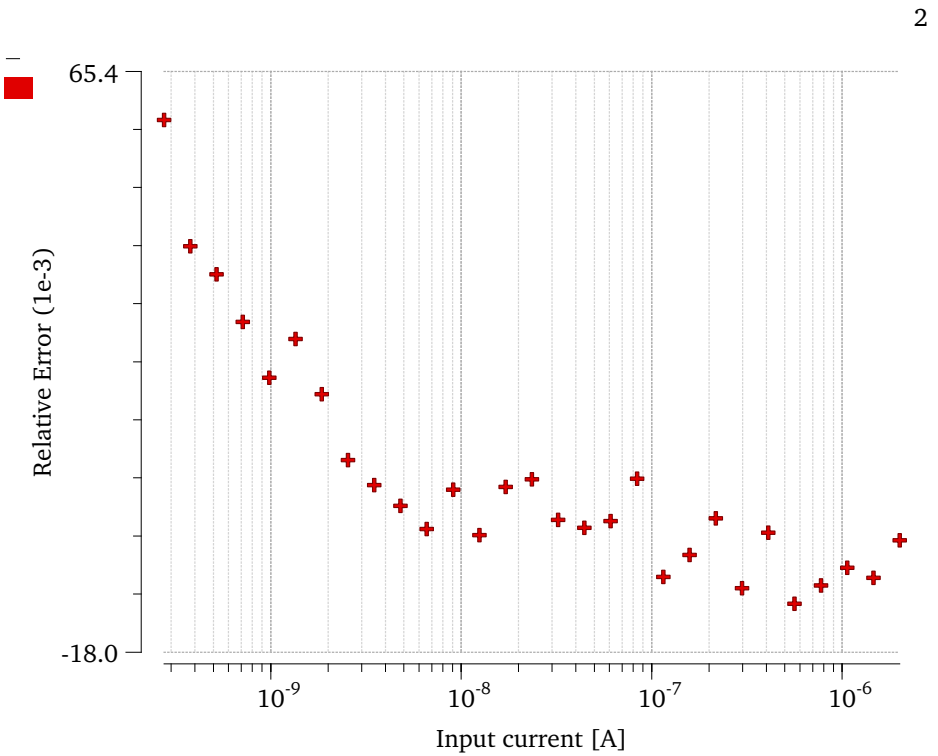
cap	nob	lsb	min	max
		fF	fF	fF
C_c	4	4	0	60
C_f	3	20	0	140
C_q	3	20	0	140

Operation Example



Simulated performance of ZC





- $C_S = 2\,\text{pF}$.

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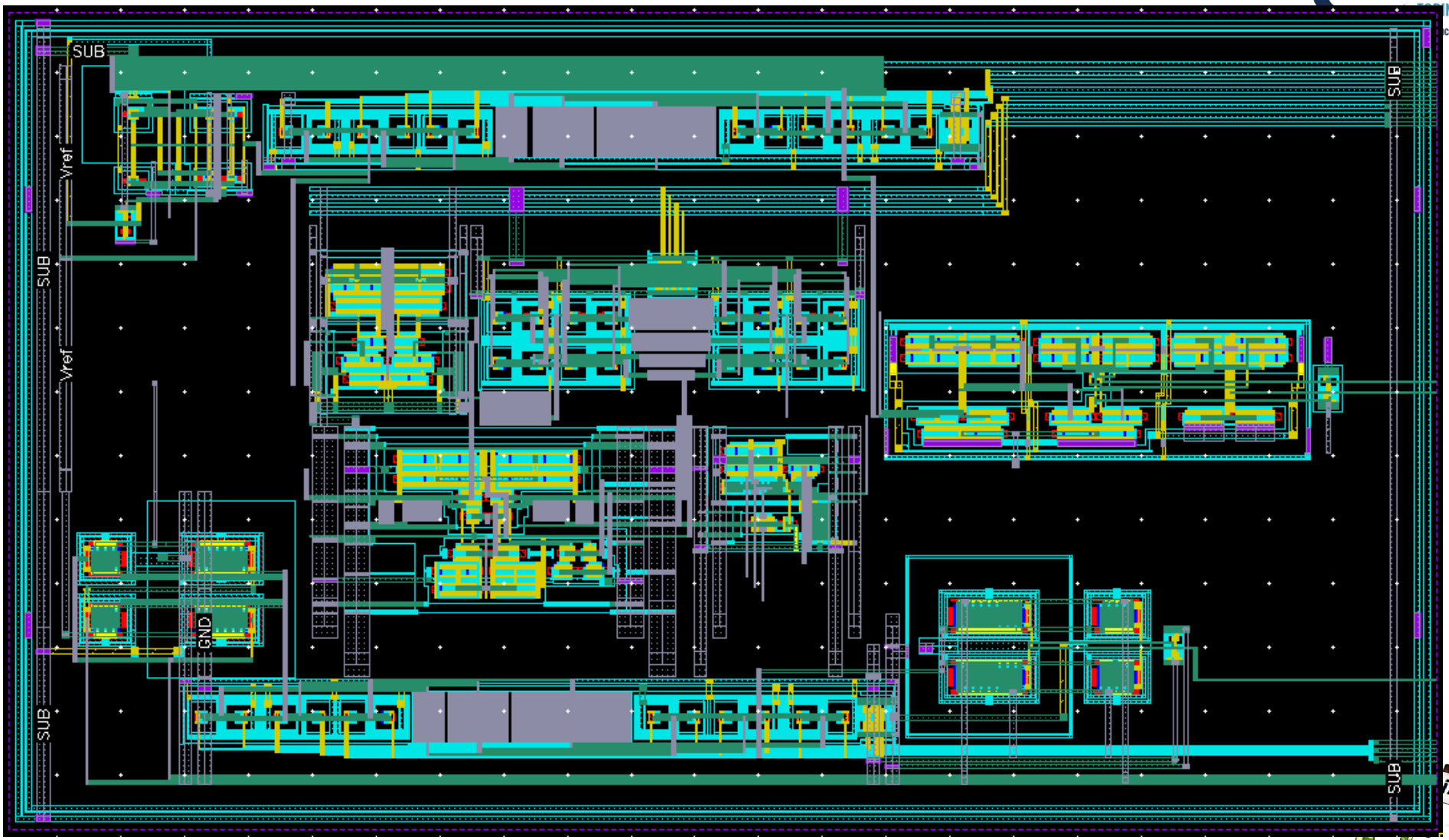
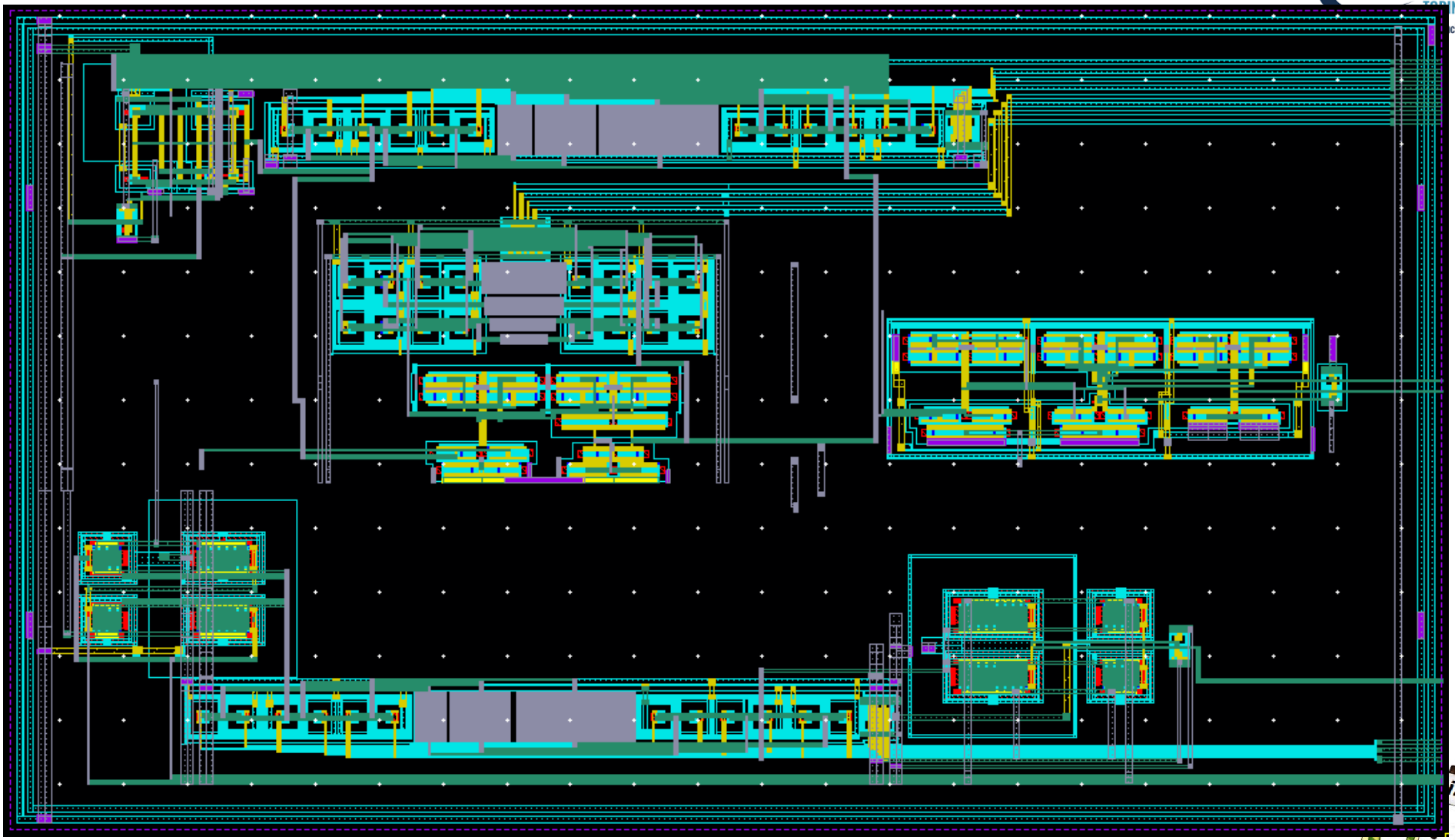
Analog Channels Implementation

- Layout of the three variants completed.
- Area $\rightarrow$ 112 µm $\times$ 64 µm.
- Ongoing DRC and LVS.
- Analog services layout to be implemented.

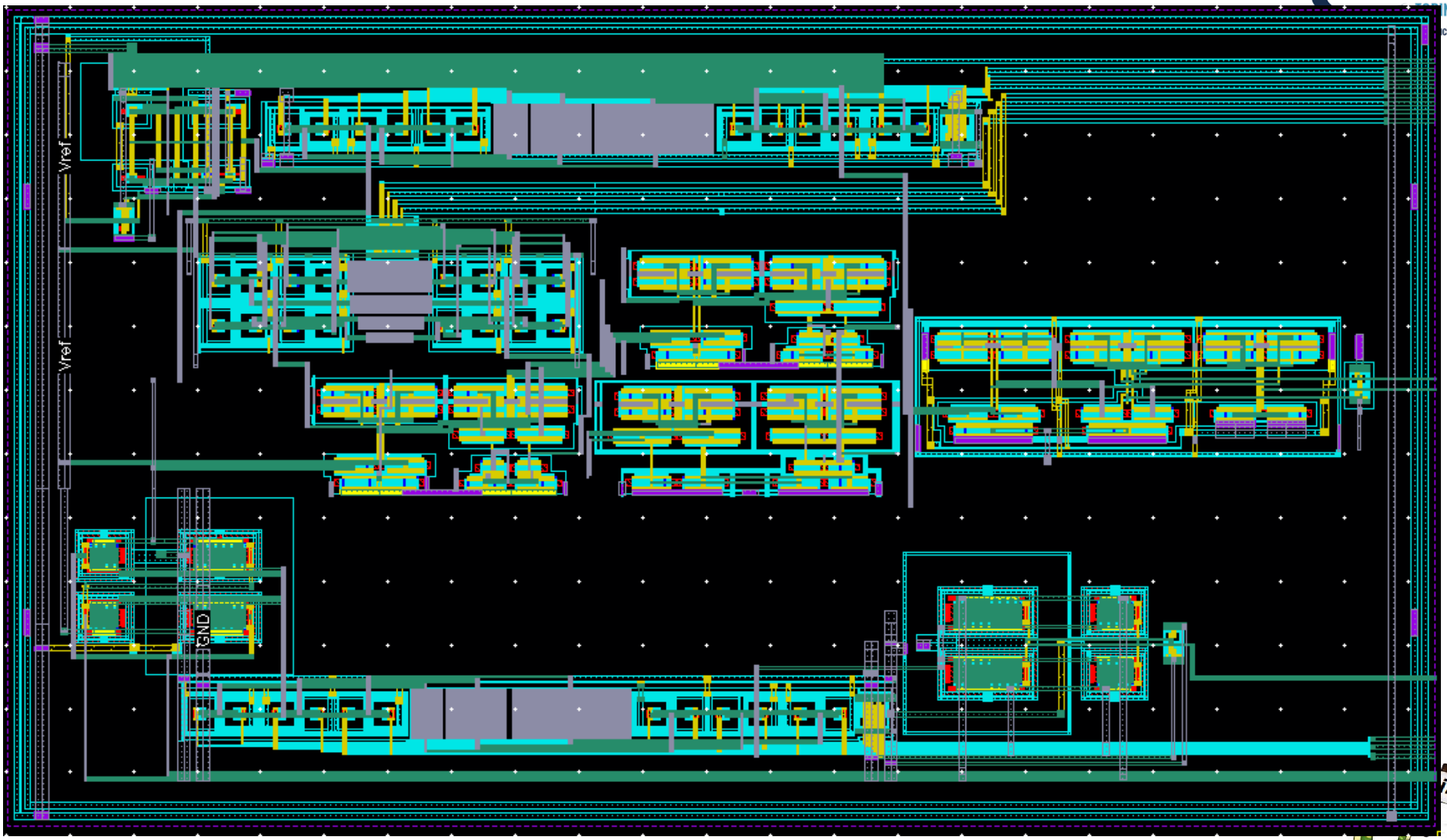
Layout of ZC



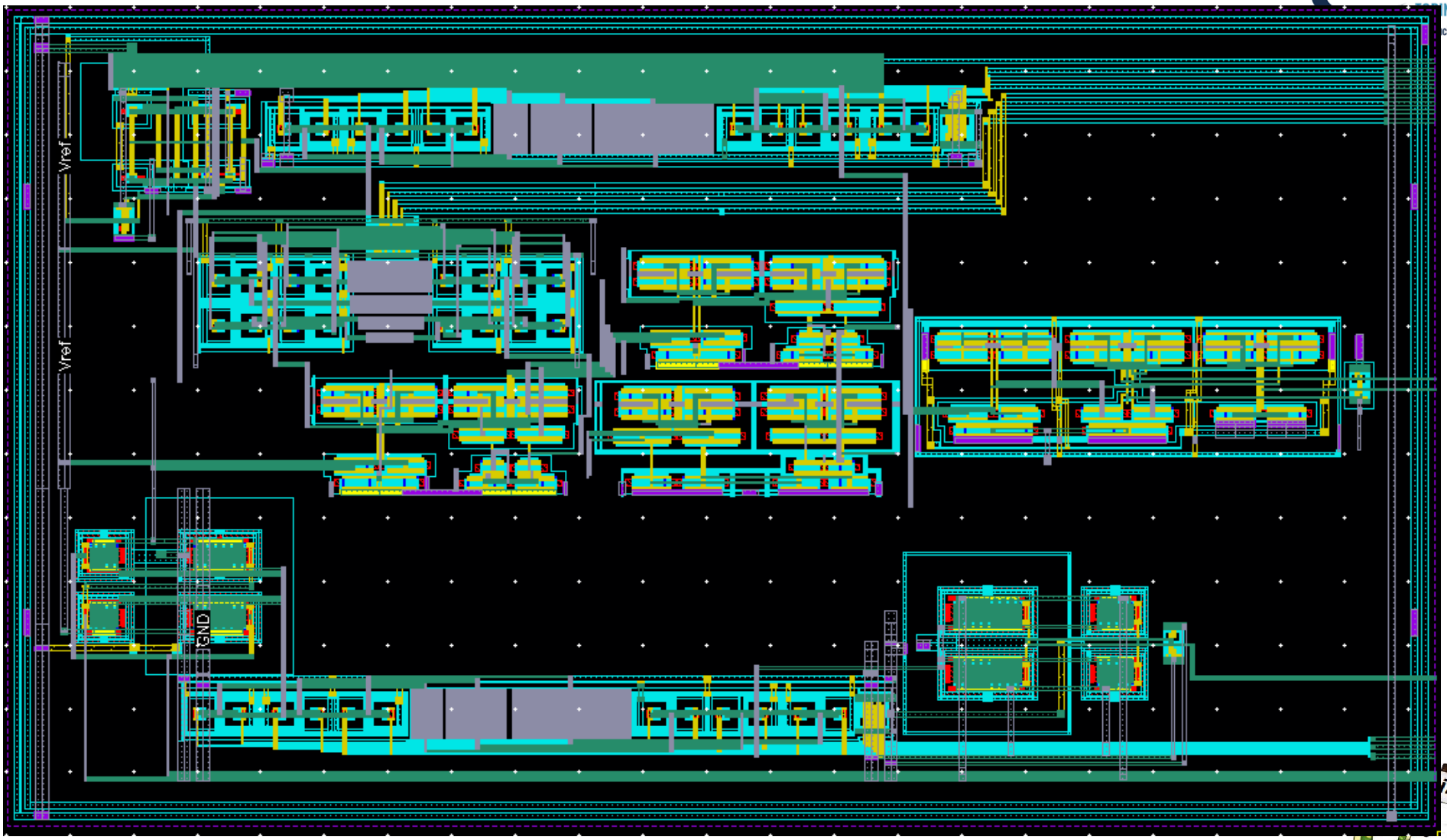
Layout of G



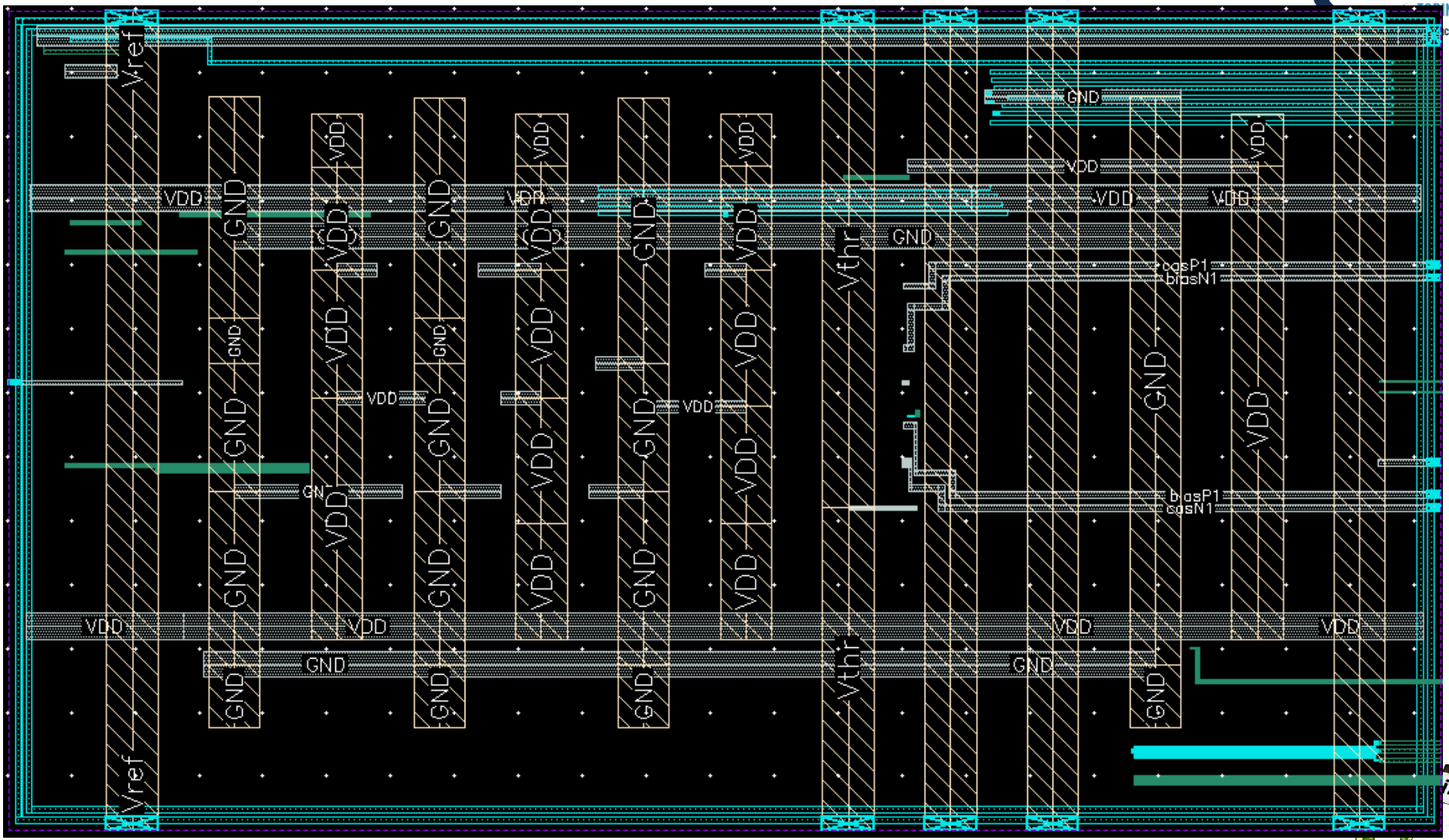
Layout of GB



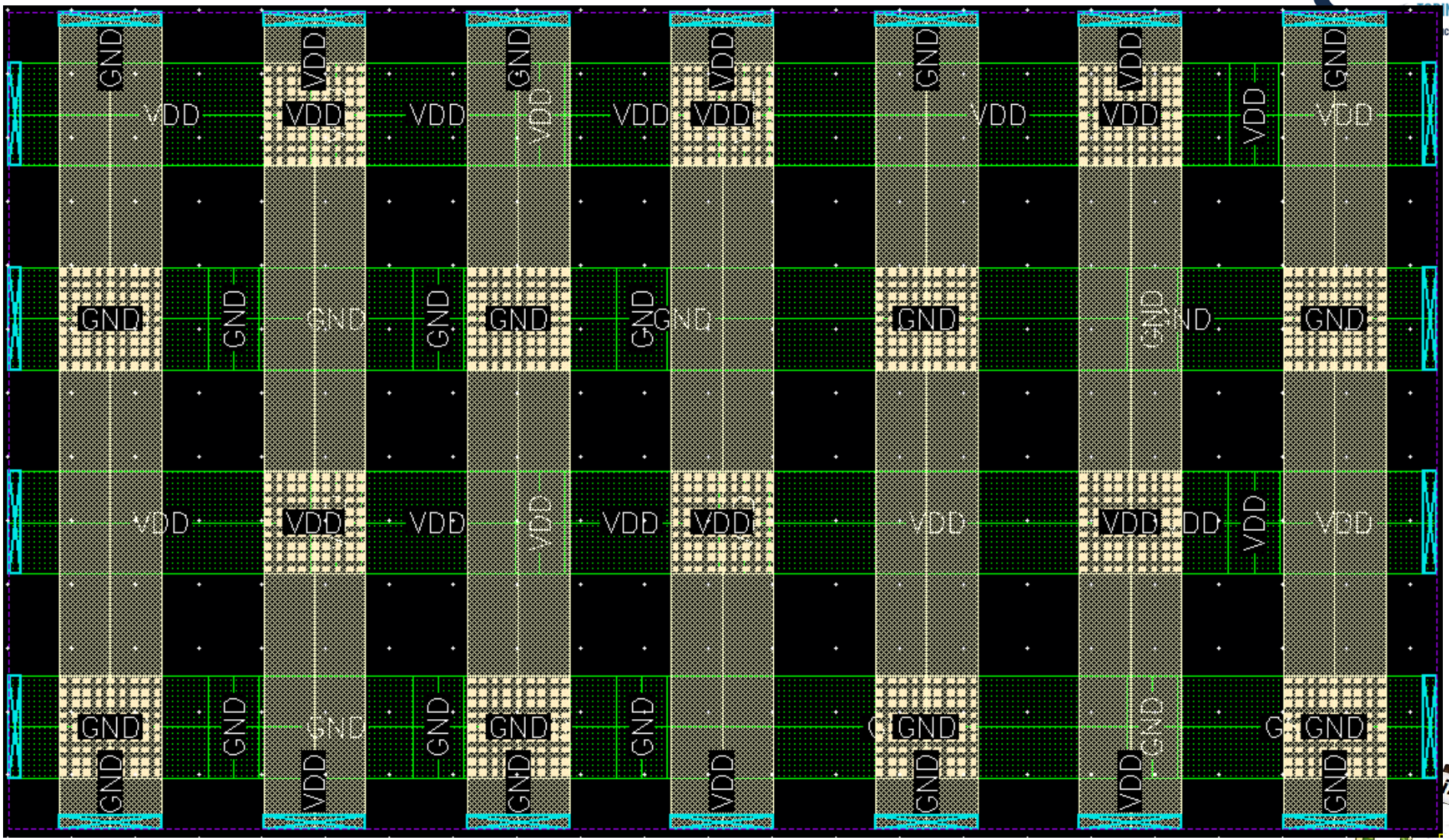
Layout of GB



Channel's Interface



Channel's Interface



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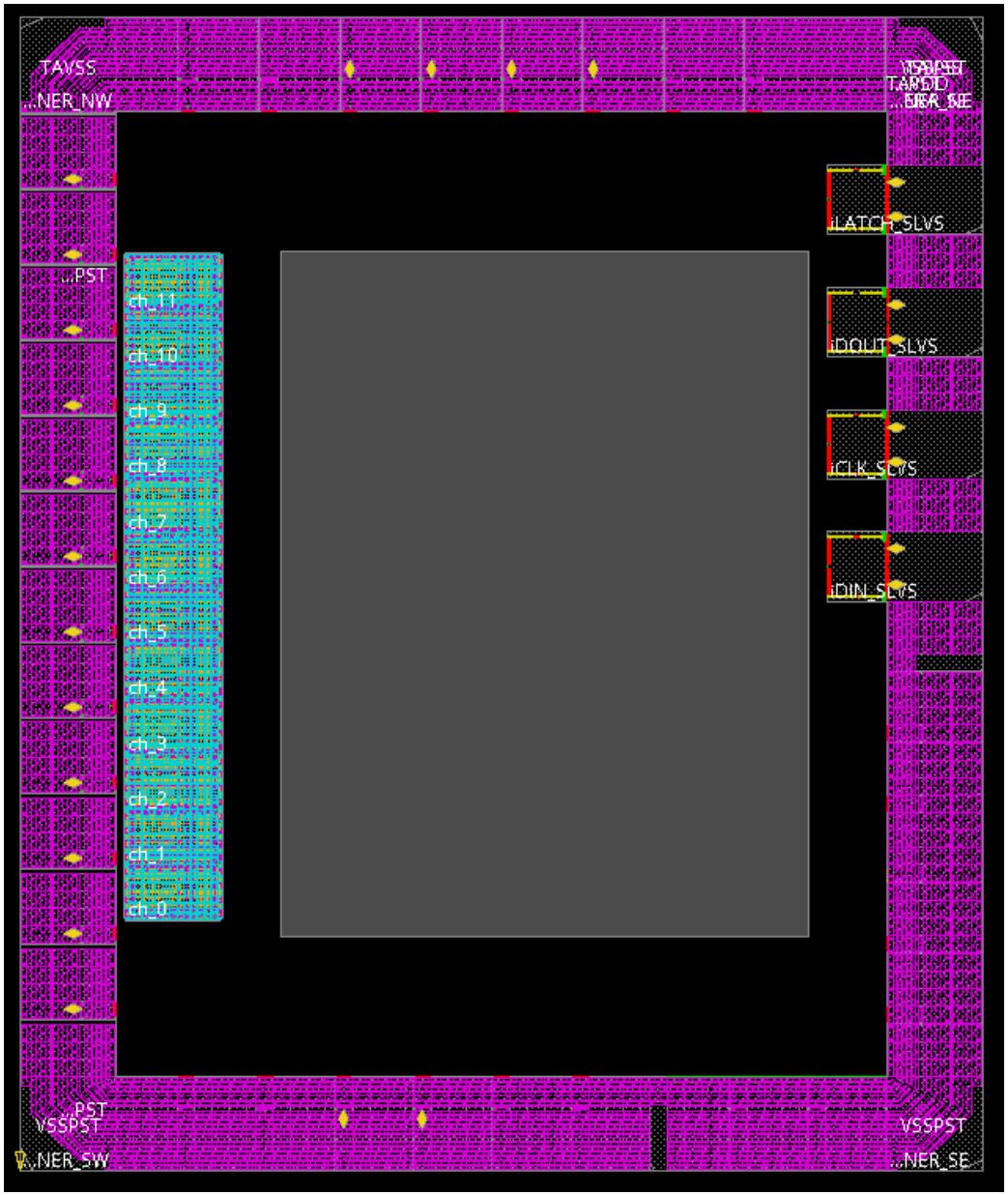
Floor plan

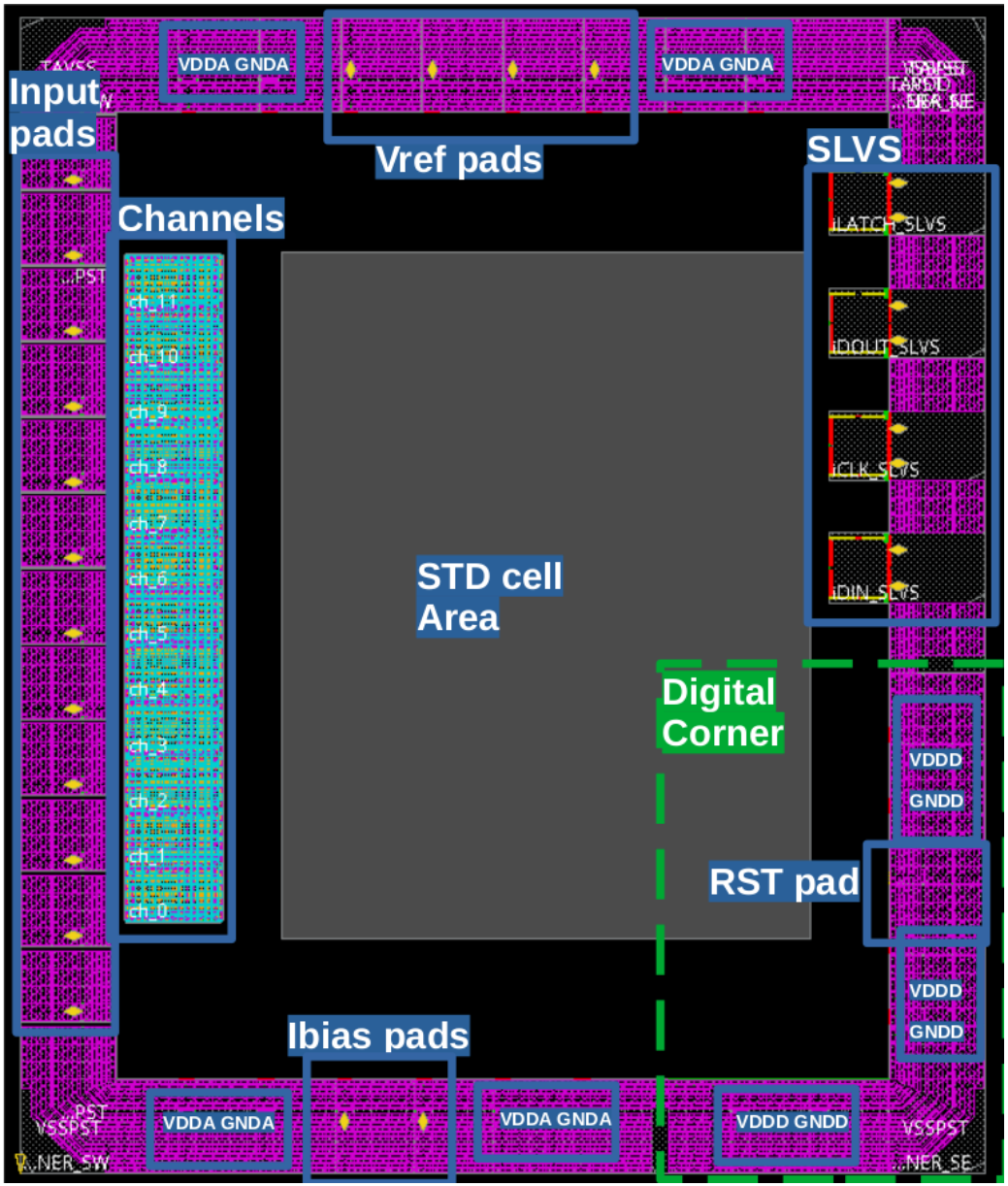
- Tentative $\rightarrow$ scripts are ready and easily modifiable.
- Waiting for rad-hard CERN IO pads.

ASIC FloorPlan: Tentative



- Name → **Cleopatra**.
- Layout area → 1111 µm × 1333 µm (0.9 shrink factor).
- Max pads number: 54 → **15 on long sides, 12 on short sides** (with a 70 µm pitch).
- In this example →
  - 12 channels (4 per variant).
  - top and bottom rows for analog periphery
  - Digital area → 600 µm × 800 µm (conservative)

ASIC FloorPlan: Tentative (Details)



- 12 channels.
- 1 digital serial output (DOUT).
- Digital serial configuration (DIN).
- CMOS reset signal.
- Analog pads: 12 current inputs, 4 voltages, 2 current biases.
- SLVS pads (differential) (CERN IP) $\rightarrow 4 \times 2$ receivers (CLK, LATCH, DIN), 1×2 transmitter (DOUT).

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To do List

- Verification → DRC,LVS ($\sim$ 50%, $\sim$ one week of work).
- Post layout simulations.
- Layout of the analog services ($\sim$ one week of work).
- Pad frame → scripts ready → finalize scheme, waiting for rad hard pads.
- Digital part implementation.
- Digital on top integration & verification ($\sim$ one month of work).

The goal is to close the design by the end of March and use the $\sim$ 4 weeks of April as buffer ("soft" official deadline: 26th April).