# HASPIDE WP2 Status

Valentino Liberali, INFN Milano

Florence, Feb. 02, 2023

# Introduction (from the proposal)

**HASPIDE[1] (HAmorphous[2] Silicon Pixel Detector for ionizing radiation)** addresses two types of detectors, for:

1. **intense radiation flux**, either continuous or pulsed, for beam monitoring in clinical and non-clinical accelerators (to be used in *WP4: Beam monitoring*);
2. **single particle**, either for cosmic radiation (to be used in *WP5: Space applications*) or neutron detection (to be used in *WP6: Neutron detection*).


[1] Greek: ἀσπίς (*Naja haie*) [photo by Ghorayr, from `en.wikipedia.org/wiki/Egyptian_cobra`]

[2] HAmorphous = H (hydrogen) + 'Amorphous', from greek ἄμορφος (= without form)

# WP2: Electronics and DAQ

Tasks:

- **T2.1**: Design of the front-end chip for clinical dosimetry
- **T2.2**: Design and test of the data acquisition board for neutron detection
- **T2.3**: Design and test of the data acquisition board for clinical dosimetry

T2.3 will use the chip designed in T2.1 (new prototype, in 28 nm CMOS);
T2.2 will use a chip already designed for other purposes (currently under characterization).

# First test chip (T2.1) – 1

First test chip (miniASIC) registered and confirmed by IMEC:

- Chip name: cleopatra (by Gianni Mazza)
- Area (design): 1.333 mm $\times$ 1.111 mm
- Optical scaling (linear): $\times 0.9$
- Area (silicon): 1.2 mm $\times$ 1.0 mm
- Design "flavor": 28 nm CMOS RF High Performance Compact Mobile Computing Plus ELK Cu 1P10M 0.9/1.8V [RF HPC +]
- Metal stack: 1P9M_5X1Y1Z1U UT-ALRDL
- Number of dies: 100 only, naked
- Backend: Wirebond

Purchase order sent to IMEC (12.169,00 € + VAT)

Deadlines:

- Preliminary gds submission deadline: 29th March 2023
- Last chance of cancellation deadline: 29th March 2023
- Final submission deadline: 26th April 2023

Preliminary gds does not need to be DRC/LVS clean. It must:

- have the final area
- include all the CAD layers and devices of the final gds

# First test chip (T2.1) – 2

Read out architecture is based on TERA chip, already in use (made with different technologies)

New design in 28 nm CMOS
Advantages:

- Mature technology, available through IMEC
- Low cost (per transistor)
- Already used in INFN projects (AM chips, TIMESPOT)
- Complete cell library available trough CERN (for the 1P9M stack), including layout view $\longrightarrow$ complete parasitic extraction is possible
- Intrinsically rad-hard

Drawback:

- Cell library was made available only in Jan. 2023
- Performance limited by layout parasitics
  $\longrightarrow$ speed and power can be estimated only with post-layout simulations


Details in the talk given by Lorenzo Piccolo

# Chip for single particle detection (TO)

- Designed for the PANDA MVD (outside the HASPIDE project)
- CMOS UMC 0.11 µm technology
- 64 channels ASIC for strip readout
- preliminary test results are available

Additional details provided by Gianni Mazza

# DAQ system with TERA chips (LNS)

- Read-out chain based on the TERA-08 chip
- Two configurations: for continuos and for pulsed proton beams
- Originally designed for continuous beams; modified to work also with pulsed beams
- FPGA board for data acquisition

Details in the talk given by Roberto Catalano

# DAQ system from University of Wollongong (UoW)

DAQ system already available.
Modified DAQ versions:

- Programmable sensor voltage
- Increase of the number of channels

Details in the talk given by Marco Petasecca

# Workplan for 2023 (1)

- miniASIC design and test:
  - design to be completed by April 26
  - 3 months for fabrication $\longrightarrow$ dice available at the end of July
  - test board design in May-June
  - test board firmware in June-July
  - assembly in August (?) or September
  - miniASIC test in (September)-October-November
  - Milestone: "Characterization of the first miniASIC" to be delayed to Nov. 30, 2023 (or Dec. 15, 2023)
- People involved in chip design: Lorenzo Piccolo, Gianni Mazza (TO); Valentino Liberali, Alberto Stabile, Luca Frontini (MI: chip integration and design support); Pisana Placidi (PG: design support)
- People involved in board design, firmware, and test: Gianni Mazza (TO: all activities); Lorenzo Piccolo and Francesco Rotondo (TO: board design); Richard Wheadon (TO: firmware and test) + new PostDoc (?)

# Workplan for 2023 (2)

- DAQ system with TERA chips:
  - assembly in July
  - firmware in July
  - test with pulsed beams in August
  - People involved: Roberto Catalano, Pablo Cirrone, Giacomo Cuttone, Giada Petringa (LNS)
- DAQ system from University of Wollongong:
  - Data acquisition system modified to allow to bias the sensor with a programmable voltage – Done
  - Test of the modified DAQ in February
  - Modified DAQ will be sent to Florence (after tests)
  - New DAQ version with 128 channels (end 2023 / begin 2024)
  - People involved: Marco Petasecca, Matthew Large (UoW)

WP2 will have regular meeting every two weeks,
on the first and the third Fridays of every month

# THANK YOU !

Questions ?