The CGEM-IT interlock system

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Interlock System

- The Interlock system is a safety system, which acts as last line of defense, and it is designed to protect the sensitive detector elements against upcoming risks
- To protect the detector, it is necessary to define and be able to identify allowed and not allowed states (according to the main parameters read by the sensors)
- In particular, the interlock system must avoid that the high voltage is switched on while the low voltage is switched off, or that there is no correct gas flow in the detector as there could be discharges which could damage the detector

Definitions

- INTERLOCK DISABLED (CONTROLLINO_output 5V or 1) = possibility of turning on the electronics
- INTERLOCK ENABLED (CONTROLLINO_ output 0V or 0) = impossibility of turning on the electronics

Define the states of the system

A 4-state logic was developed in which the states are identified by a binary number (i.e. [001]). Each binary number will correspond to a specific system configuration

- To define the system state a set of specific functions are used, each one operating on one specific status bit

- When all parameters of a single stage are ready, we set the specific bit to 1(1 stage OK, 0 something wrong)

Define the states of the system

- The allowed configurations are:

- [000] (0), some parameters are out of proper range, LV and HV interlocks are enabled
- [001] (1), all parameters are correct, and the LV interlock is disabled, the HV interlock is still enable
- [011] (3), all parameters are correct, and the low voltage is turned ON and the high voltage interlock is disabled
- [111] (7), all parameters are correct, the LV and HV are turned ON

- If the system is in a different state than the allowed ones, the logic will bring the system back to a «Safe State», (for example [101] → [001])

Reading LV state

- A new routine executed periodically by the soft microcontroller in the GEMROC FPGA monitors the FEBs' supply voltages and currents and removes the LV interlock bits when they are in the correct power state
- The new routine sets an HDMI port pin based on the status of FEBs
- The interlock system obtains the LV configuration information by reading this digital pin (1 pin per GEMROC)

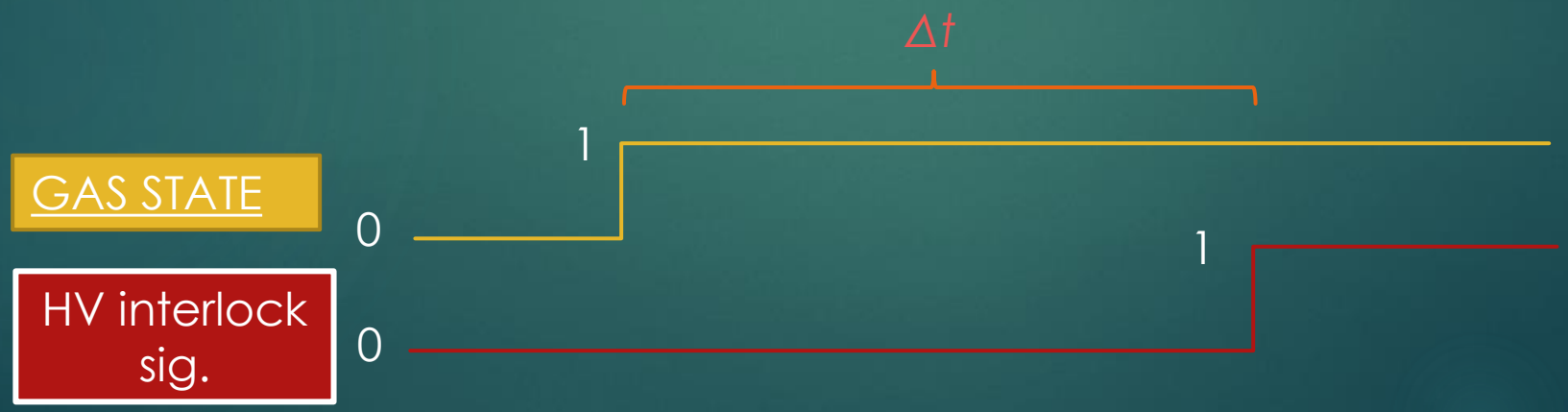
Pin level	FEBs configuration	HV interlock sig
LOW (0V)	FEBs OFF or errors*	LOW (0V), turn-ON the HV **not allowed**
HIGH (5V)	FEBs ON and no errors*	HIGH (5V), turn-ON the HV **allowed**

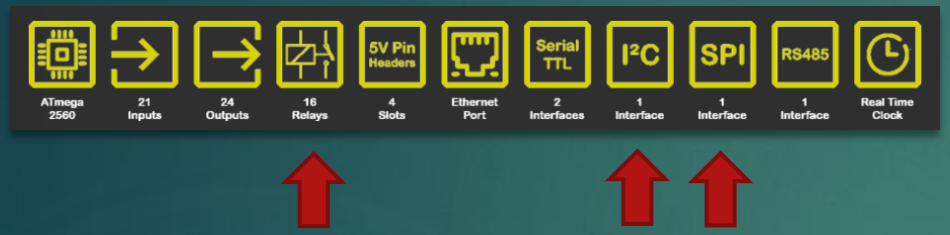
Errors* = over currents/voltages, the desired pattern does not corresponds to actual pattern.

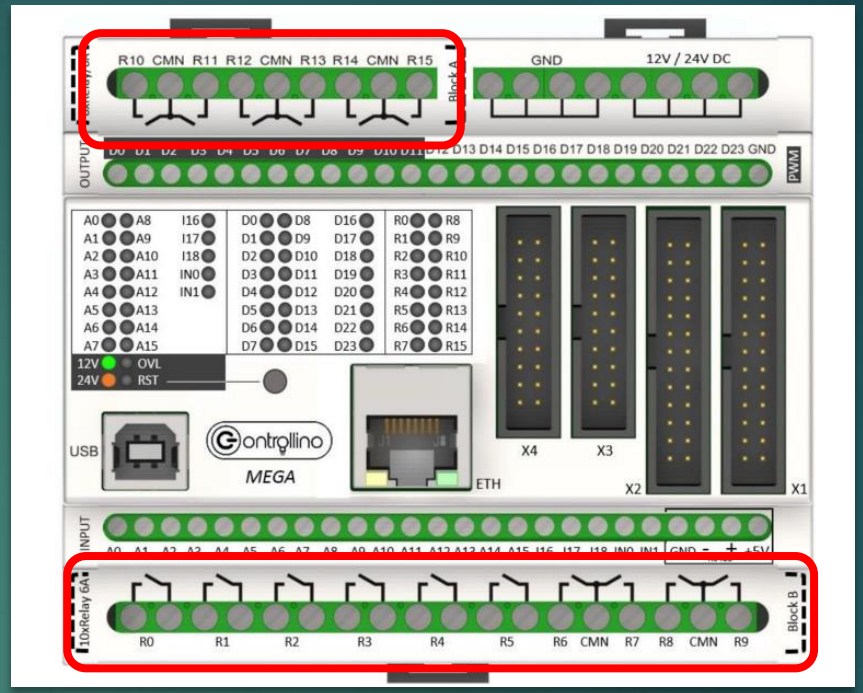
Gas-HV delay, [011] → [111]

- Remind: [011] (3), all parameters are correct, and the low voltage is turned ON and the high voltage interlock is disable. [111] (7), all parameters are correct, the LV and HV are turned ON

- The state transition is as usual, but the possibility to turn on the high voltage is given only after a certain time interval has passed since the gas state is equal to 1
- The time interval is such that the gas can adequately fill the detector volume (≈1 min for the planar setup in 334)





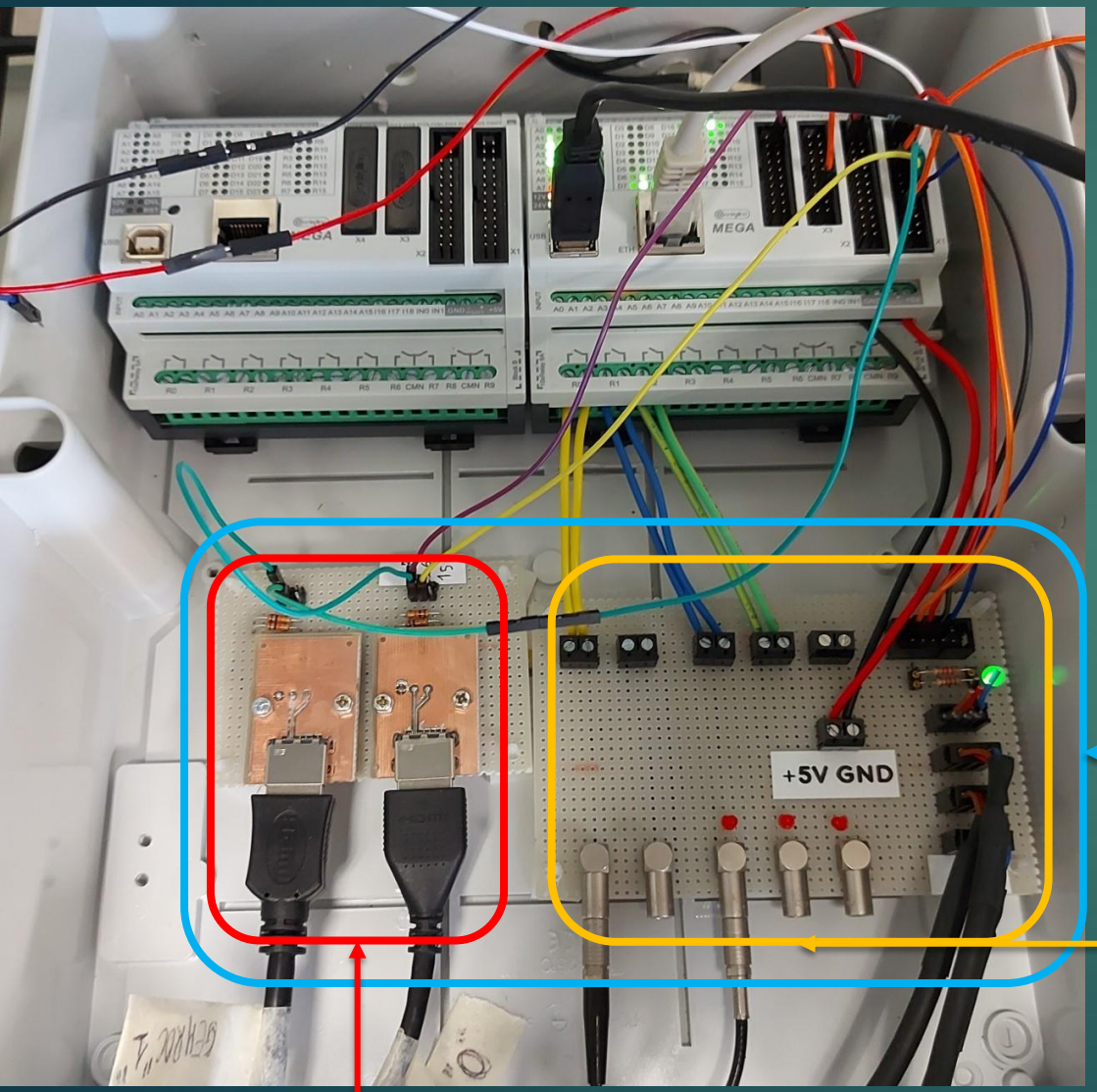


(User Manual)

Core of the Interlock system

- The core of the Monitoring and Interlock is a “CONTROLLINO MEGA ”
- The I2C interface is used to communicate with the sensors
- The Relays of the controllino are used to manage the interlock signals

Interface board



- The interface board features the interlock/sensor I/O connections and the GEMROC cards interface
- It allows a stable connection between sensors, CAEN electronics, and the interlocking system

Interface board

Interlock/sensor pannel

GEMROC cards interface

Interlock signals

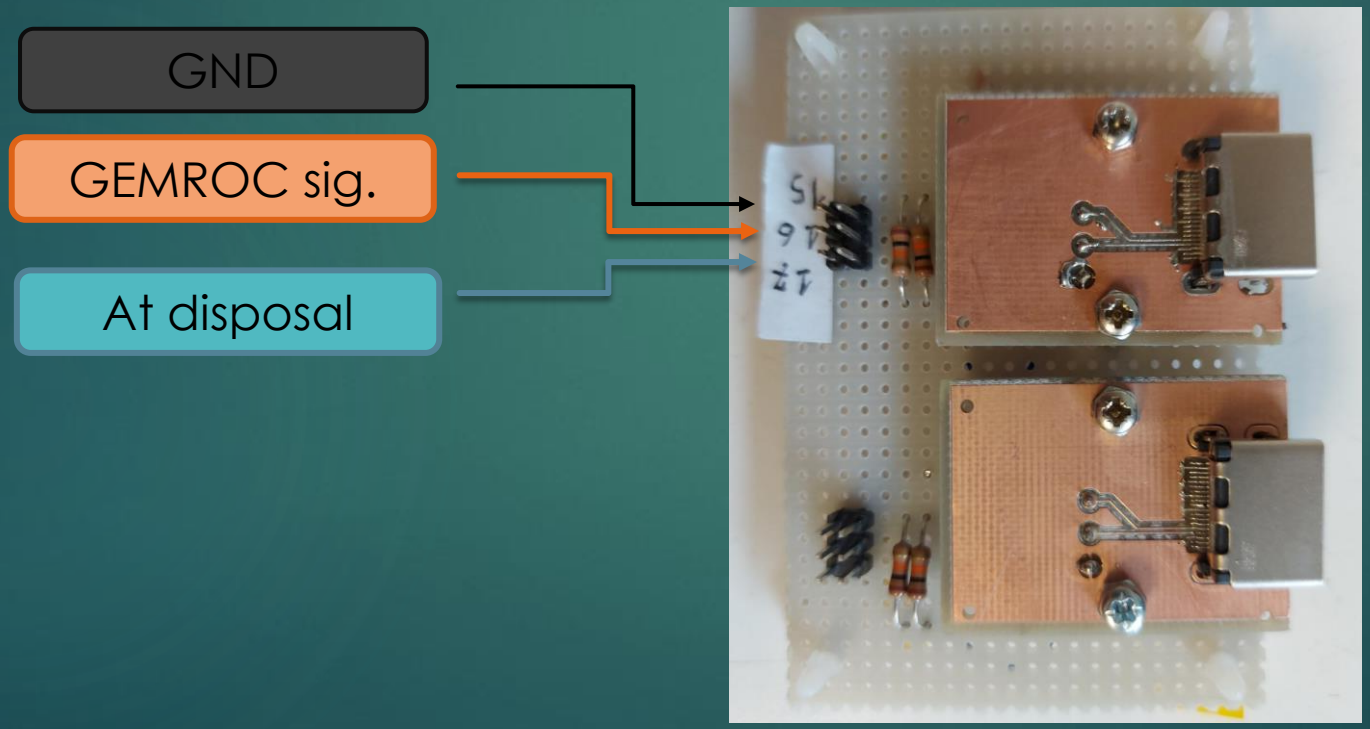
- The logic for the interlock signal is based on the normally open relays of the CONTROLLINO
- The mainframe interlock switch must be in the upper position (OPEN state)
- In this configuration, if anything happens to the CONTROLLINO, the electronics will be switched off

Interlock sig	Board config.
HIGH (5 V)	Interlock disable
LOW (0 V)	Interlock enable

Interlock switch	Mainframe config.
OPEN	Interlock disable
CLOSE	Interlock enable

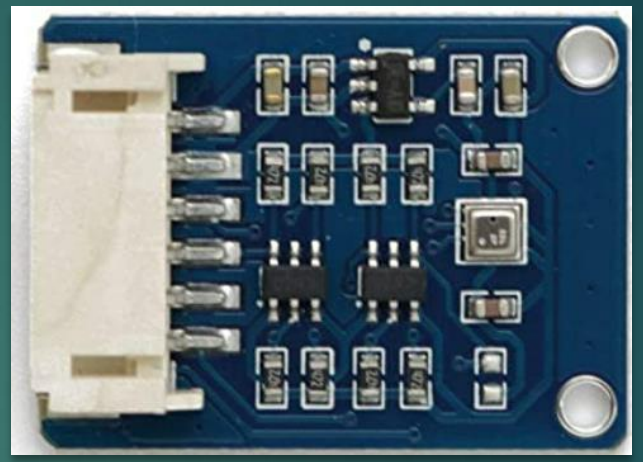
GEMROC-IL communication

- The interface between the GEMROC and the interlock system consists of the HDMI breakout, which provides easy access to the HDMI pin16 and 17 "open-drain" driven by the attached GEMROC cards



Chipcap-2sip

YF-S401



BME280

Sensors

- Gas temperature, humidity and pressure sensors: BME280 (I2C)
- Temperature and humidity sensor: Chipcap-2sip (I2C)
- Flowmeter (cooling):YF-S401

Test of the sensors

- I2C communication was tested up to 15 m (useful information for defining the final configuration)
- To ensure stable and error-free communication, pull-up resistors (2.2 KΩ) and a suitable CLK frequency were placed on the I2C bus

Clock signal, freq = 100KHz

Clock signal, freq = 50KHz

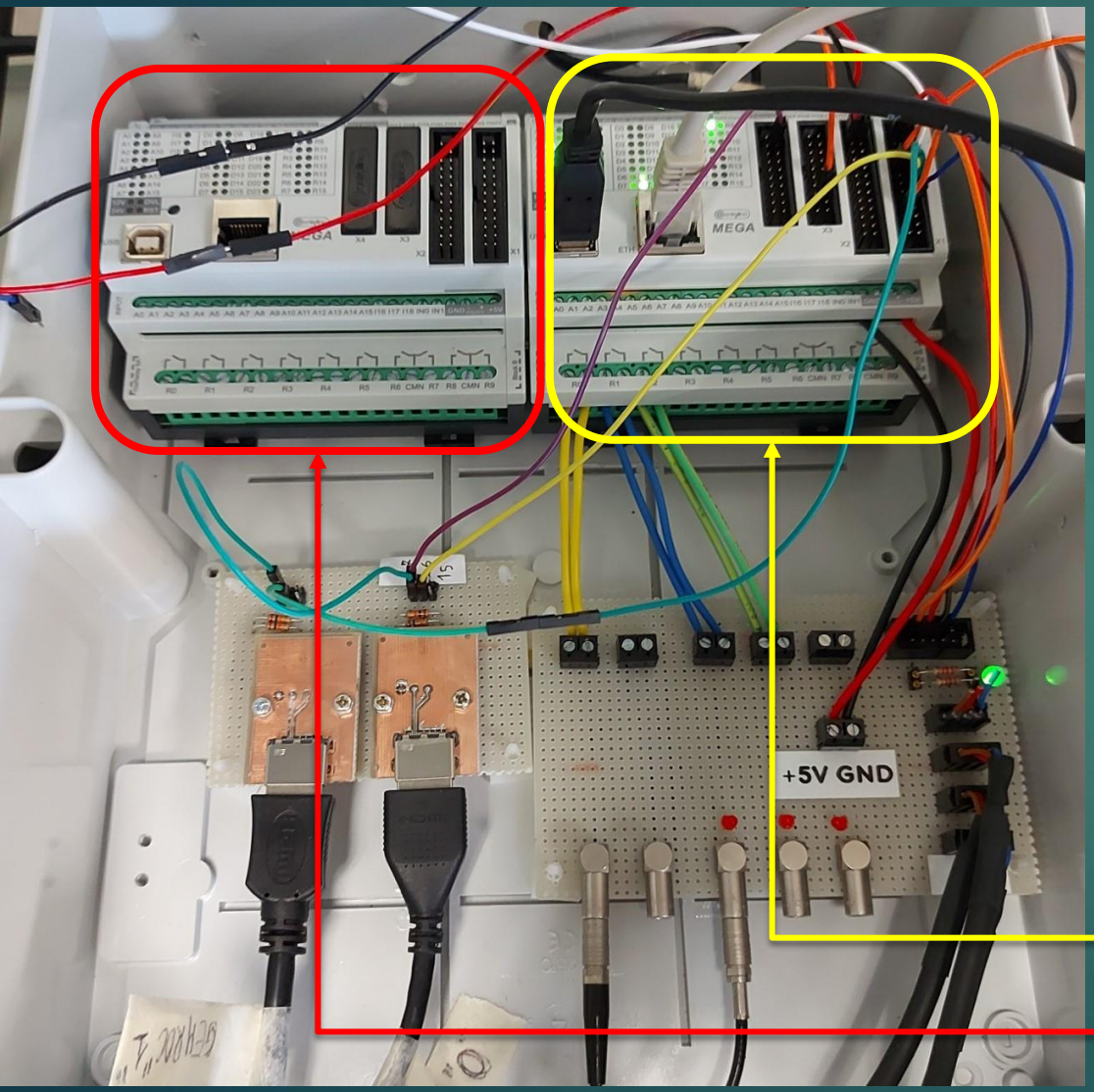
Data storage and Alarms

A UDP communication is used to send the collected data to the laptop (where it will be written to a file)

The alarms signals are sent to a laptop through the same UPD communication of the date.

Alarms are identified by the python routine that is able to alert users through an e-mail

The redundancy of the system



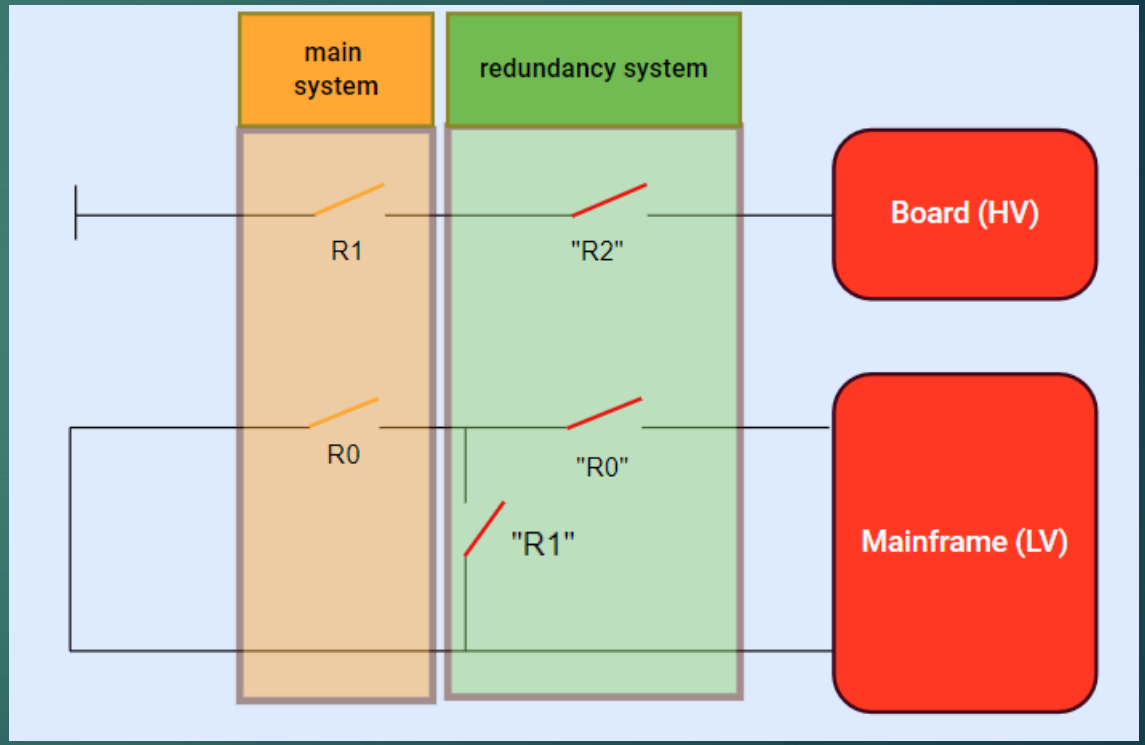
- The secondary system monitors the main CONTROLLINO
- If the main system stops working, the secondary system turns-OFF the detector
- The main system sends a rising edge to the secondary system at each cycle end. The latter checks if there is the propper frequency coming from the main one

Main system

Secondary system

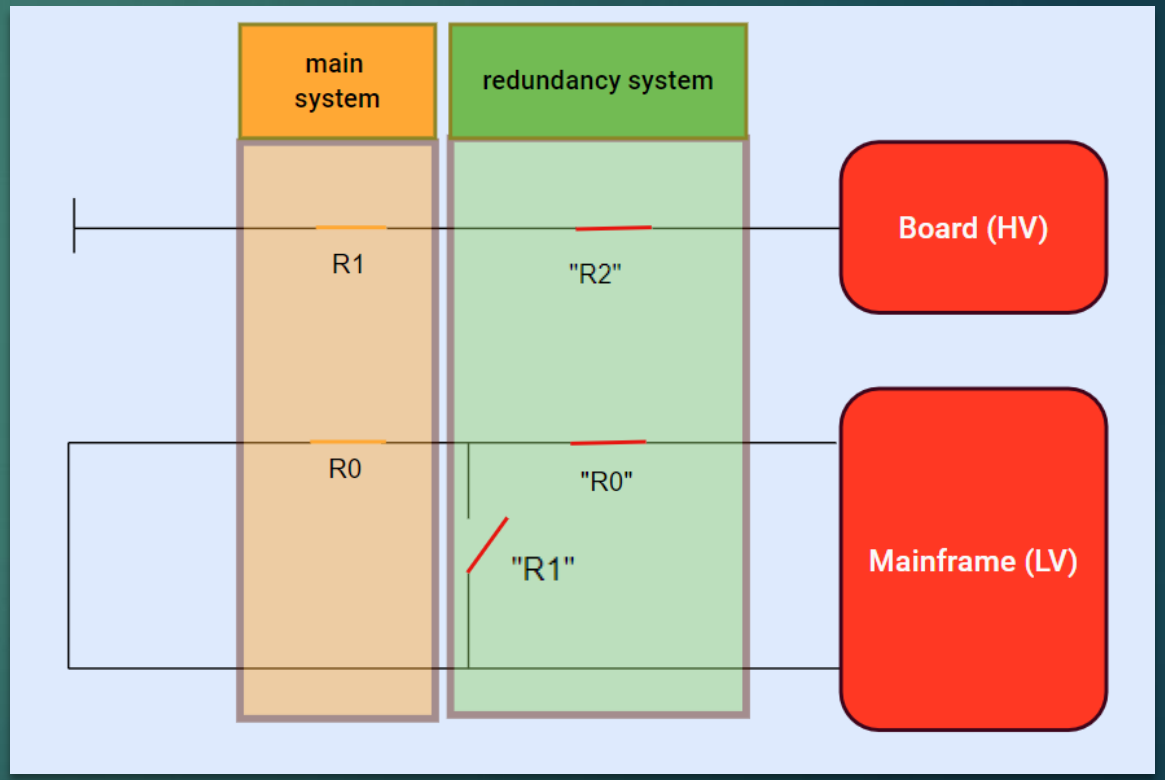
The redundancy of the system

- The secondary system reads HV and LV status, so it always knows the detector configuration
- It drives three relayes (“R0”, “R1”, and R2”) in such a way to switch-OFF the detector if necessary (in the correct way)



The redundancy of the system

- During the working phases the secondary system allow to the main one to control the detector state
- If the main system stops working, the second one get the control of the interlock signal



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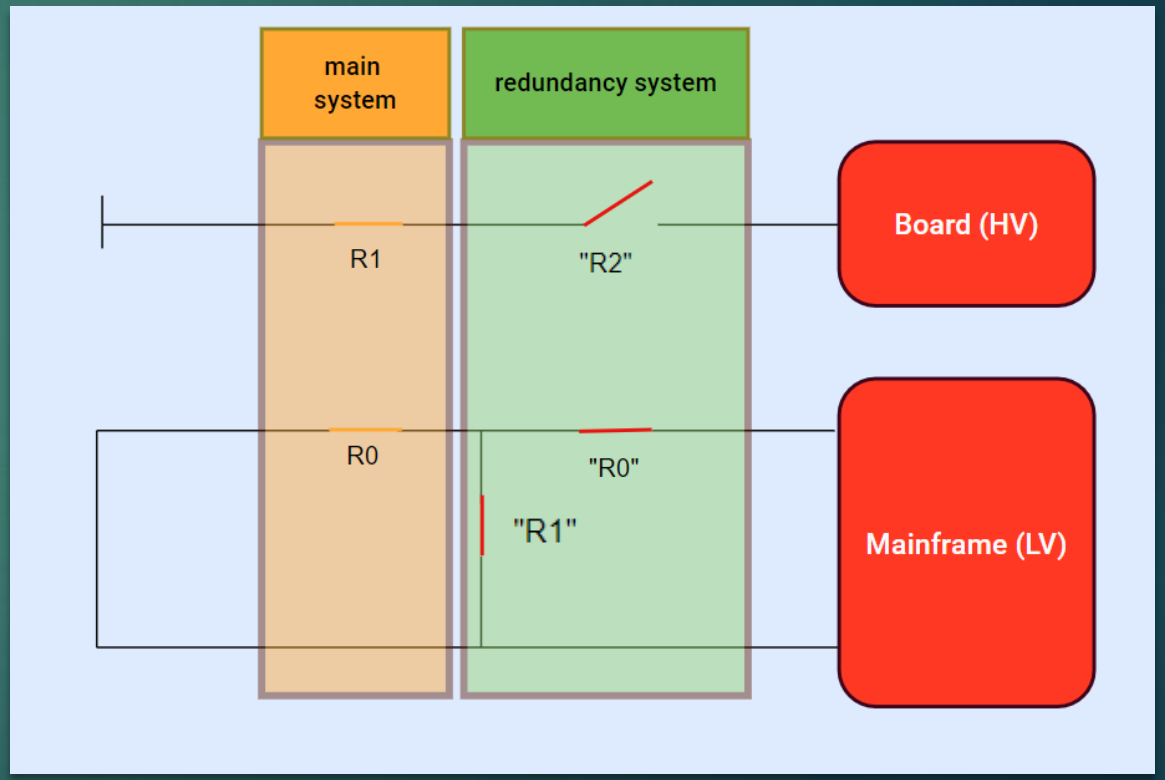
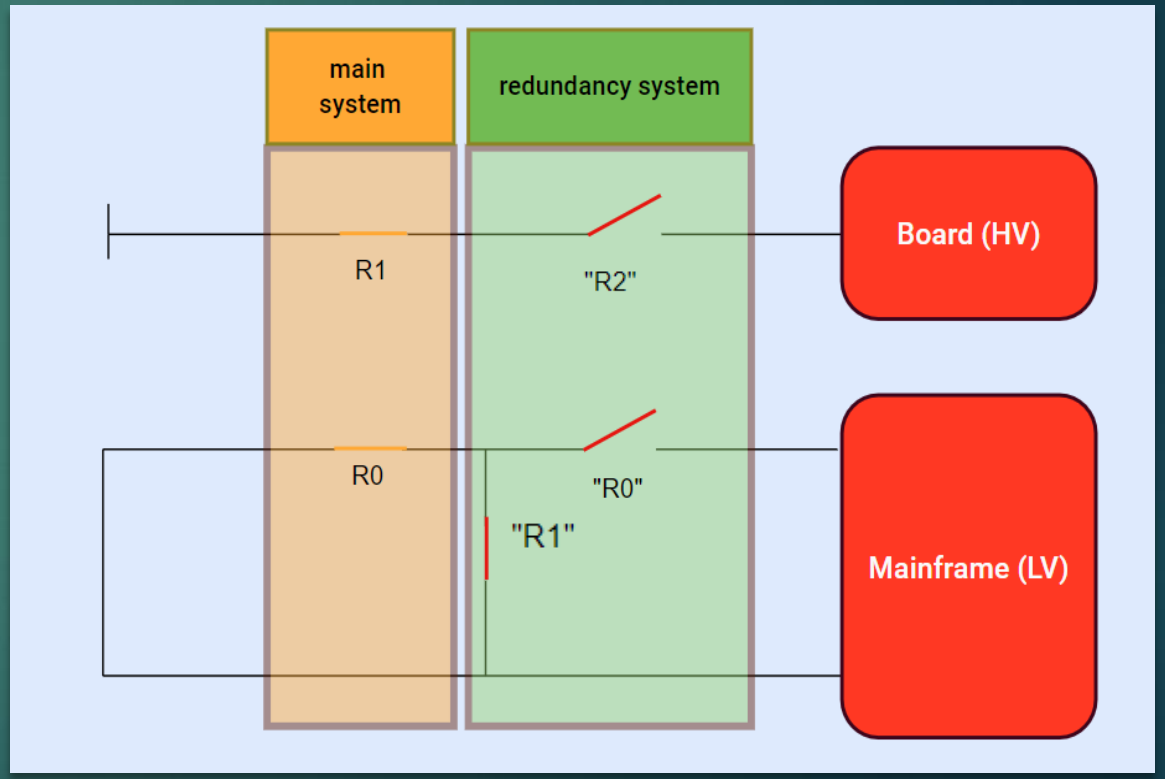


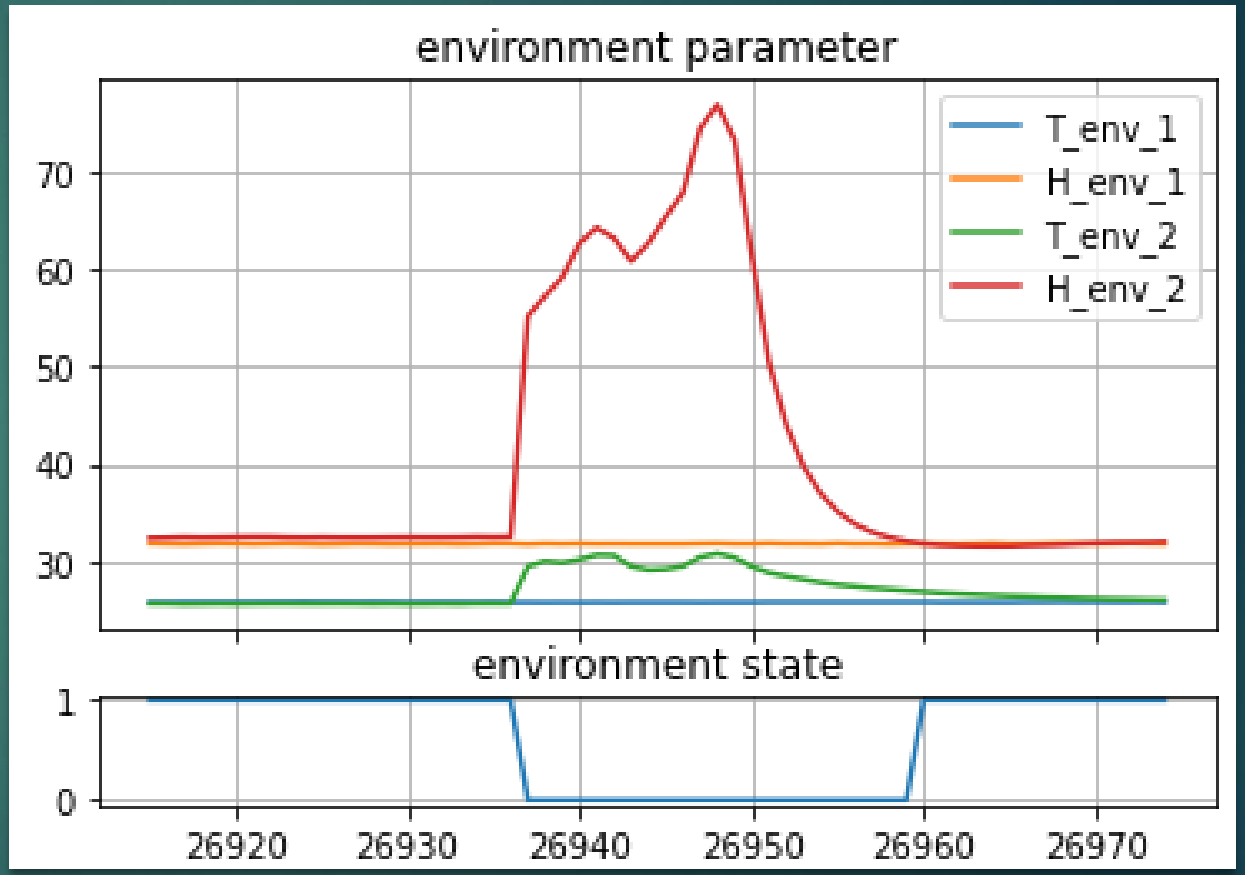
The redundancy of the system

- A crucial point concerns 'R0' and 'R1', since if they are blocked, the LV can remain turned-ON all the time.
- The fact that the realys are normally open makes this less probable
- However, the development of this part of the system will be the subject of further debate



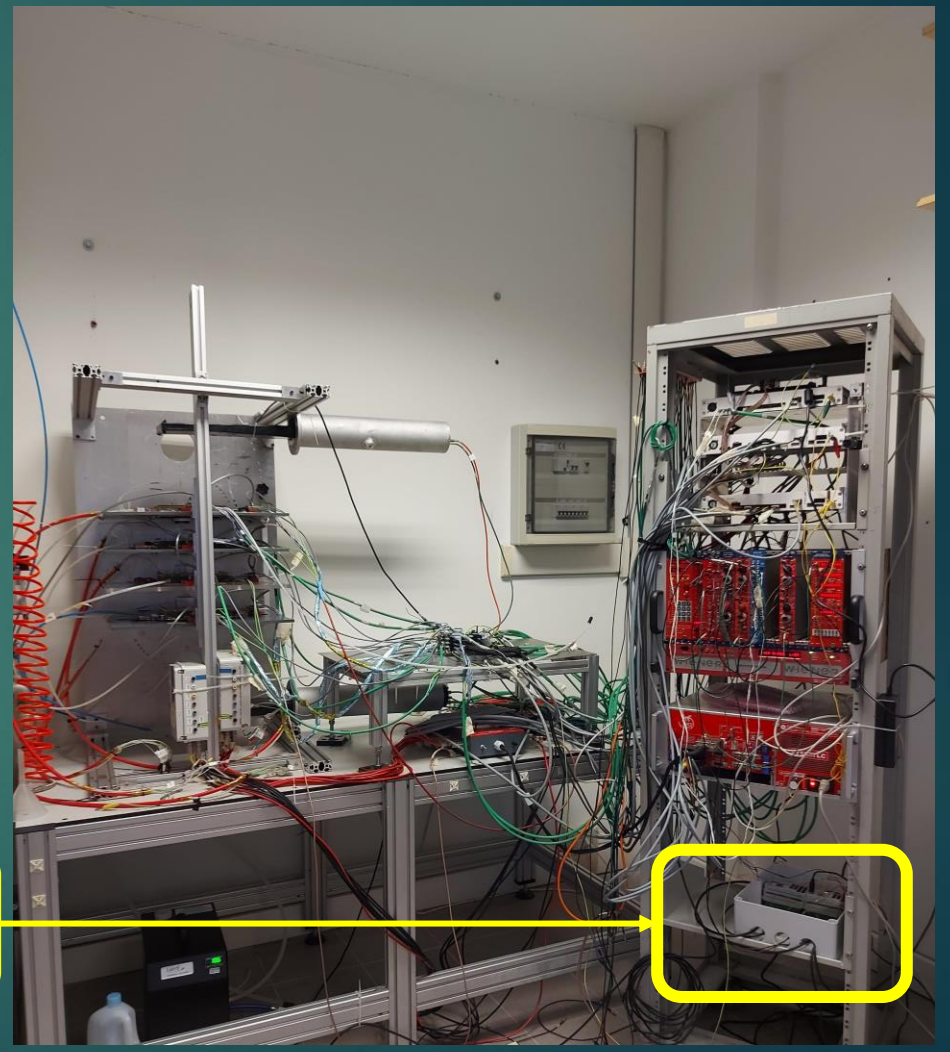
Plot example of the read parameters and the relative state

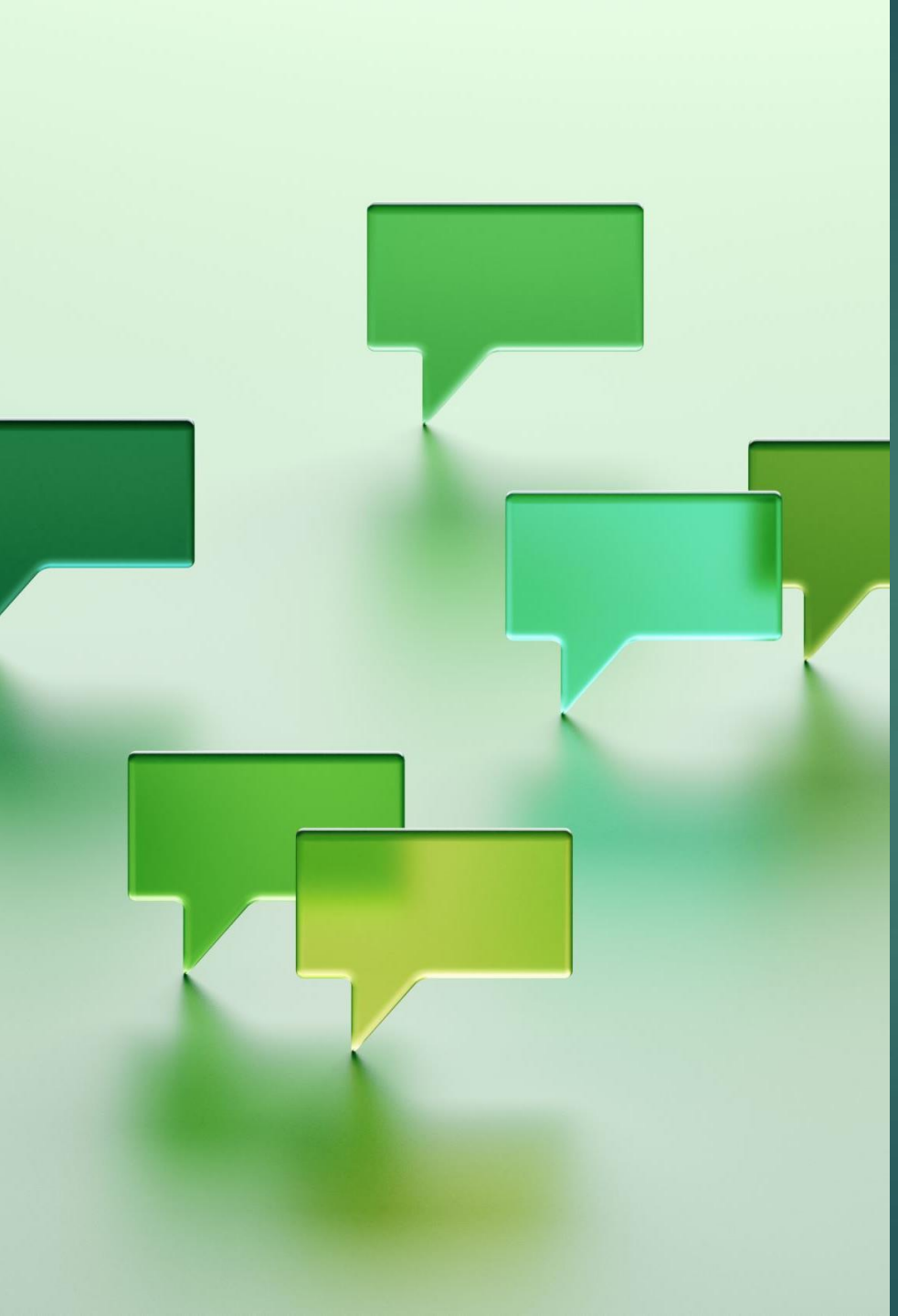
- In figure the plot of the environment humidity and temperature vs Number of measures
- In normal conditions, it saves 1 measurement every 5 seconds, while under alarm it saves all measurements taken
- The upper threshold 30°C and 80%, reentry values 27°C and 60%



Where we are…

- The first prototype of the system was installed in the setup in 334
- The most appropriate values for the thresholds are being evaluated
- The logic, the sensors and communications (with the sensors and with the laptop) are being tested
- The tests regard short transition between the state and long periods of operating to verify the stability of the system





Final comments:

- We are looking for ways to get information from HV (hopefully for updates in the coming months). A firmware modification is asked to CAEN in such a way to have these information
- Further implementation of the redundant system is being considered, (with an additional set of sensors to improve the security of the system, and a different way to interact with the detector)
- This preliminary work could be the basis for the development of slow control

Thank you for your attention