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The front-end electronics of the Hyper-Kamiokande Far Detector.

Hyper-Kamiokande (HK) is the successor of the Super-Kamiokande (SK) experiment; HK has a world class physics programme including accelerator neutrino beam as well as search for proton decays and neutrino from sun, atmosphere and astrophysical sources. HK will be using the same 295 km baseline as T2K (Tokai2Kamioka) but with a larger Far Detector (FD) fiducial mass than SK and a higher beam intensity obtained by upgrading the J-PARC proton accelerator. The FD is a 258 kton water-Cherenkov consisting of a 68m (diameter) by 71m (height) cylindrical-shape water tank. The FD is divided into 2 parts: an *Inner Detector* (ID), instrumented by 20000 20" PMTs, surrounded by an *Outer Detector* (OD), consisting of 3600 3" PMTs looking outwards and acting as a *veto* for the ID.

This contribution describes the front-end electronics developed for the ID; the key point of the circuit is the design relying on discrete commercial Integrated Circuits. The circuit is divided into 3 sections: the first is the *input receiver*, which matches the impedance, buffers, and shapes the PMT input signal; following the receiver there are the *timing* and *integration* paths: the *timing* path consists of a fast discriminator which provides a trigger signal marking the beginning of a hit; the *integration* path converts the charge of the hit into a voltage level, which is then sampled by an ADC.

An FPGA implements a 250-ps resolution TDC which time-stamps the analog trigger signal and reads the slow ADC that digitizes the integrated charge. The digitized hits are then formatted into packets and sent through a 3Gb/s high speed copper link to a close-by board, which, in turn, transmits data on a optical link to the DAQ backend.

This work will describe in details both the circuit working principle and its performance quantitative evaluation.

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