

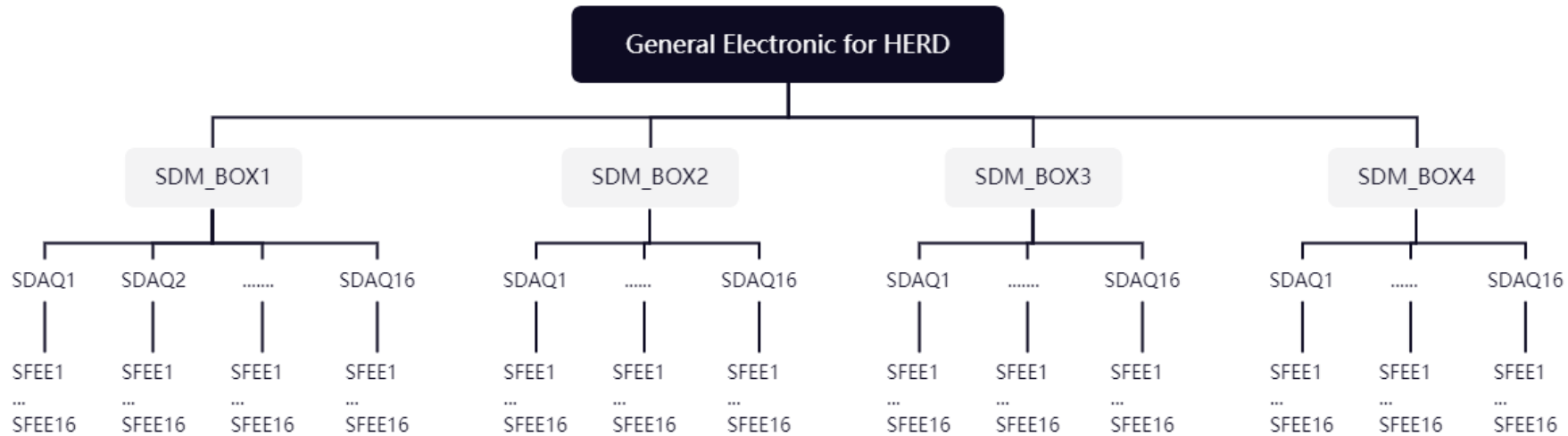
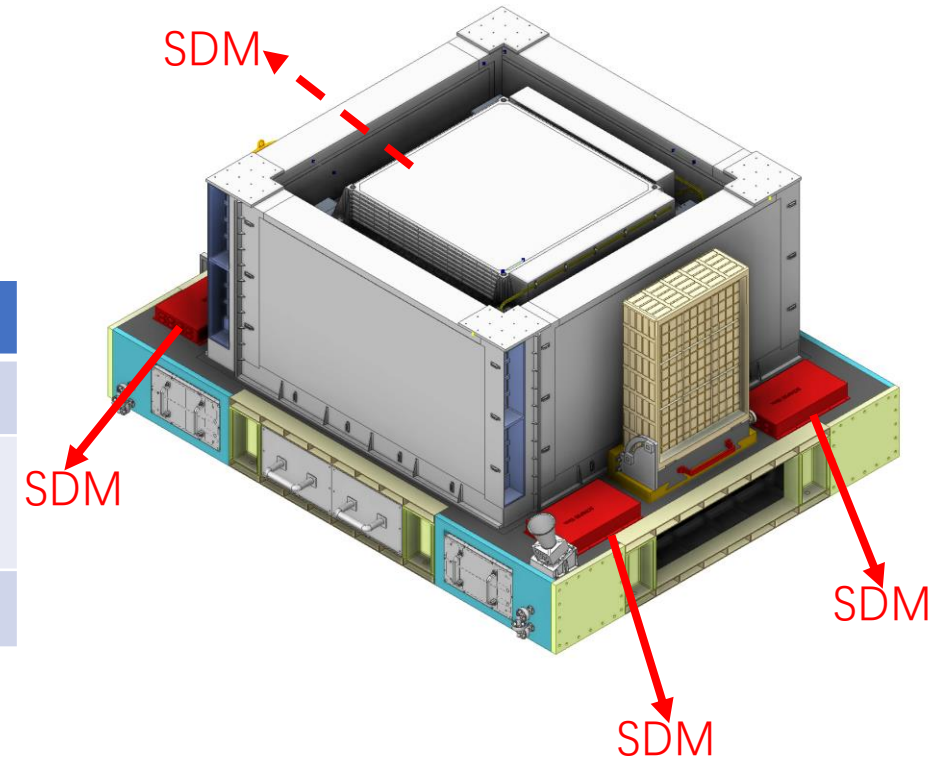
SCD Electronics

2022_12_19

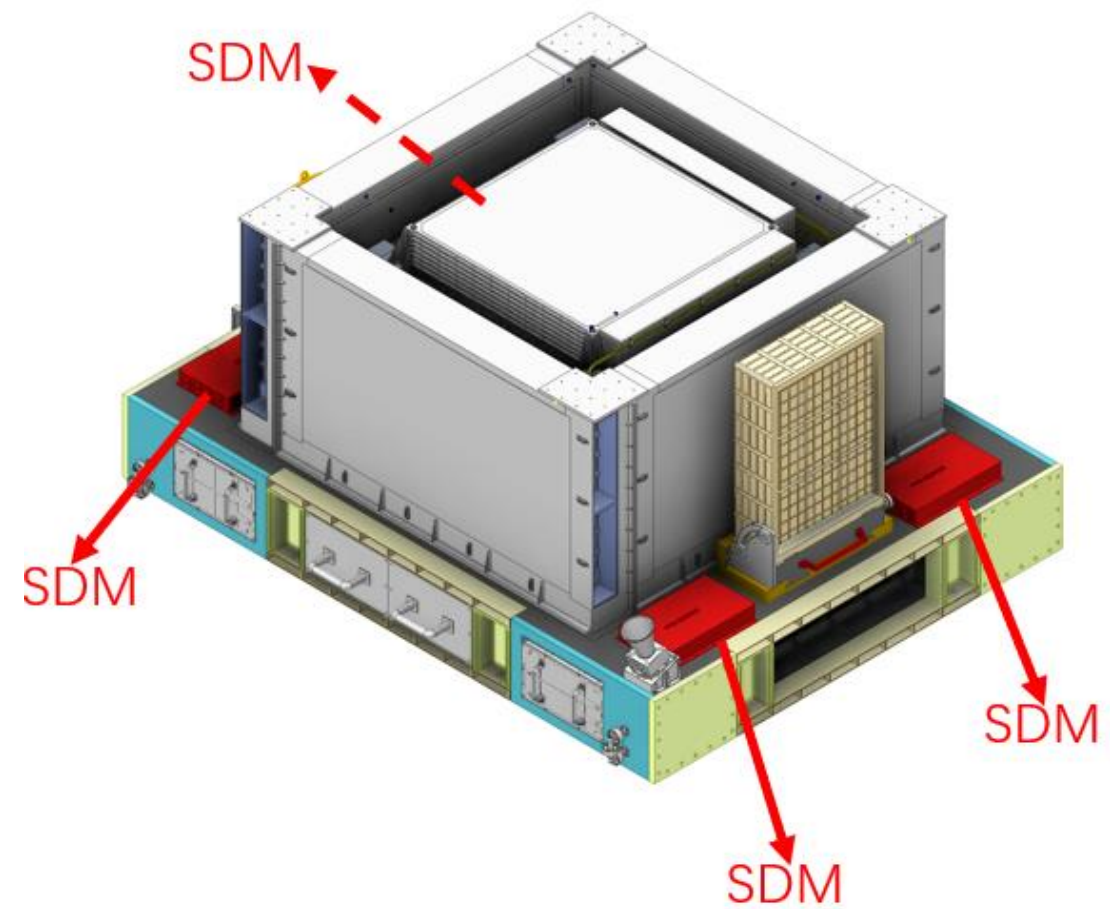
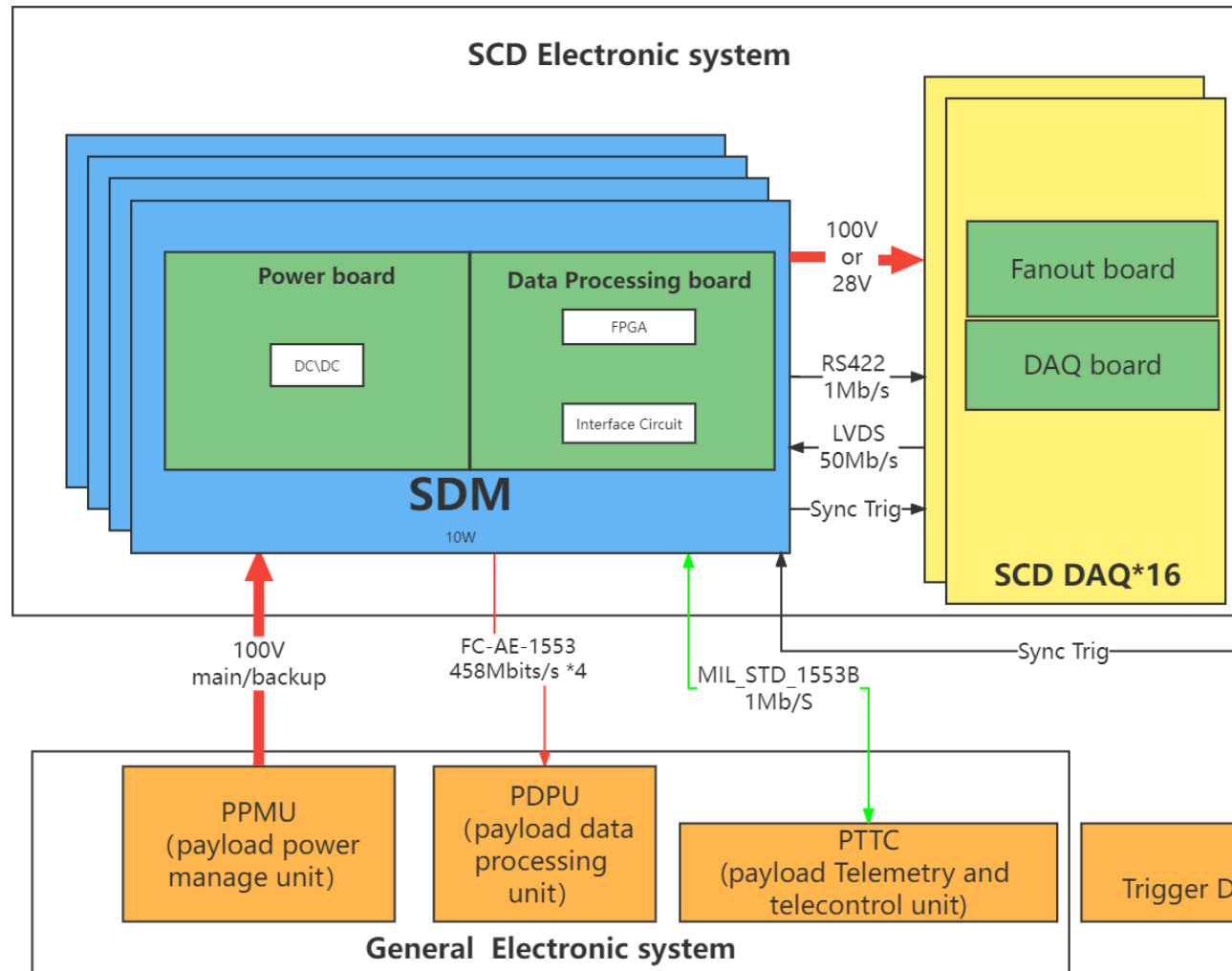
Ke Gong, Rui Qiao, Wenxi Peng, Ruijie Wang

SCD Readout Electronics Architecture

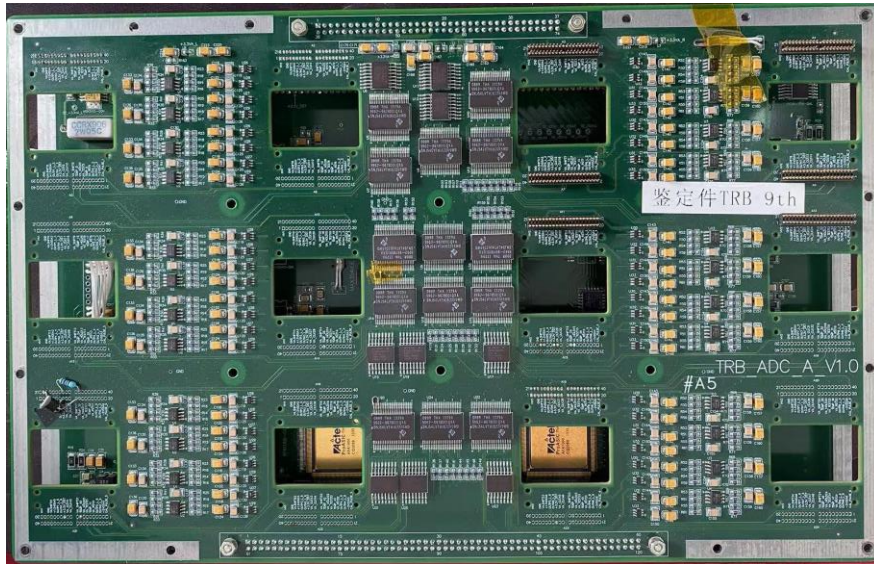
Submodule for SCD	function
SDM	DC/DC, data compression & transmission
SDAQ	RAW Data packing, Level shift, ASIC ctrl fanout
SFEE	Front end preamp , ADC



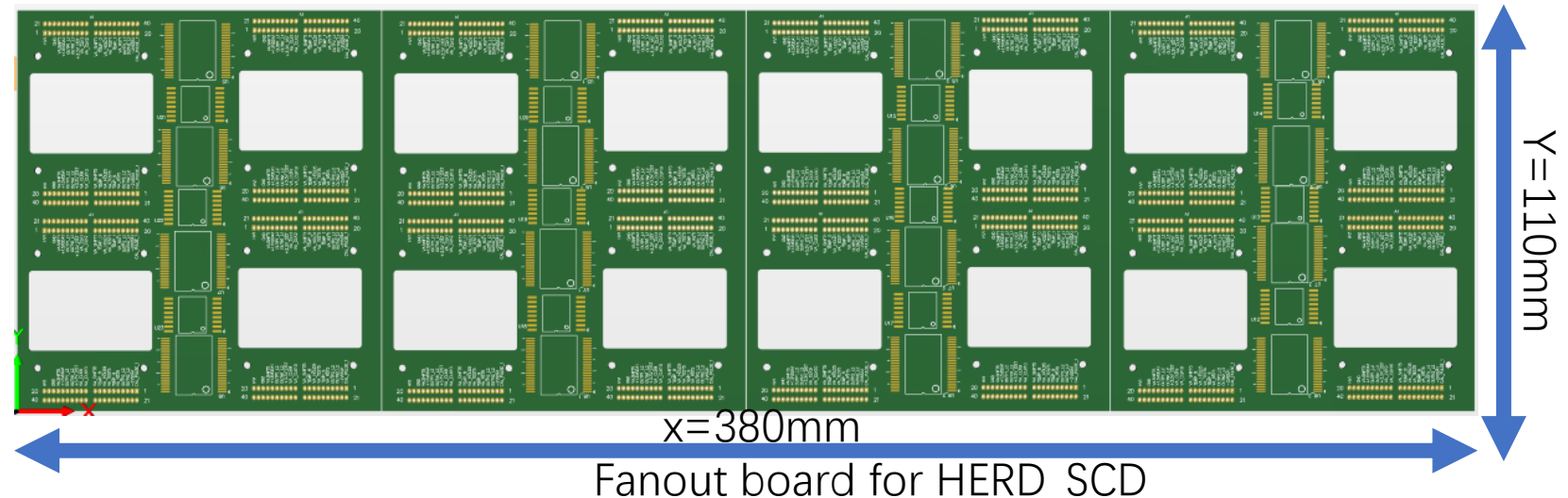
Input and output for SDM



Space we need for side SCD Fanout

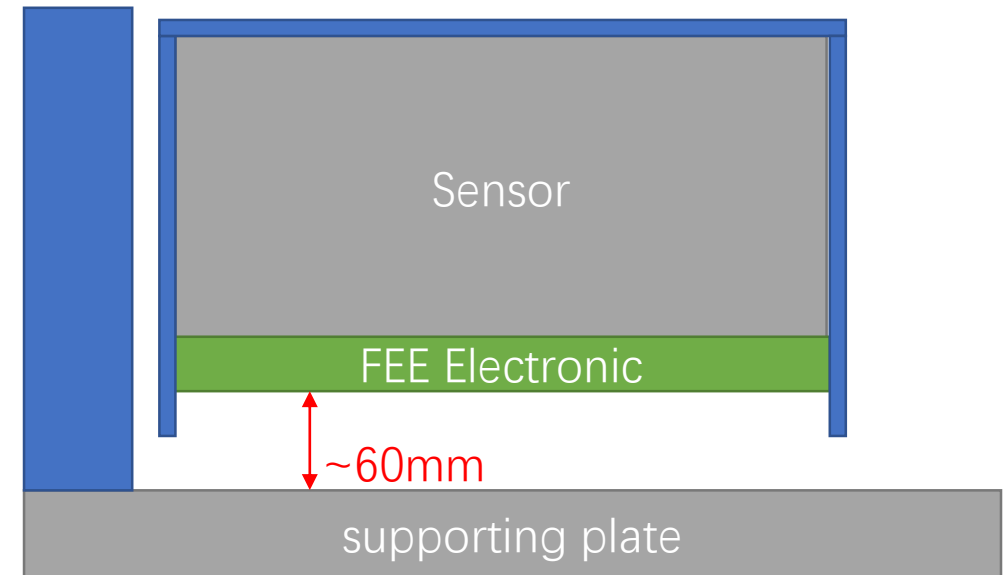
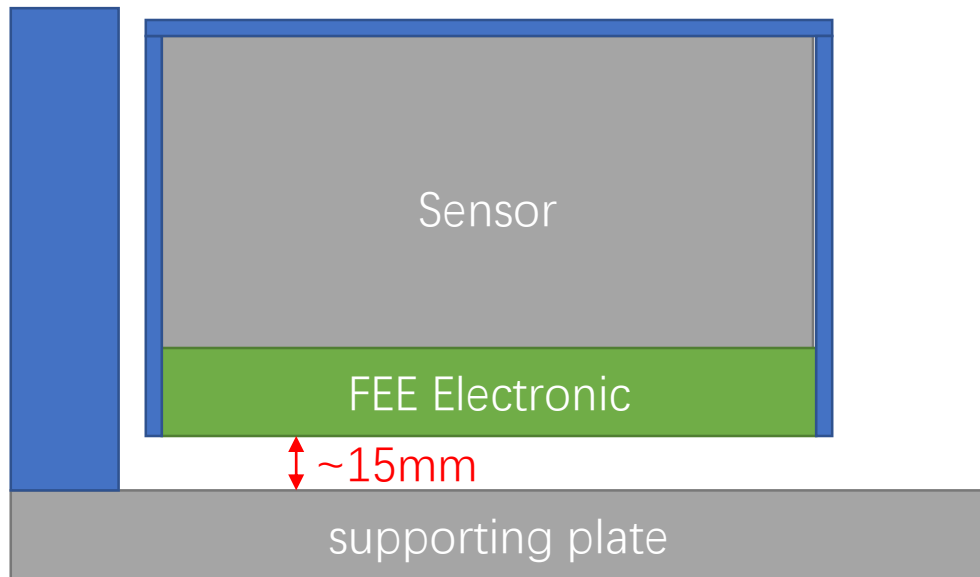


TRB for DAMPE_STK



Space we need for side SCD Fanout

Can we limit the size of the ASIC readout electronics, from 100*100mm to 100*55mm?



Front-End readout chip selection

- 1.IDE1140 --- space experience、 low dynamic range、 low power consumption、 no internal ADC
- 2.New ASIC designed in INFN-To

	Dynamic Range	ENC	Internal ADC	Power	Supply voltage
IDE1140	+200fC	139e + 5 e/pF	No	20mW total	+1.5/-2
ASTRA64 (INFN-To)	80 or 160 fC	ENC<1000 e	YES	<1mW per channel	1.2V

Next step

1. back-end electronics design based on the ASTRA64 ASIC.
2. Start the electrical model design.