SuperB EMC Electronics

La Biodola SuperB Workshop May 28 June 2, 2011

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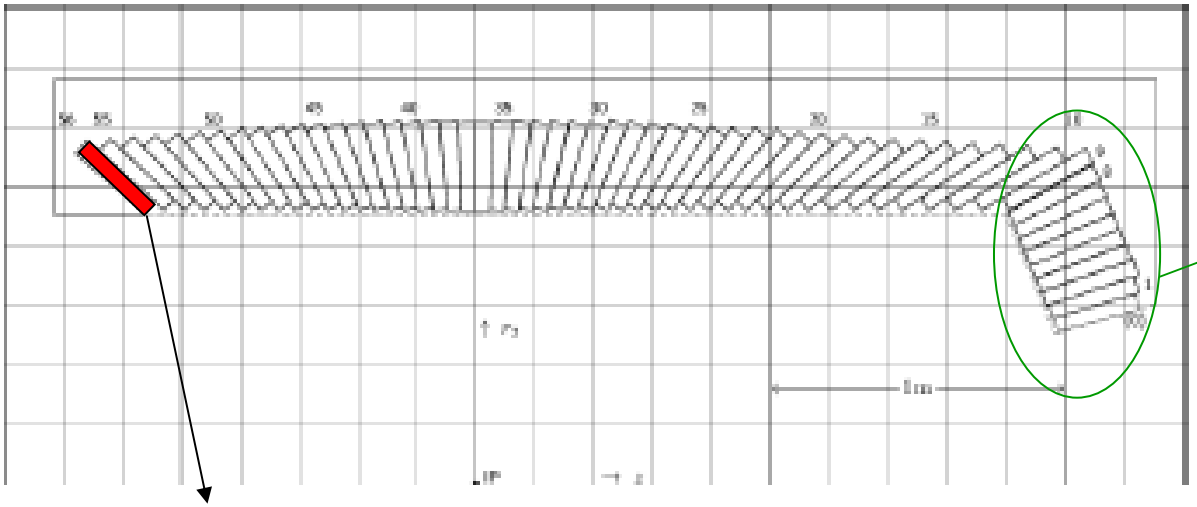
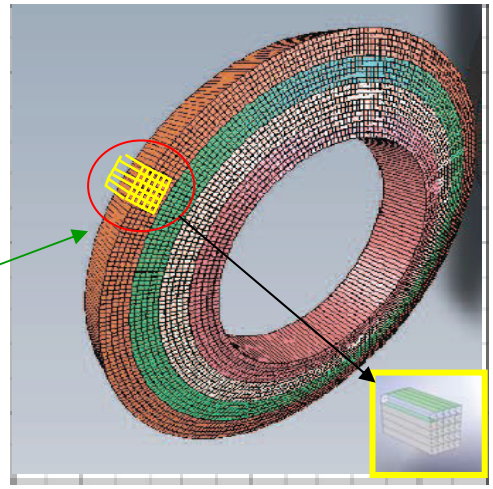
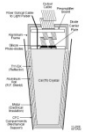
INFN Roma

EMC electronics: INFN Roma,INFN Perugia

SuperB EMC



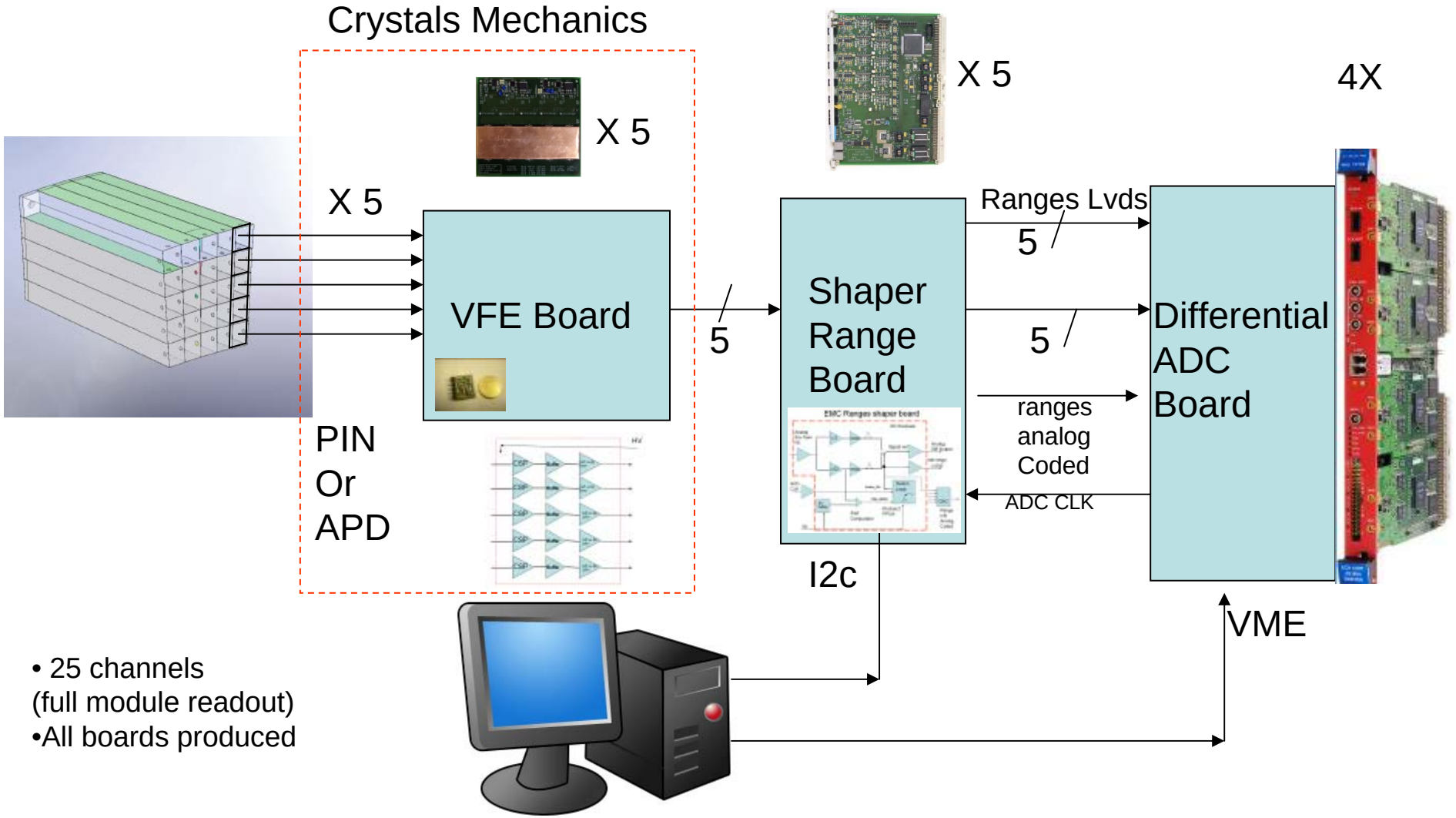




EMC Barrel :
5760 CsI(Tl)
Crystals

EMC Forward =
4400 Lyso (BGO ?)
Crystals
(176 modules)

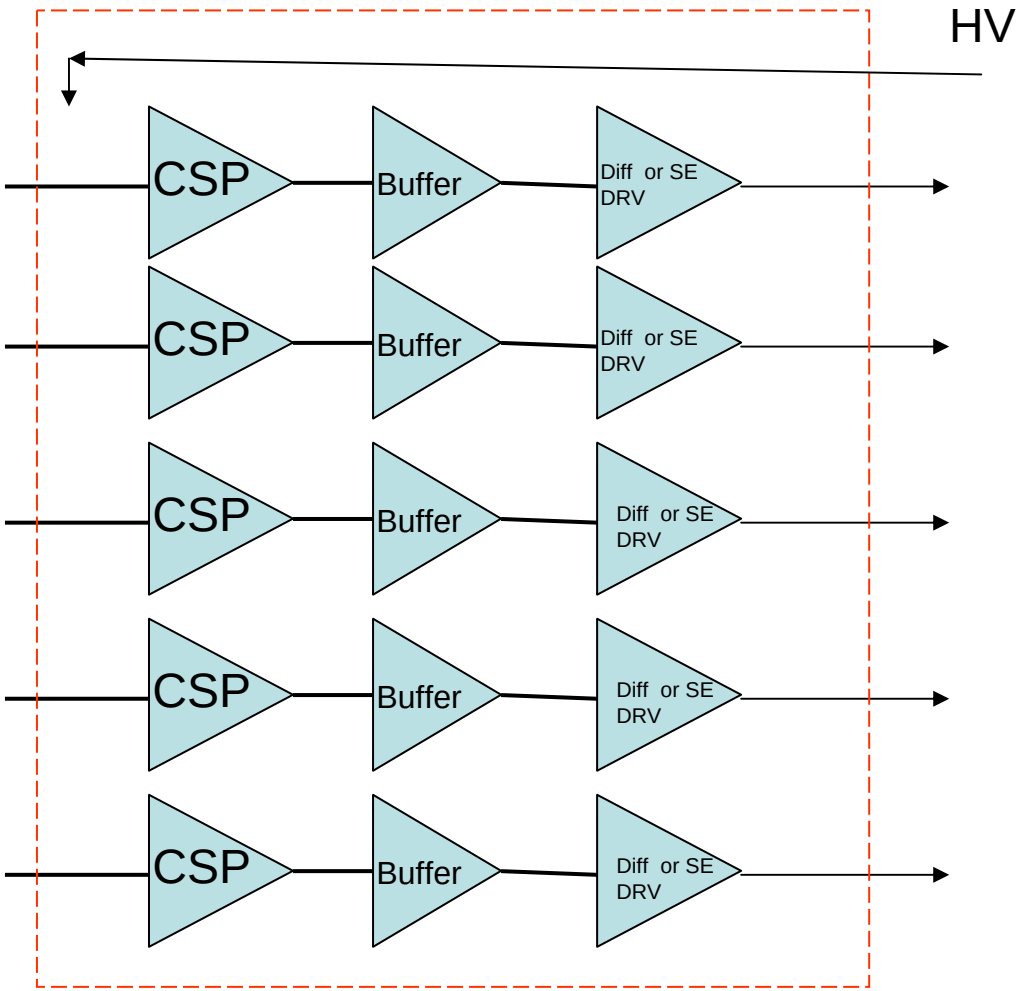
25 crystals tower readout electronics



- 25 channels (full module readout)
- All boards produced

Very Front End Board

- EMC VFE Board
- 5 CSP Channels
- Enable to mount: Cremat, Hamamatsu, Home Made CSP
- HV distribution



Very Front End Board

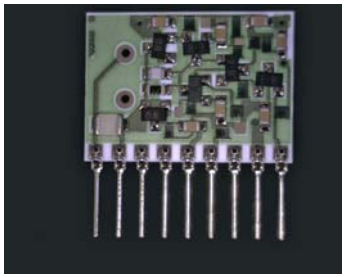
(PCB layout D. Ruggieri, A.Papi)

- EMC VFE Board
- 4 Layers
- 5 CSP Channels
- Enable to mount:
  Cremat,Hamamatsu,Home Made CSP
- HV distribution
- Mounted on crystals
- Interface with EMC range Board

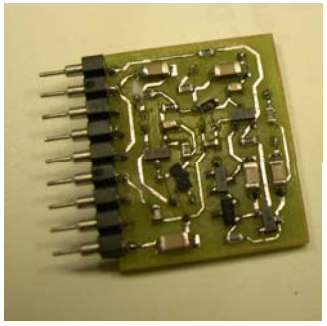
Three Type of CSP under evaluation

Cremat 1.4 V/pC

Hamamatsu 1 V/pC

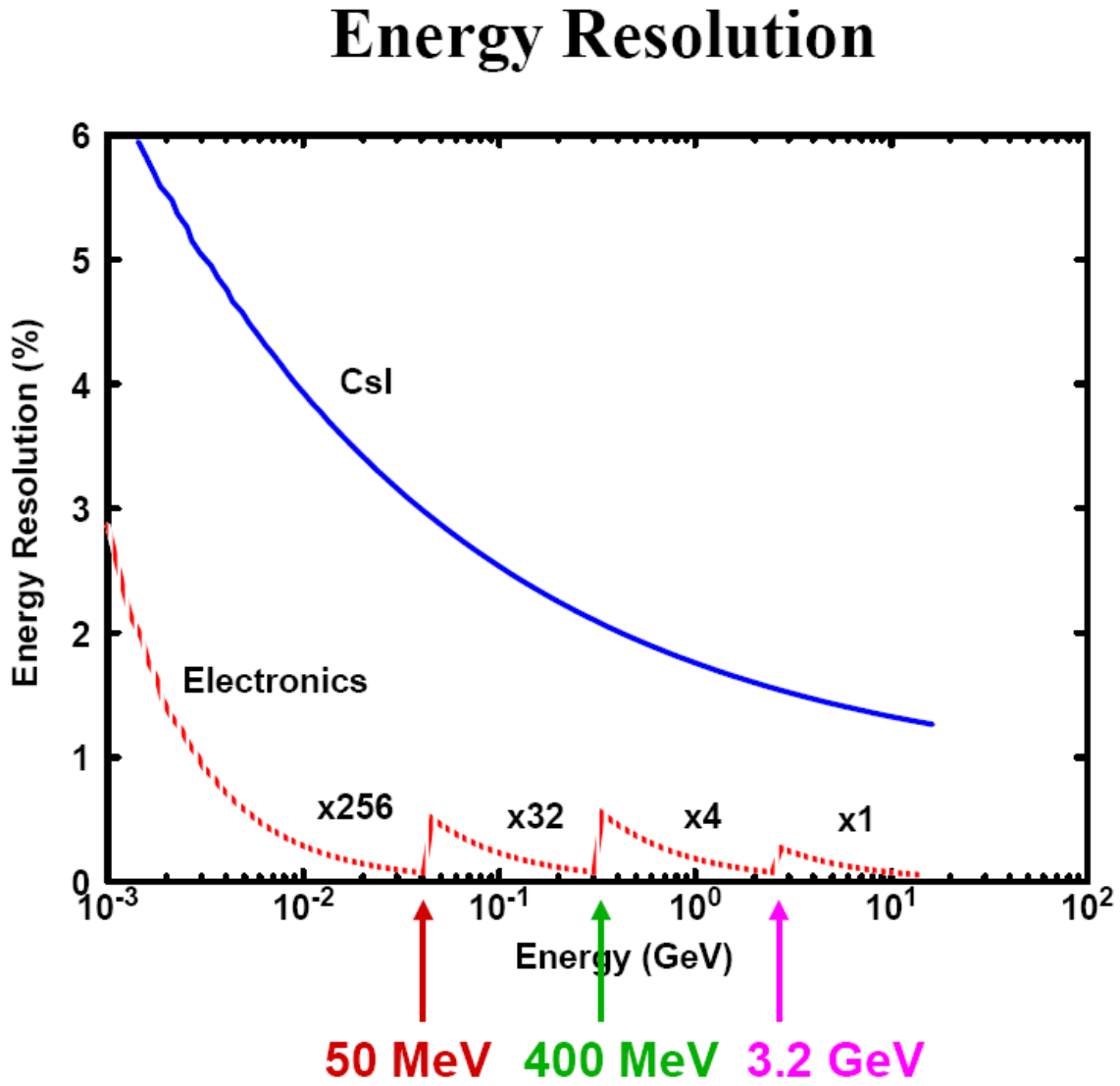


Homemade 1 V/pC

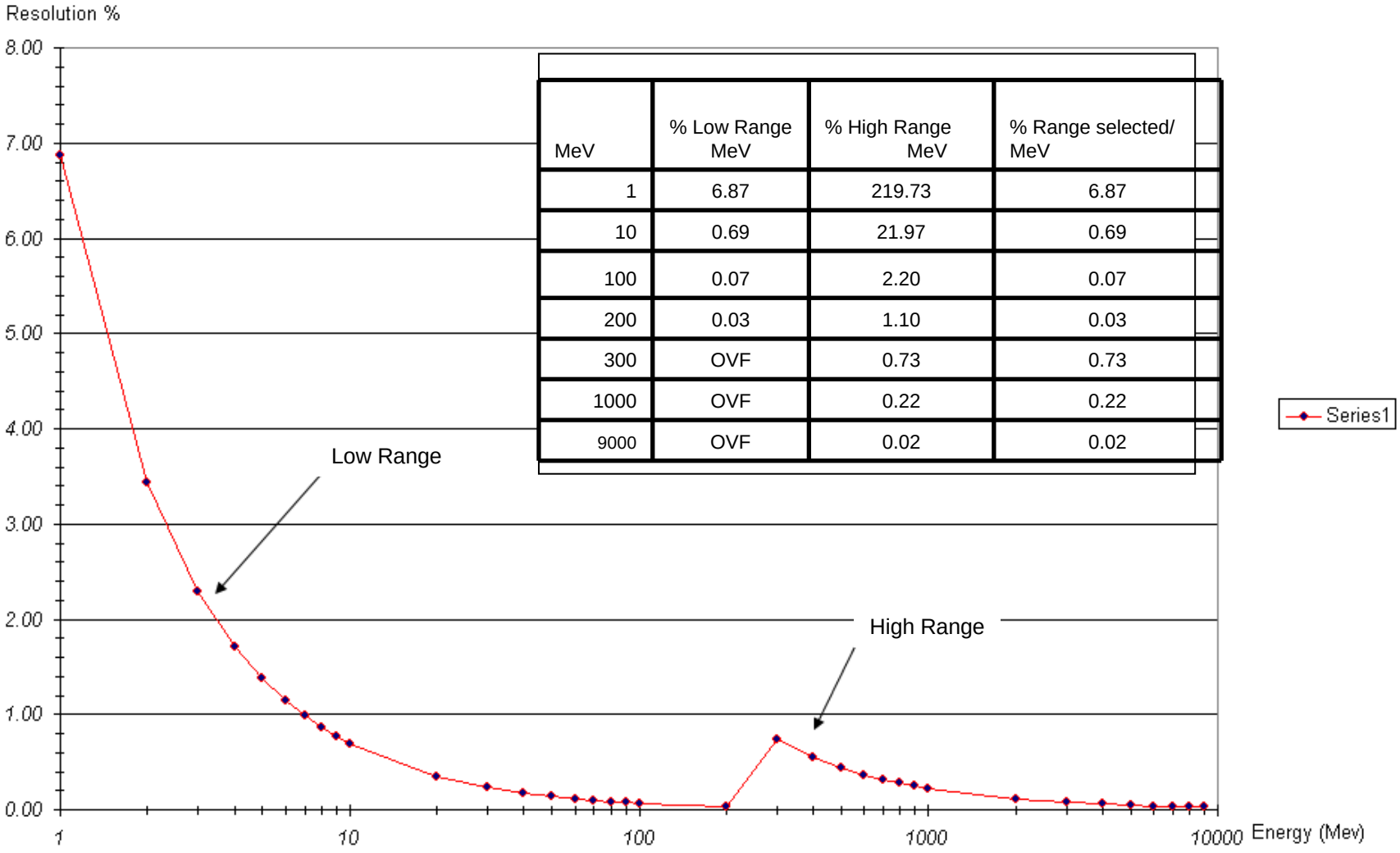


WE can change Rf constant.

Babar Energy resolution

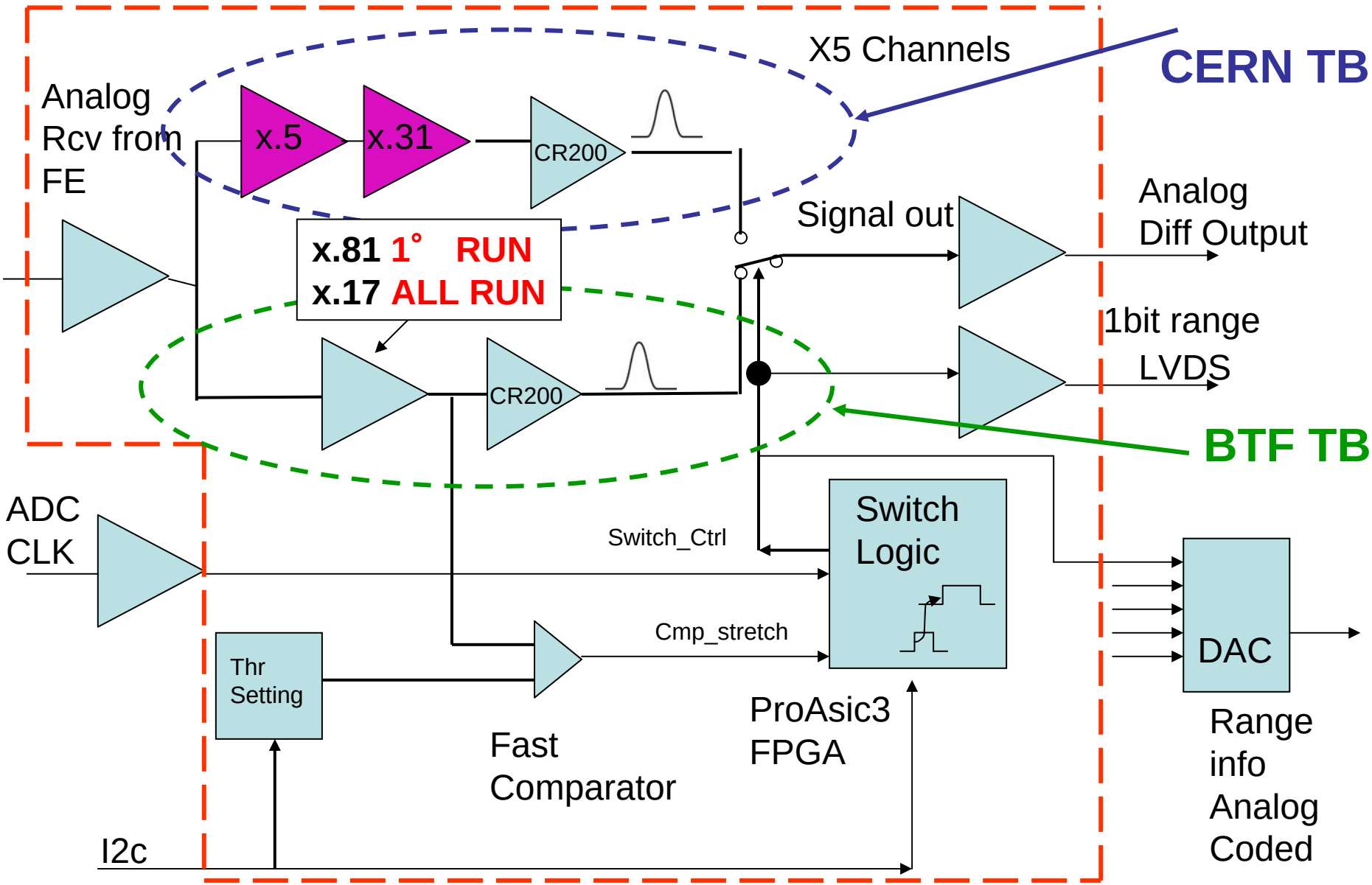


Energy Resolution SuperB



MeV	% Low Range MeV	% High Range MeV	% Range selected/ MeV
1	6.87	219.73	6.87
10	0.69	21.97	0.69
100	0.07	2.20	0.07
200	0.03	1.10	0.03
300	OVF	0.73	0.73
1000	OVF	0.22	0.22
9000	OVF	0.02	0.02

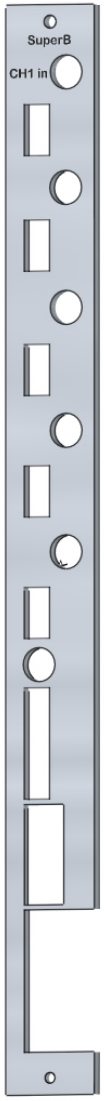
EMC Ranges shaper board test beam settings

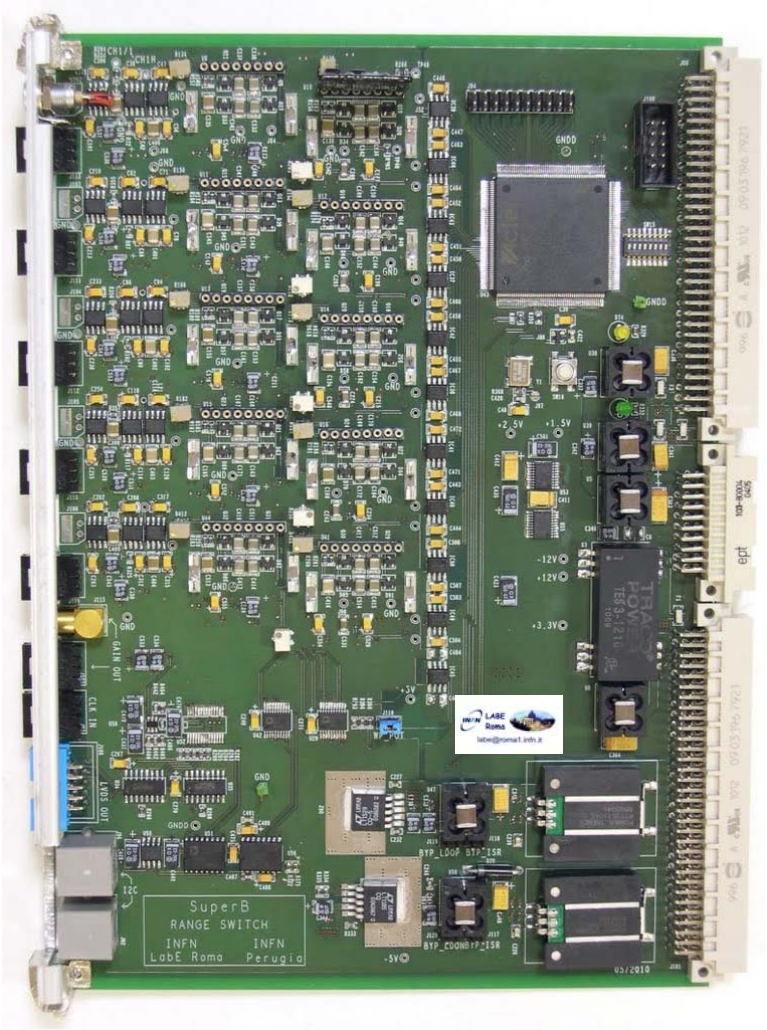


EMC Range Board

(PCB layout R.Lunadei,G.Chiodi)

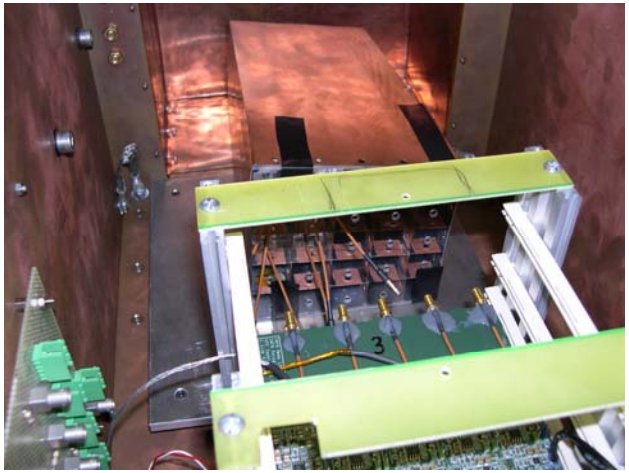
- EMC Range Board
- 8 Layers VME size
- 5 Channels Analog Differential input
- 5 Channles Analog Differential output
- 1 Main clock input
- Long line I2c control input
- Range info analog coded
- Lvds output for Range bit

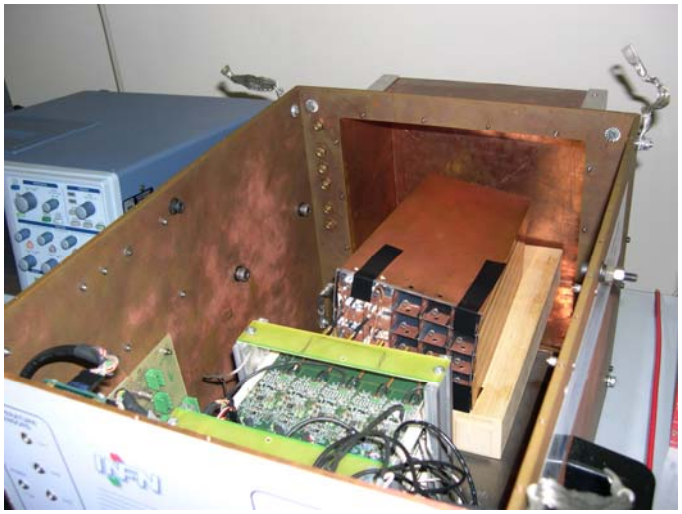


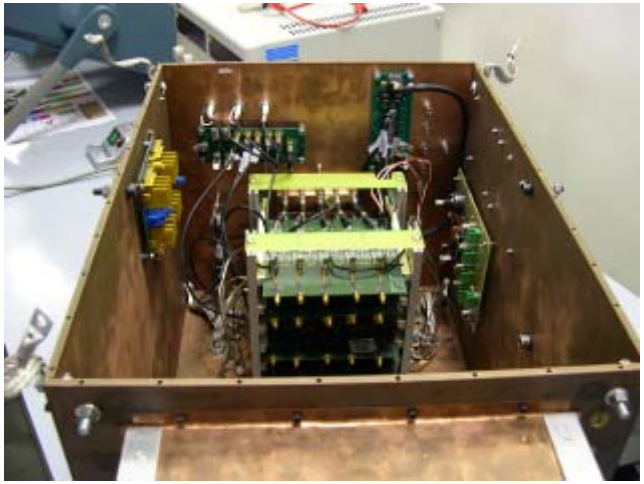


VFE inside the copper Box

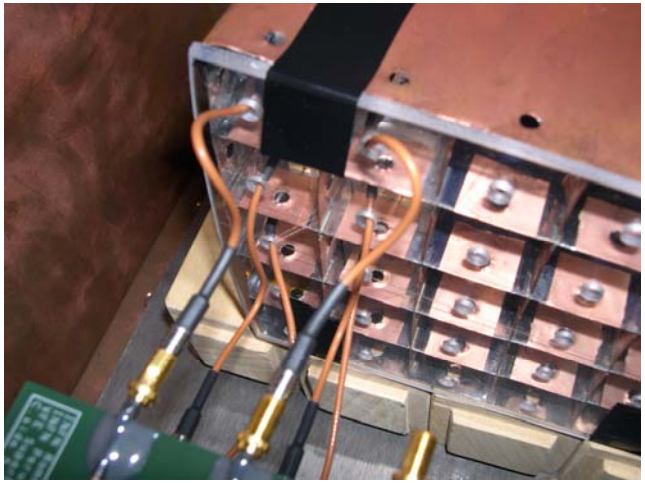
(INFN Perugia,INFN Roma)





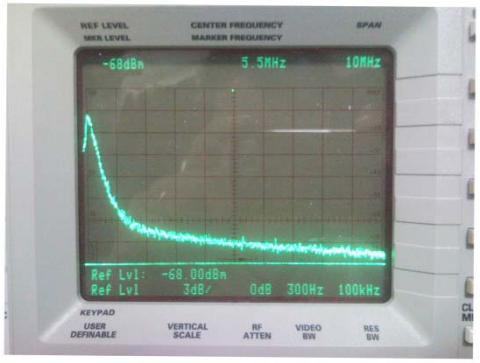


Cabling by M.Bizzarri

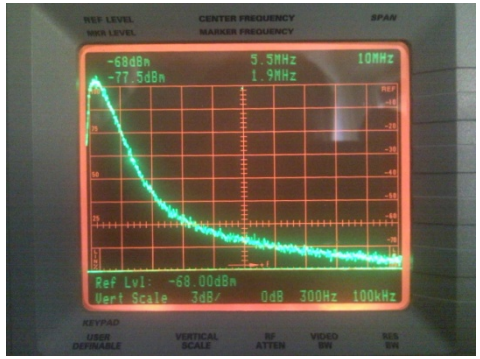


As we know the noise spectrum depends from the shaping time we do not find any noise source with an heavy contribution.

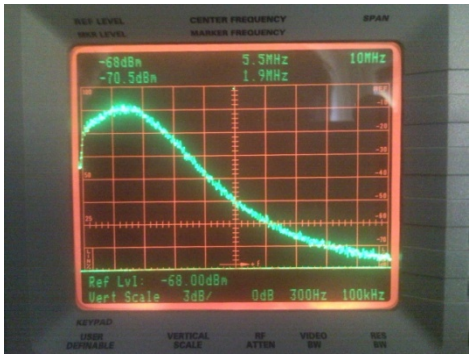
Power Spectrum 500 ns Shaper

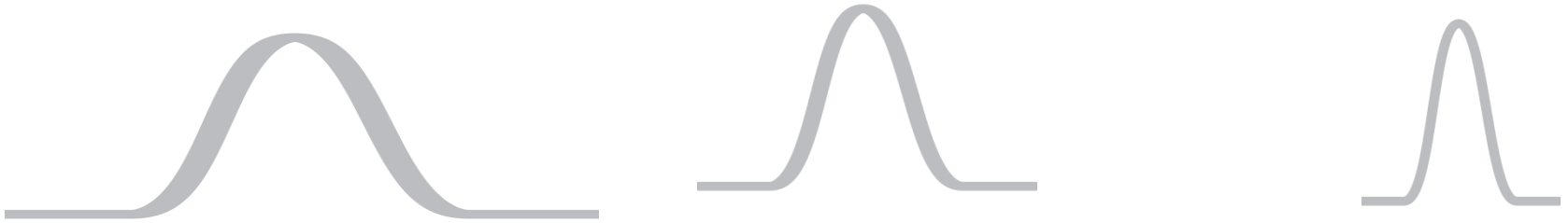


Power Spectrum 250 ns Shaper



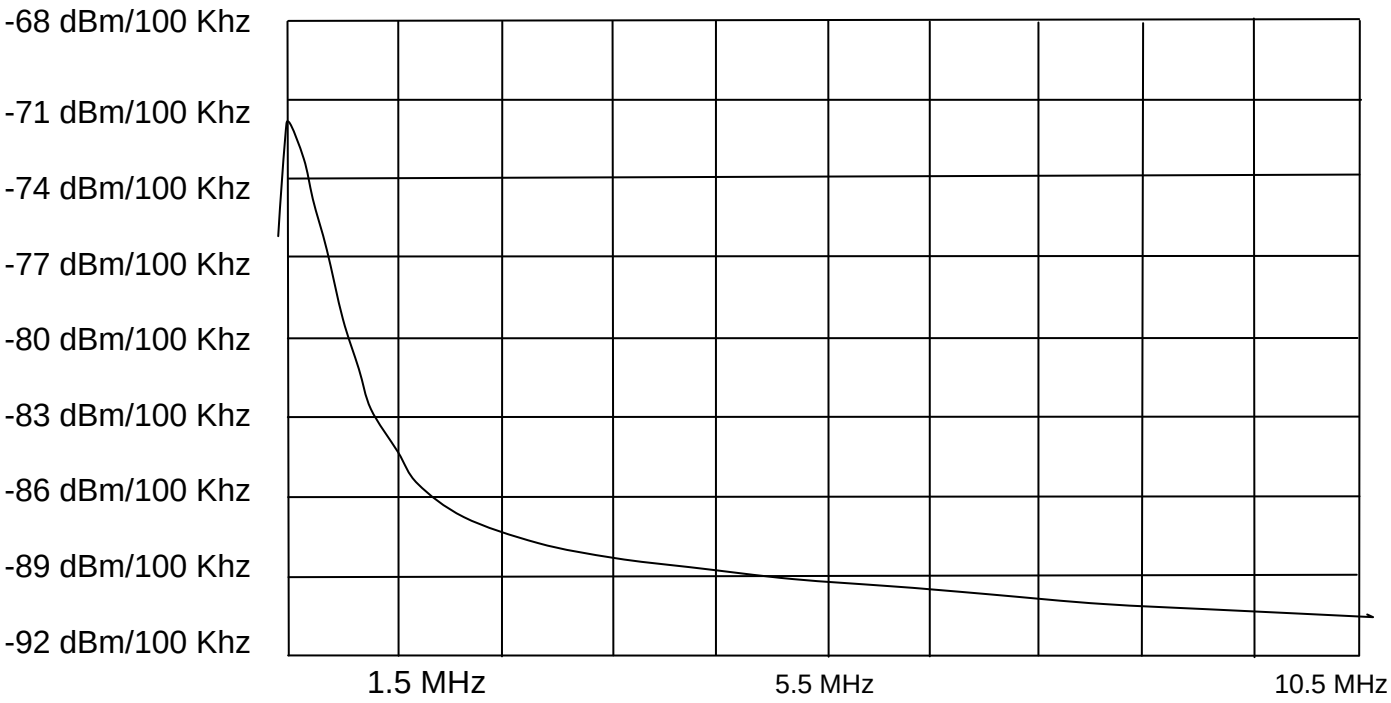
Power Spectrum 100 ns Shaper





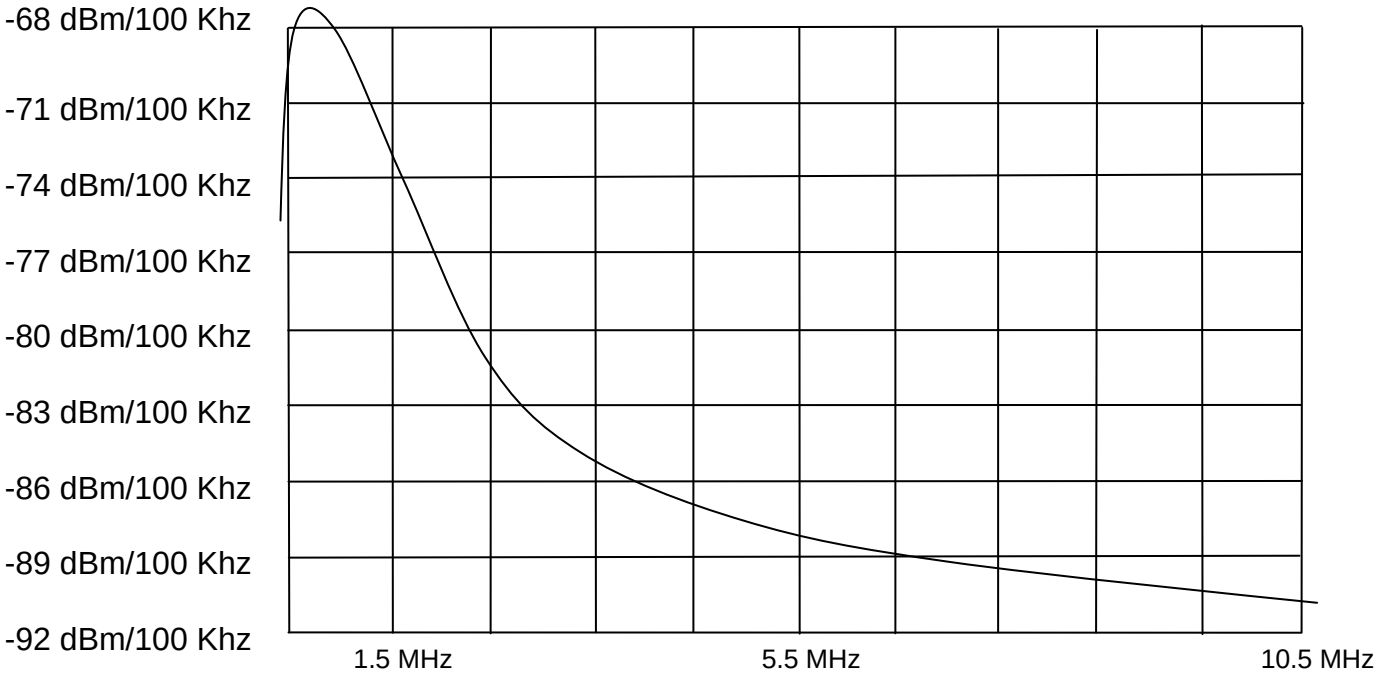
More noise

Power Spectrum 500 ns Shaper

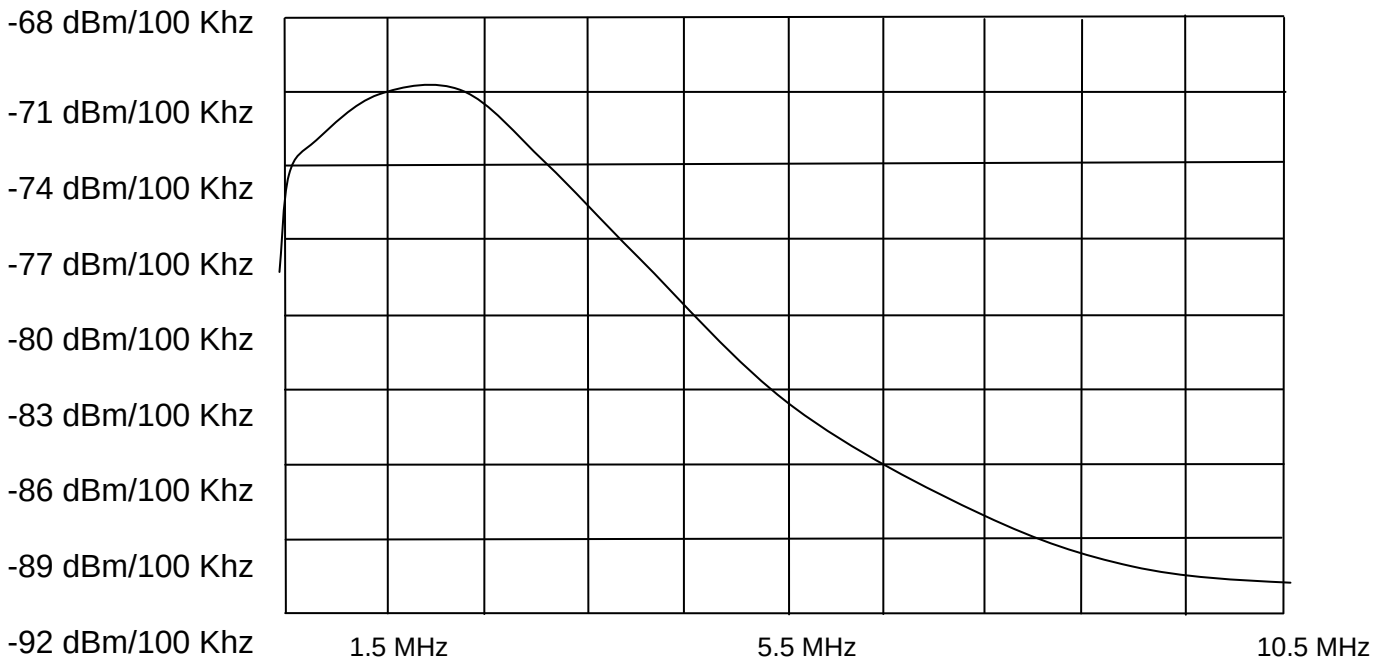


This is the shaping time used in LNF beam test

Power Spectrum 200 ns Shaper



Power Spectrum 100 ns Shaper



This is the shaping time used during the CERN and BTF test beam

We integrate the noise spectrum and we have evaluated the noise level in Veff

- **100ns -> 745 uVeff**(0.5-10.5 MHz)
- **200 ns -> 565 uVeff** (0.5-3.5 MHz)
- **500 ns -> 418 uVeff (0.1-2.1 MHz**)

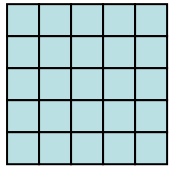
1 Mev 600 uv High Gain during CERN test Beam
1 Mev 180 uv Low Gain during CERN test Beam

EMC Fast Trigger Path and Slow Energy Path

Forward

$N_{cryst} = 25$

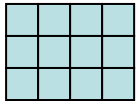
$N_{Towers} = 176$

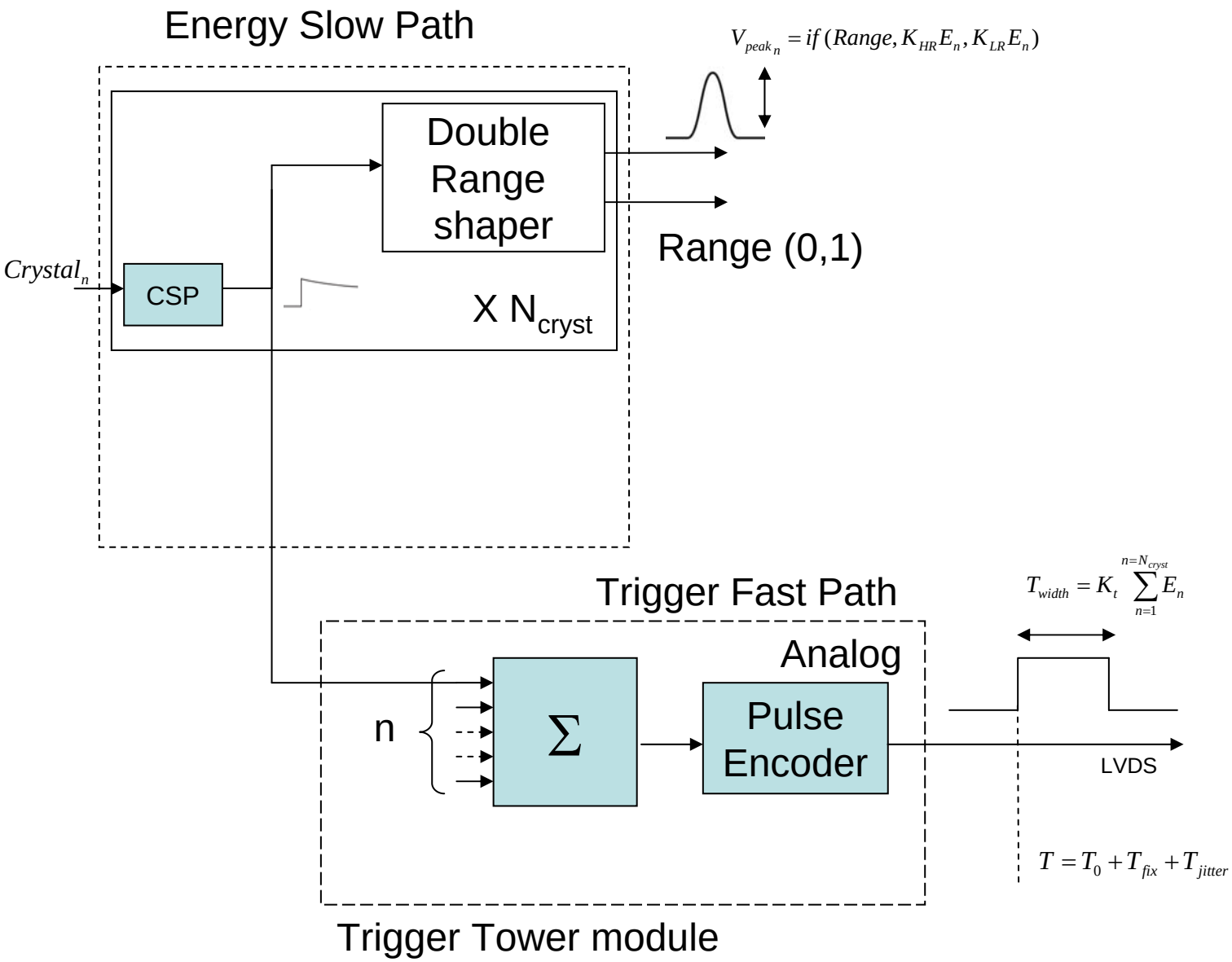


Barrel

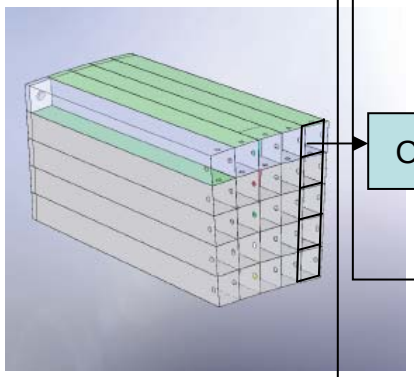
$N_{cryst} = 12$

$N_{Towers} = 480$





EMC Forward tentative of Implementation



5 x 5 =25 crystal tower

CSP

X5

5 input

Σ

VFE

X5

Double Range shaper

X5

Range

VME Range Shaper

New Circuit Analog Sum over 5 input.

5 input

Σ

Analog Pulse Encoder

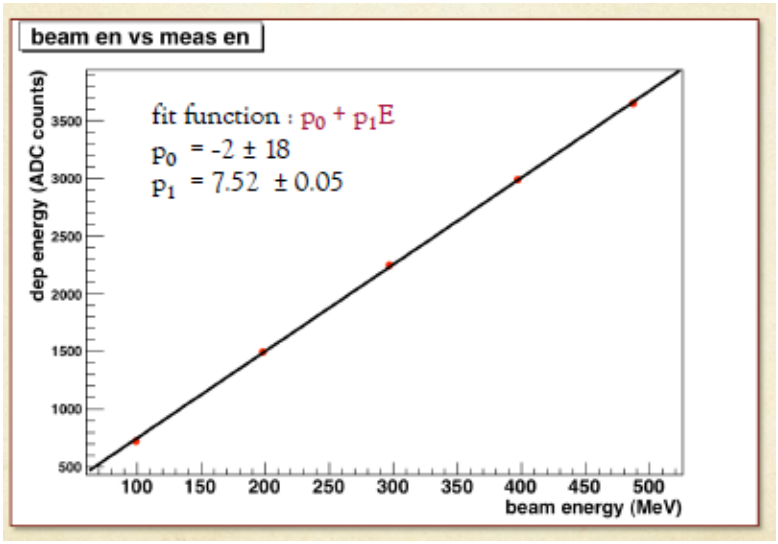
LVDS

$T = T_0 + T_{fix} + T_{jitter}$

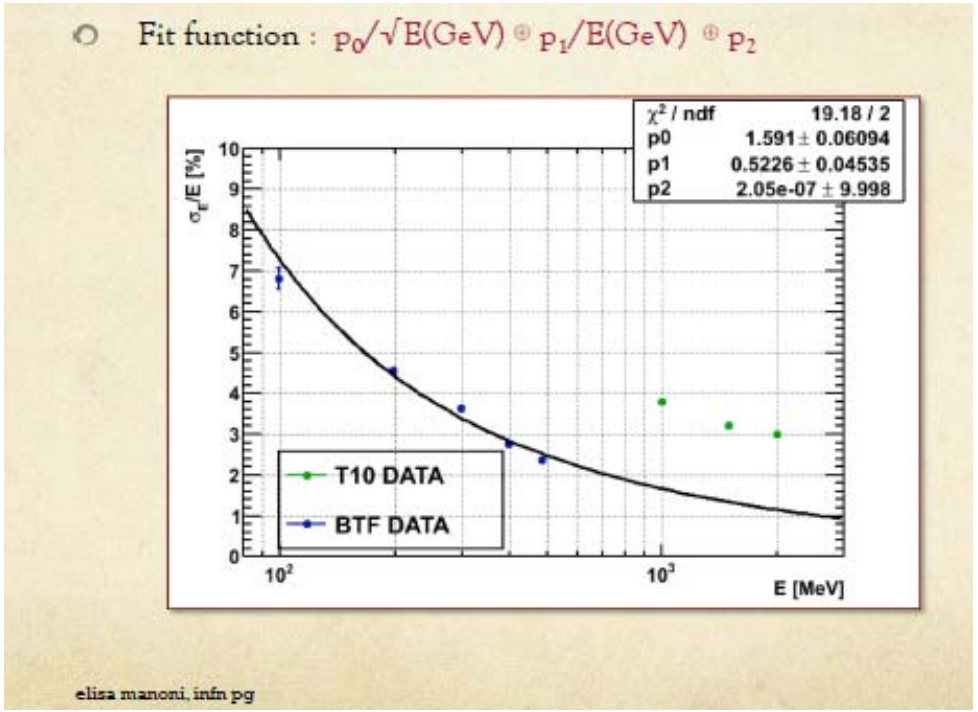
Trigger Tower module

X 176 lvds Links

May 2011 LNF BTF Beam Test

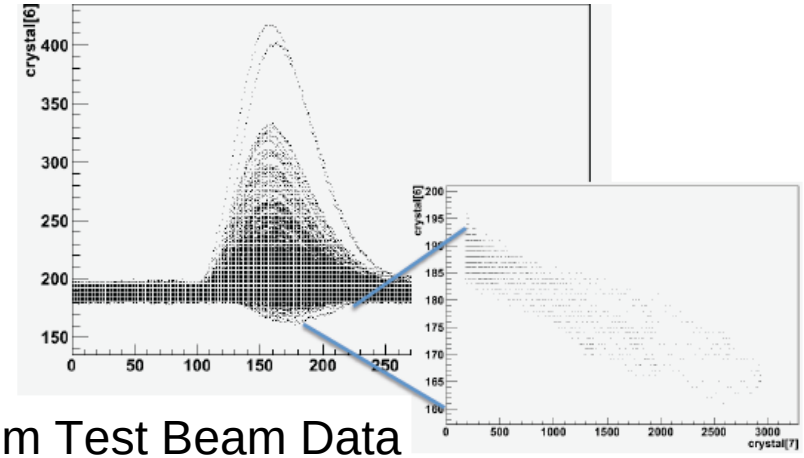


From Elisa Manoni Presentation

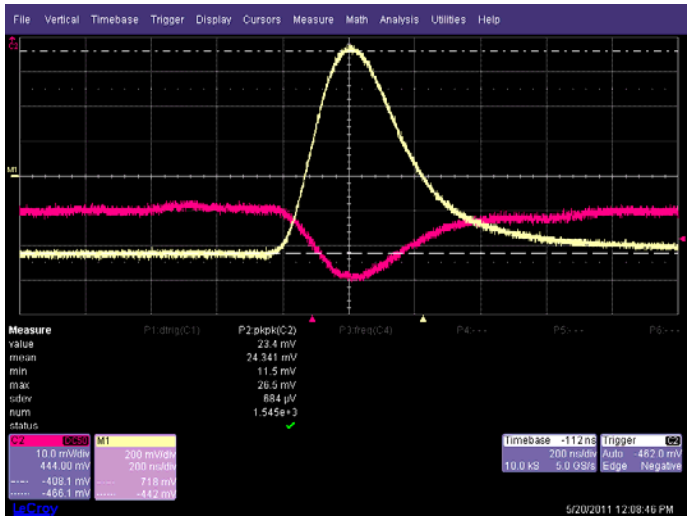


second order problems found during the test beam

Discovery of Xtalk Ch_{N-1} vs Ch_N

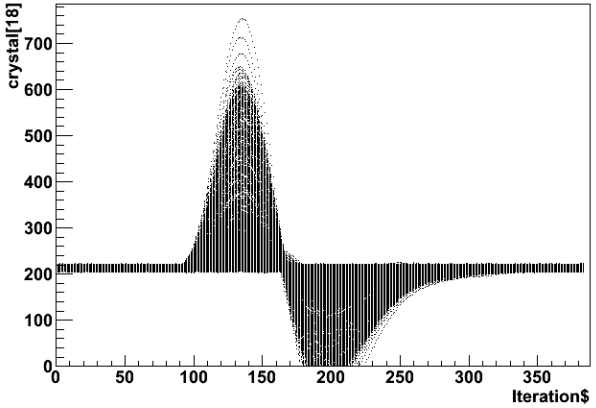


From Test Beam Data



Replicated in LABE

Similarly (7,8), (8,9), (2,3), (3,4),(20,21)



Just a couple of fake cables from VFE to Range shaper

Xtalk Matrix measuraments

(A.Papi L.Recchia)

	2.2%	2.0%	1.7%	1.7%
	2.2%	2.0%	2.0%	2.0%
	1.2%	1.2%	1.1%	1.0%
	0.5%	0.5%	0.5%	0.5%
	2.2%	2.0%	2.4%	1.7%

Ch0

Ch24

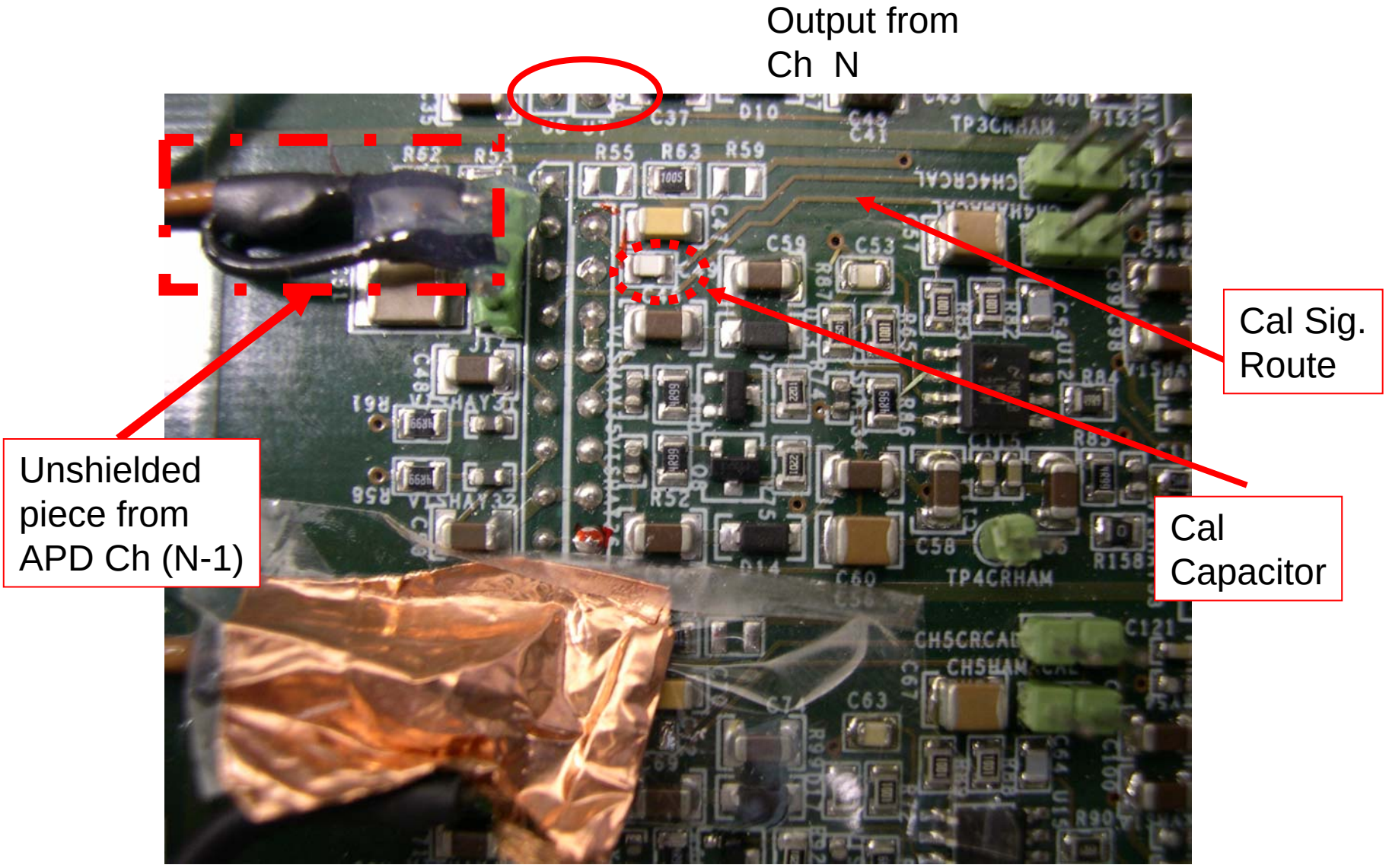
Ch3= Ch3(real) + 2.2% of Ch4

Very Front End Board

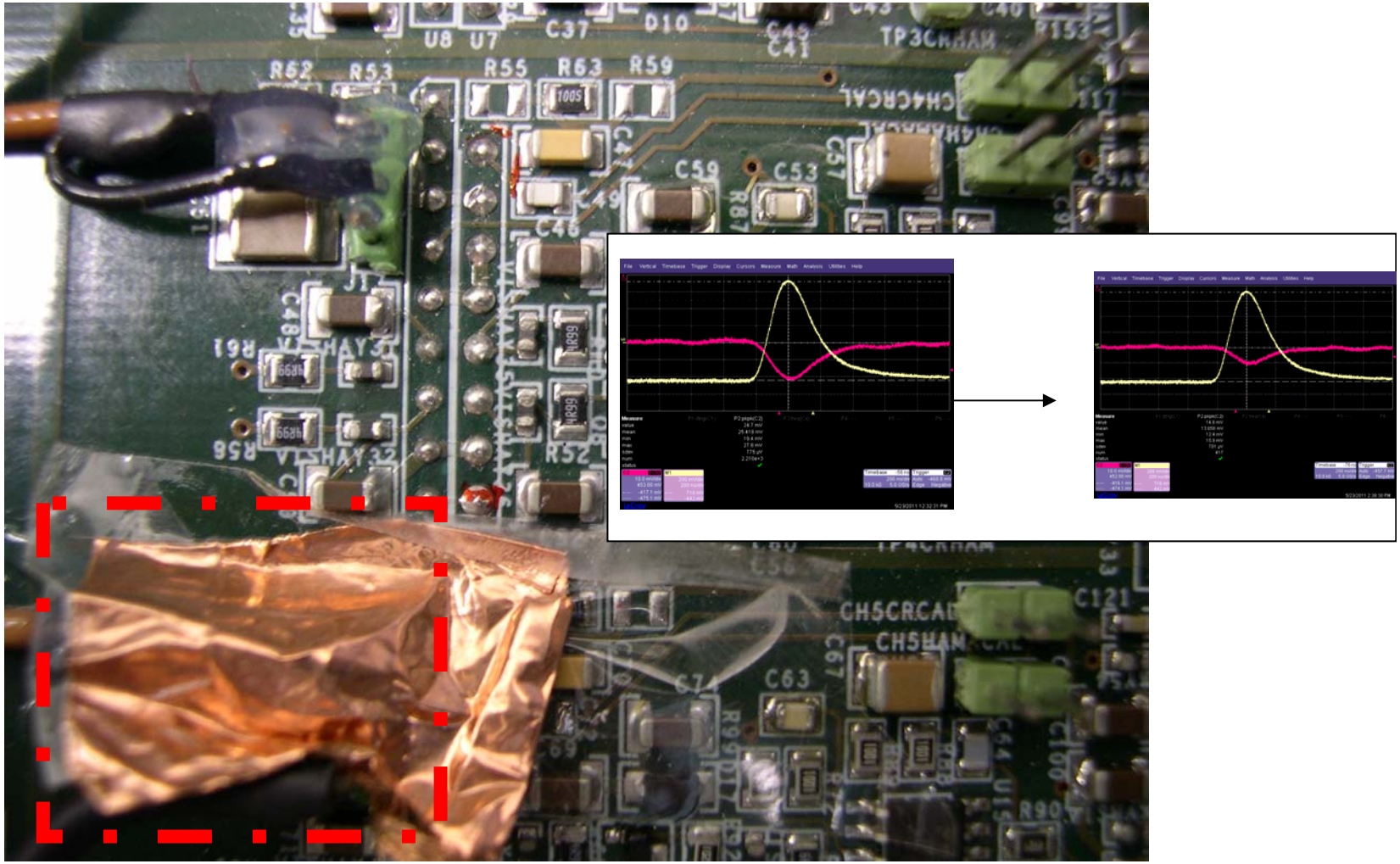
(PCB layout D. Ruggieri, A.Papi)

- EMC VFE Board
- 4 Layers
- 5 CSP Channels
- Enable to mount:
  Cremat,Hamamatsu,Home Made CSP
- HV distribution
- Mounted on crystals
- Interface with EMC range Board

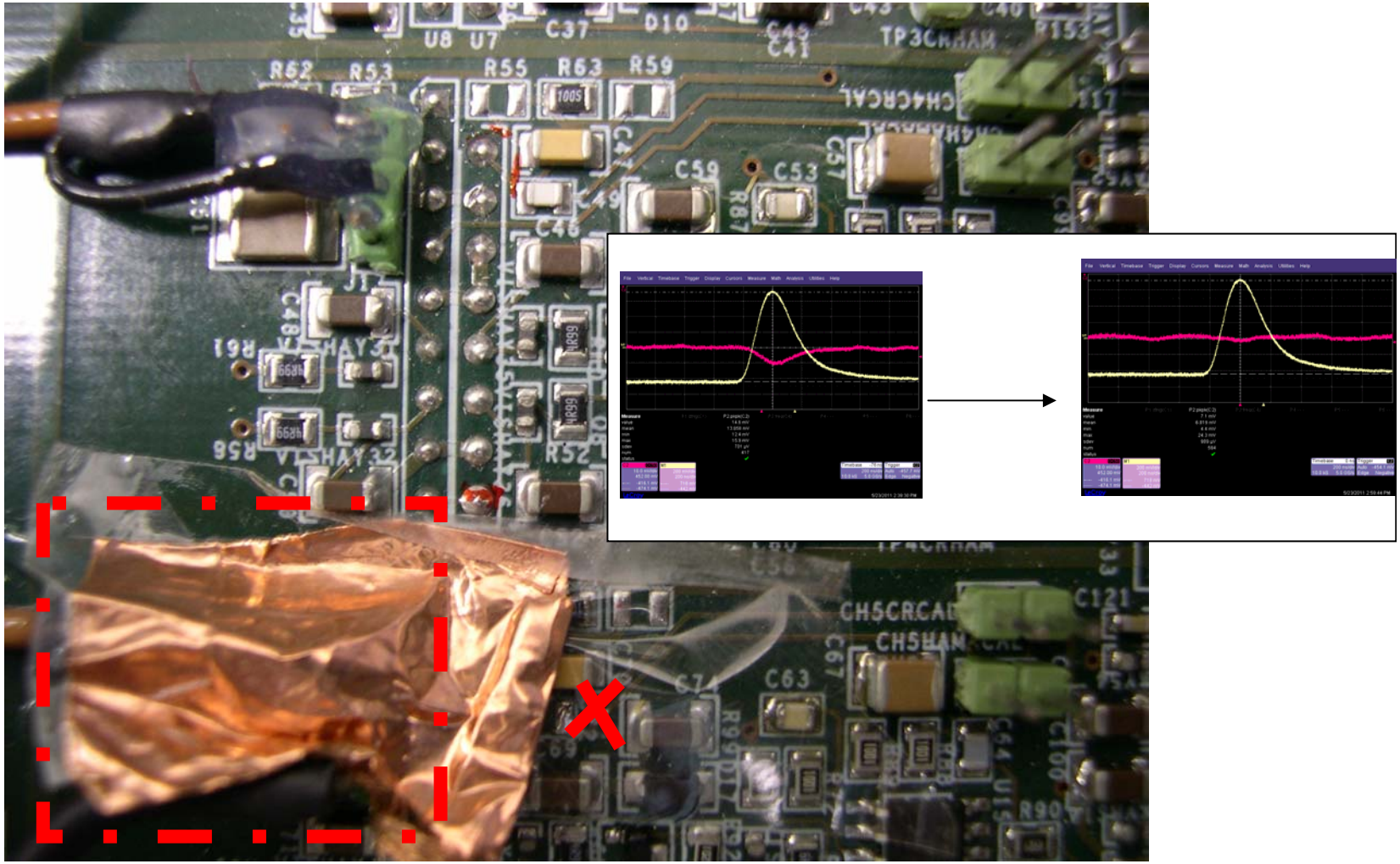
VFE Board Xtalk Source and target



VFE Board Xtalk Source and target

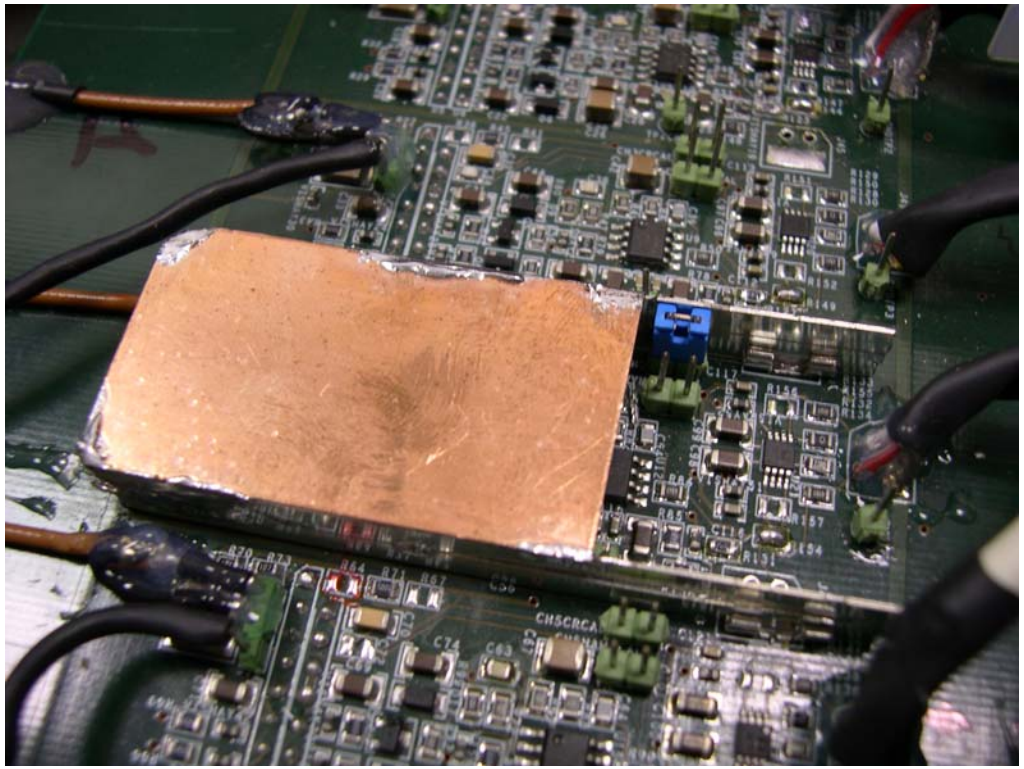


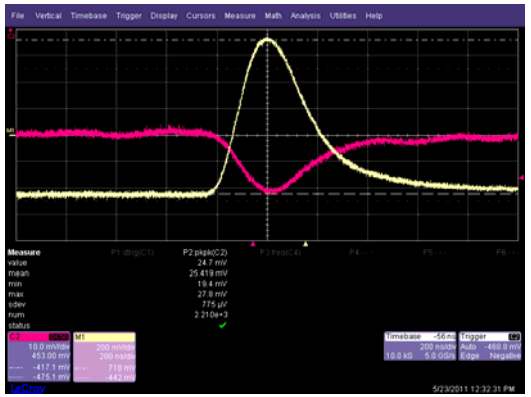
VFE Board Xtalk Source and target

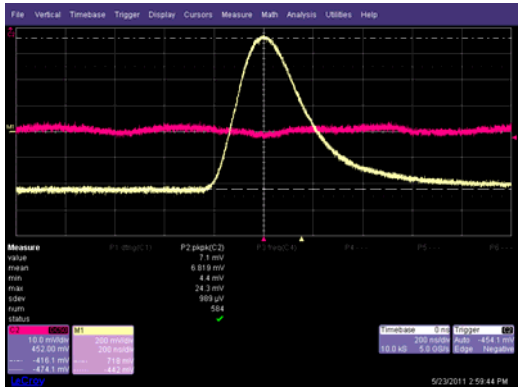


Final Xtalk solution

(by Luigi Recchia)







Preliminary ruffle estimation of FE Power

- 0.5 W/Ch CSP
- 1 W/ch Shaping switching
- <1 W/ch Adc including buffers and logic
- Tot 2 W/Ch
- ruffle FE forward Barrel + Forward → 20 Kwatt

Digital part of the Front End

- We are interested to explore the possibility to use Xilinx FPGA in the Front End
- The use of such flexible device have positive impact of the architecture
- A qualification in short time is necessary
- We have explored and used this approach some years ago:
  Radiation Test and Application of FPGAs in the Atlas Level 1 Trigger,
  V. Bocci at al, 7° Workshop on Electronics for LHC Experiments, Stockholm, Sweden,
  September 2001
  http://cdsweb.cern.ch/record/529388/files/p137.pdf

Conclusions

- We replicate the results from the CERN test beam
- The Better conditions of the Environment permits to discover second order effects not cleary visible during test CERN
- About the architecture and design of digital part of the front end the possibility of use of Xilinx FPGA can have a strong positive impact.