SuperB IFR electronics: status update

Moving from prototype electronics to the final design:

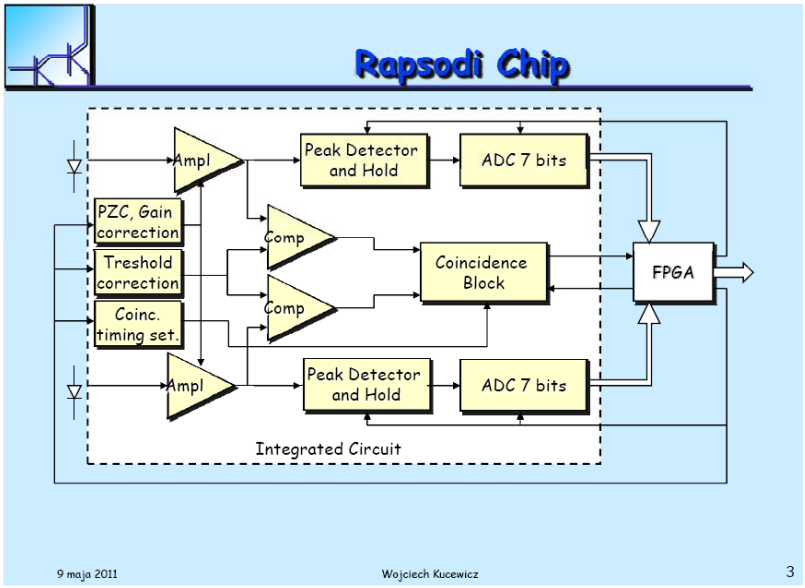
- new SuperB collaborators from the AGH, CUT Universities and the INP PAN Institute in Krakow
- 2010 Fermilab beam test results for the IFR prototype
- from baseline to final design : exploring an all "binary mode" ("BiRO") readout for the IFR
- from baseline to final design: exploiting available SiPM readout ASICs
- from baseline to final design : using FPGAs and design tecniques for radiation mitigation
- conclusions

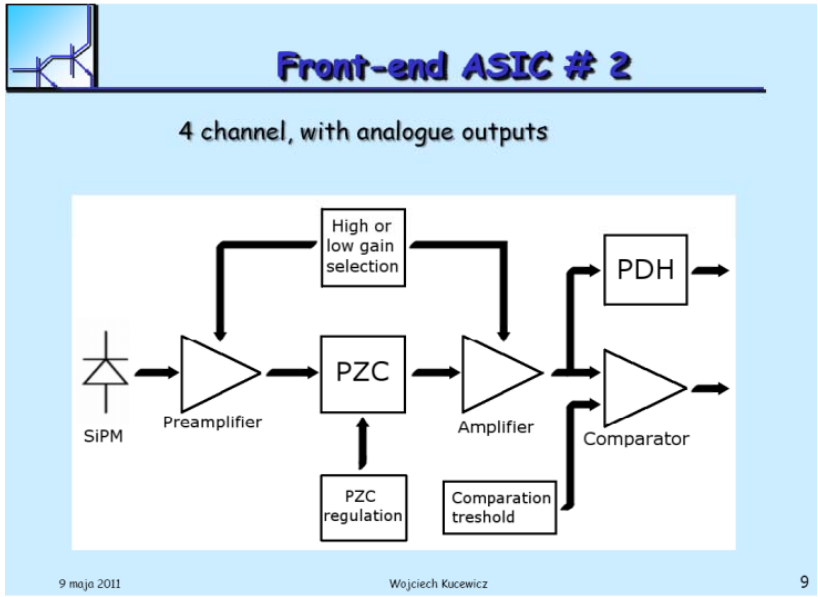
SuperB IFR electronics: new SuperB collaborators from the AGH, CUT and INP PAN Universities in Krakow

Three teams respectively from the:

- AGH University of Science and Technology (AGH), led by Prof. Wojciech Kucewicz (electronic engineering)
- Cracow University of Technology (CUT), led by Prof. Bogdan Szybiński and Prof. Jacek Krużelecki (mechanical engineering)
- Institute of Nuclear Physics Polish Academy of Sciences (INP PAN) led by Prof. Tadeusz Lesiak

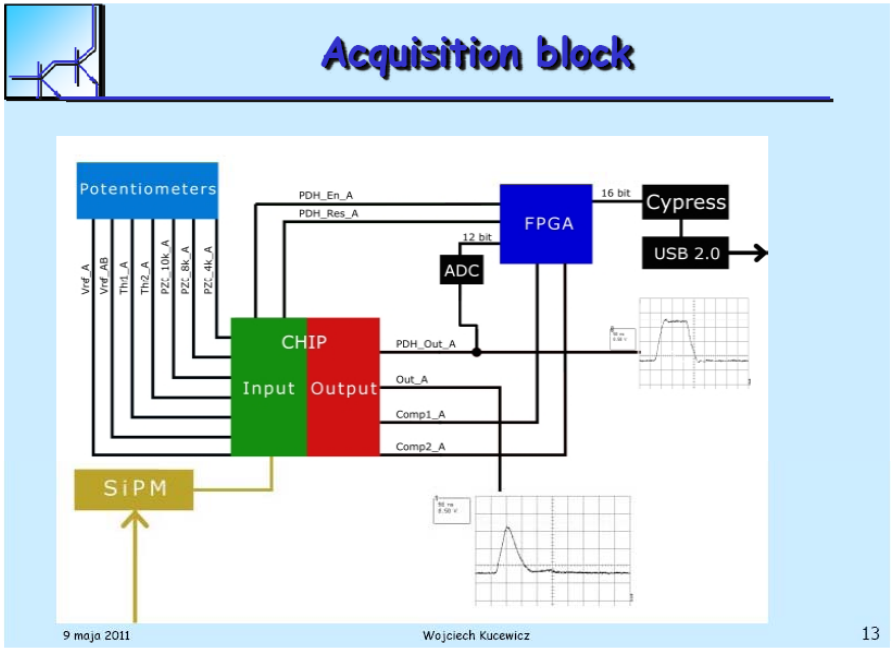
One of the important assets brought by Prof. Kucewicz is his experience with SiPMs and with the design of dedicated ASICs such as the RAPSODY chip and its successor:

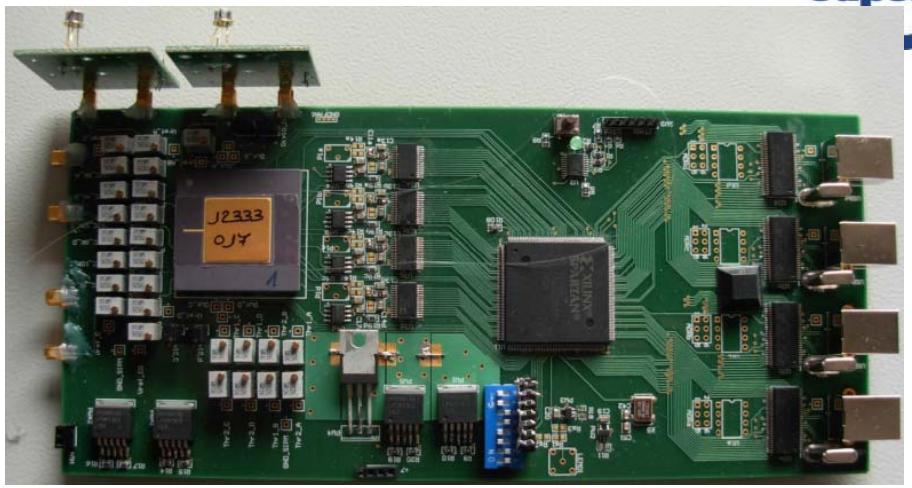




From: "Silicon Photomultiplier Activity at AGH-University of Science and Technology", W. Kucewicz, J. Barszcz, S. Głąb, M. Sapor.

SuperB IFR electronics: new collaborators from AGH University of Science and Technology in Krakow



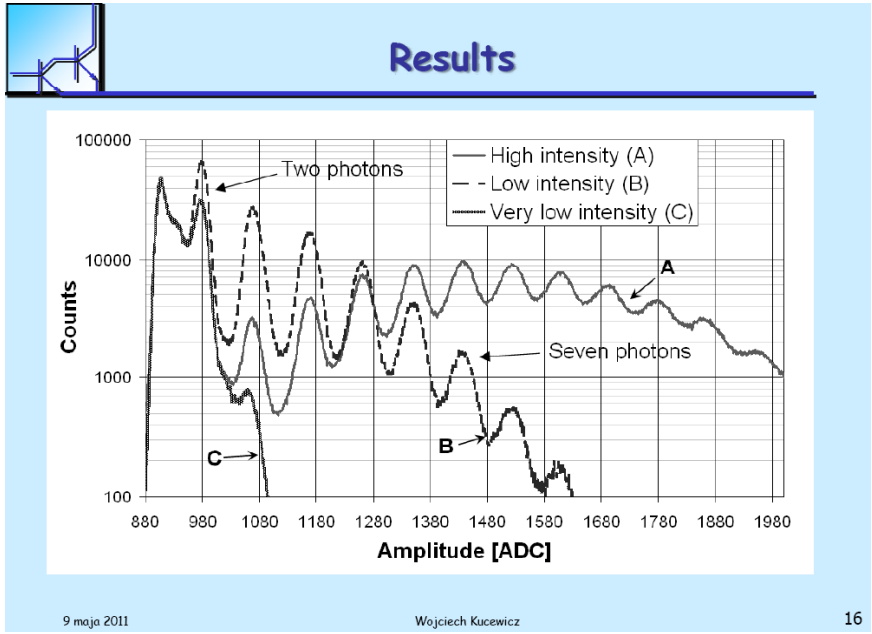


From:

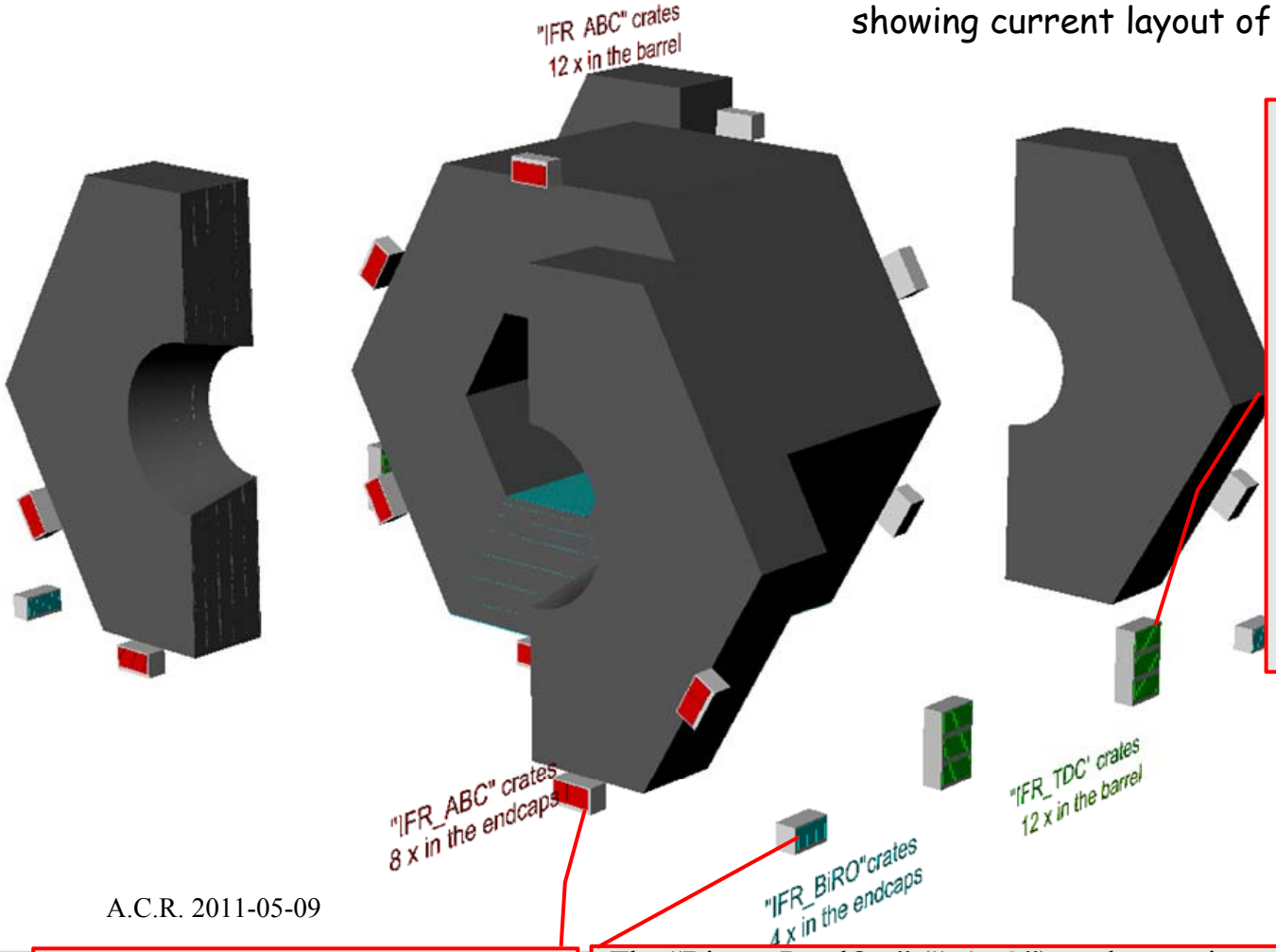
"**Silicon Photomultiplier Activity at AGH-University of Science and Technology**",

W. Kucewicz, J. Barszcz, S. Głąb, M. Sapor.

Prof. Kucewicz will soon connect our FBK SiPMs to his test board for ASIC#2 with the aim of studying the feasibility of a large scale quality control system based on it (in multiple copies)



SuperB IFR electronics : overview - baseline design: IFR front end electronics showing current layout of crates



The "**TDC**" cards contain:
- TDC digitizers (ACAM TDC GPX)
- memories, to buffer timing records for the trigger latency time
- trigger processing unit
- data link drivers

They readout the BARREL channels which produce **TIMING** information

A.C.R. 2011-05-09

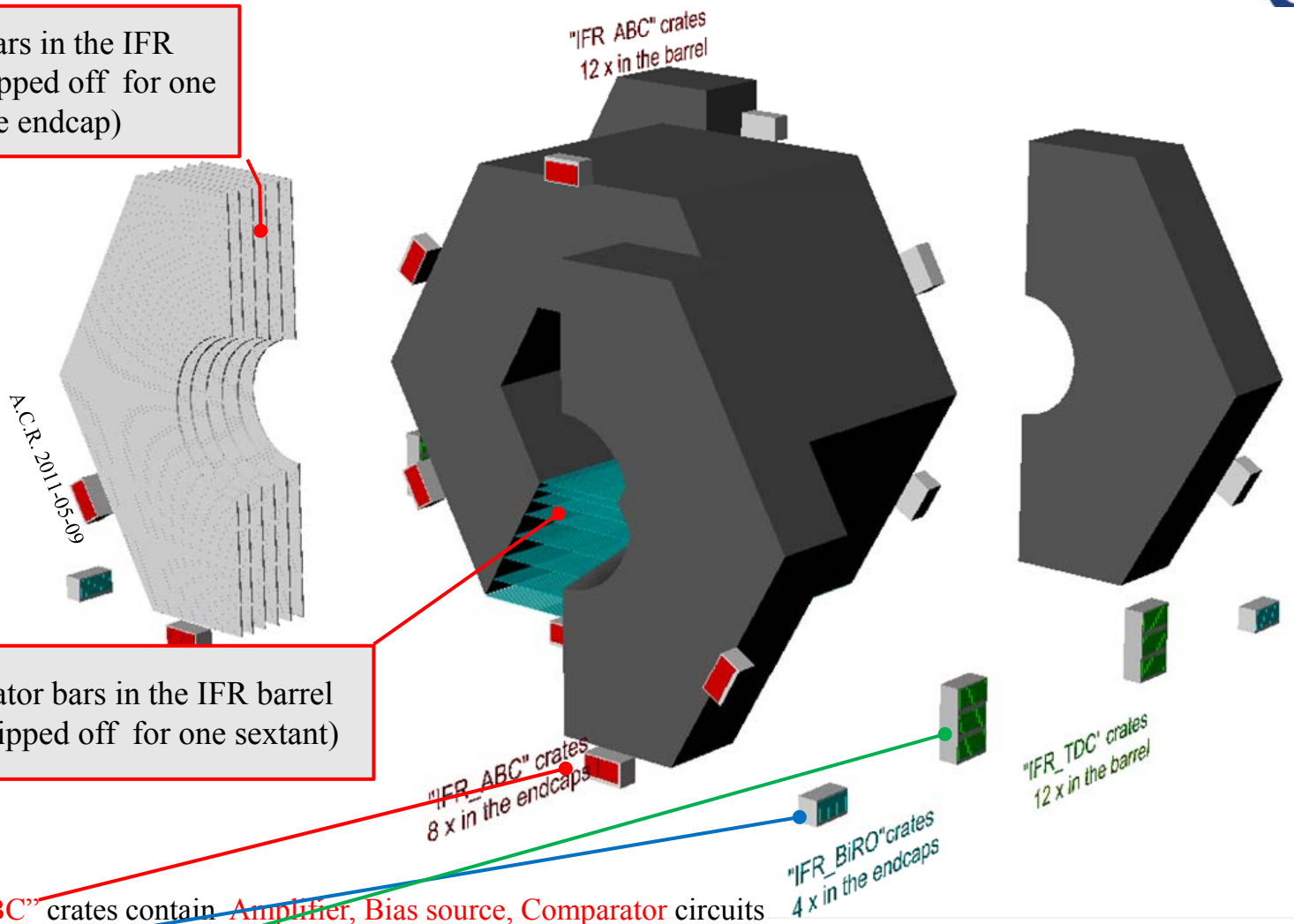
The "ABC" cards contain:
-Amplifier
-Bias circuit
-Comparators

The "Binary ReadOut" ("**BiRO**") cards contain:
- memories, to buffer samples of the comparator output for the trigger latency time
- trigger processing unit
- data link drivers

They readout the ENDCAP channels which produce a simple binary information ("hit" or "not hit")

SuperB IFR electronics: 2010 Fermilab beam test results for the IFR prototype – a reminder

Scintillator bars in the IFR endcap (iron stripped off for one half of the endcap)



Scintillator bars in the IFR barrel (iron stripped off for one sextant)

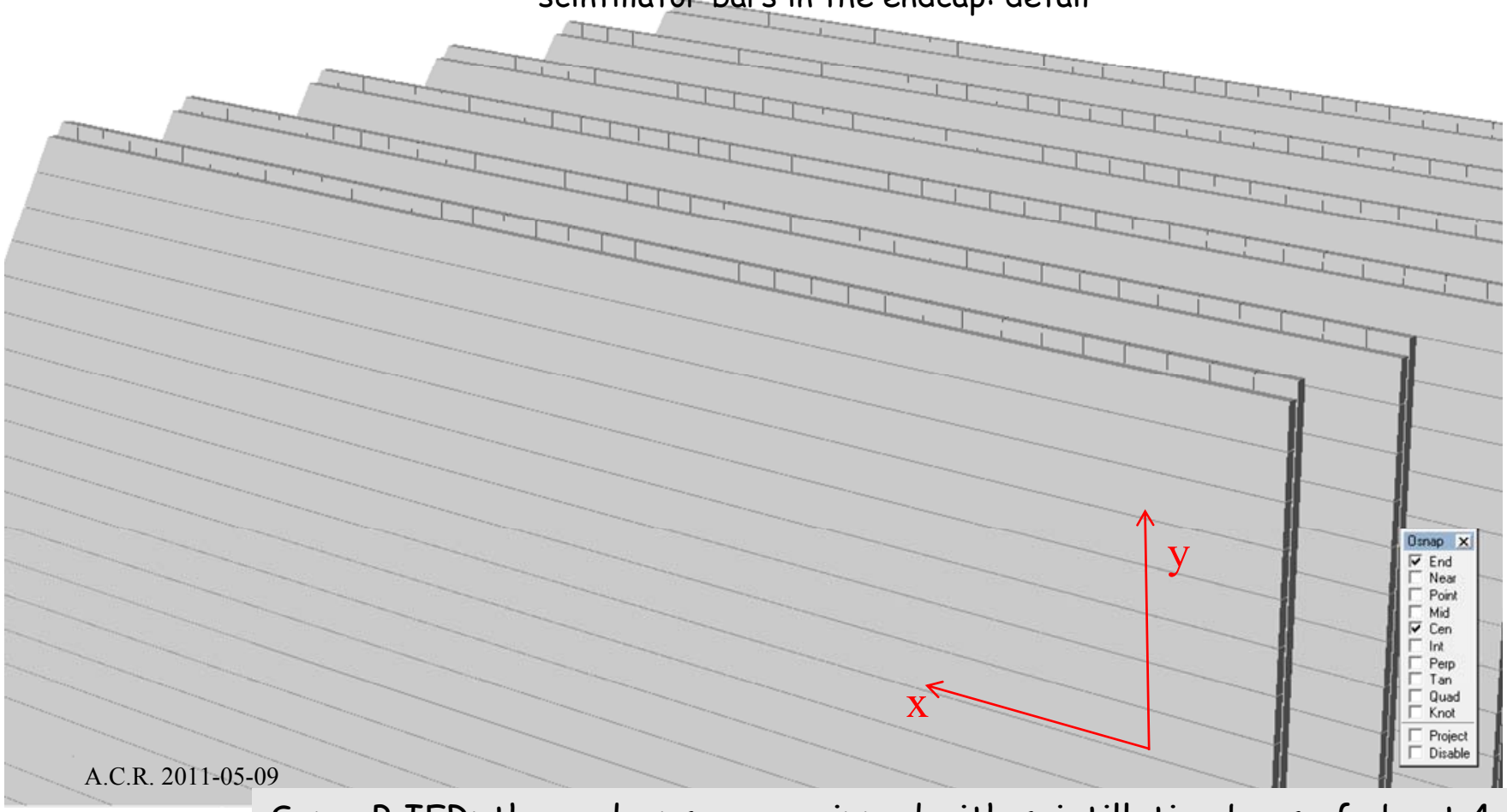
Legenda:

- "IFR_ABC" crates contain Amplifier, Bias source, Comparator circuits
- "IFR_BiRO" crates contain sampling circuits and buffer memories to Read Out the IFR_ABC cards in Binary mode
- "IFR_TDC" crates contain TDC circuits and buffer memories to readout the IFR_ABC cards in timing mode

In the baseline design the splitting of functions was meant to allow the digitizers and latency buffers to be positioned as far as possible away from the high radiation region of the detector and surroundings.

SuperB IFR electronics: 2010 Fermilab beam test results for the IFR prototype – a reminder

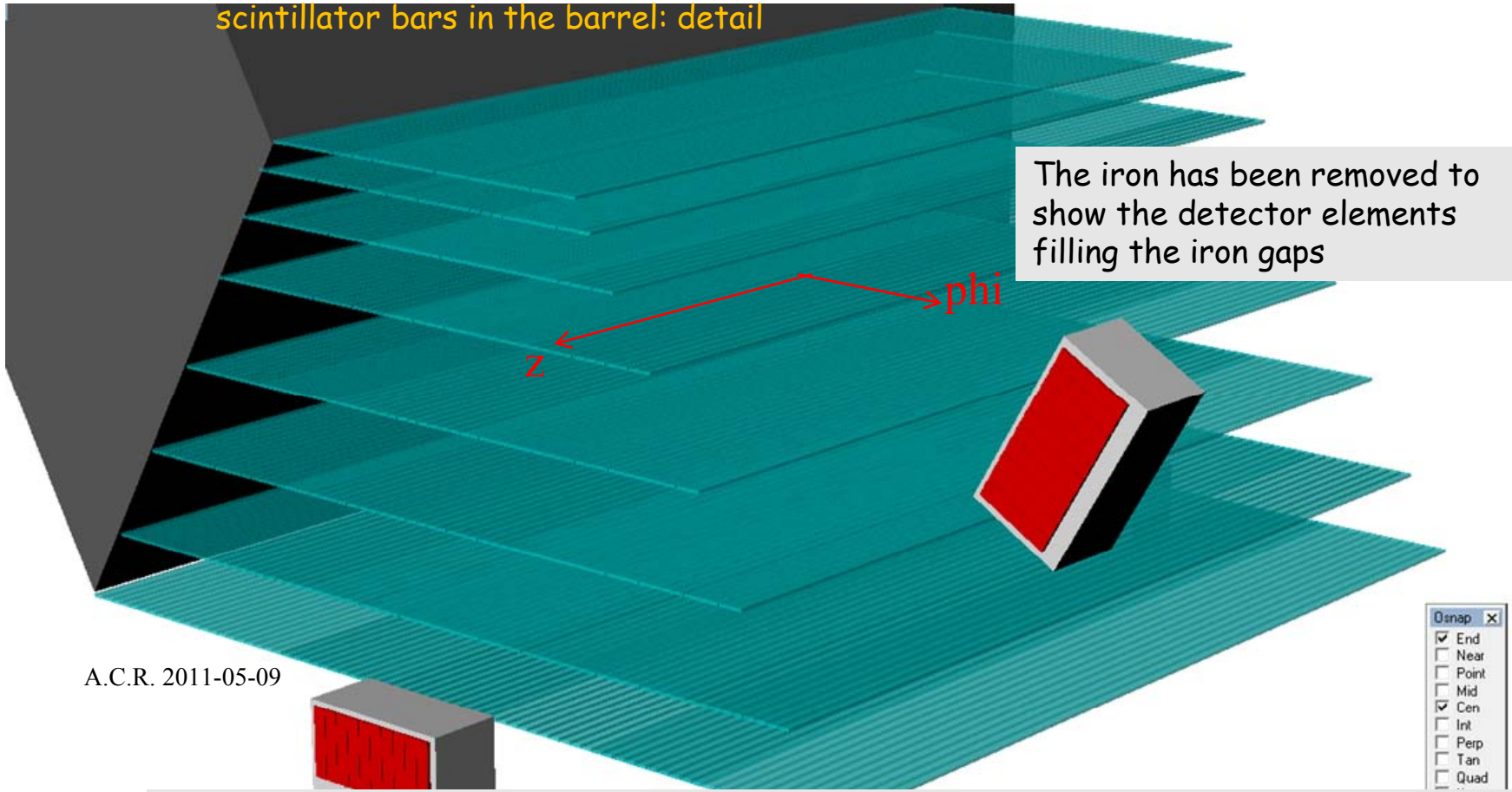
scintillator bars in the endcap: detail



SuperB IFR: the endcaps are equipped with scintillating bars of about 4x1 cm^2 cross section which are assembled orthogonally and inserted in the iron gaps. Each bar is READ OUT BY SiPM AT ONLY ONE END.
The "hit" coordinates are found by simply recording the IDs of the two orthogonal bars producing a signal (the off line reconstruction will resolve ambiguities due to high multiplicity)

SuperB IFR electronics: 2010 Fermilab beam test results for the IFR prototype – a reminder

scintillator bars in the barrel: detail

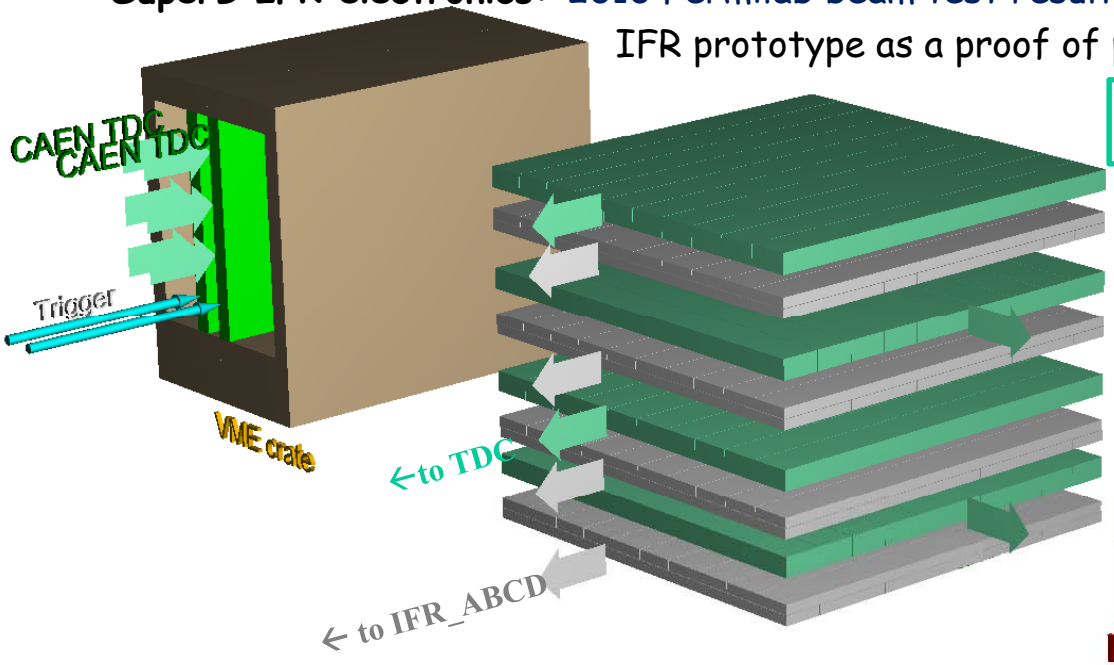


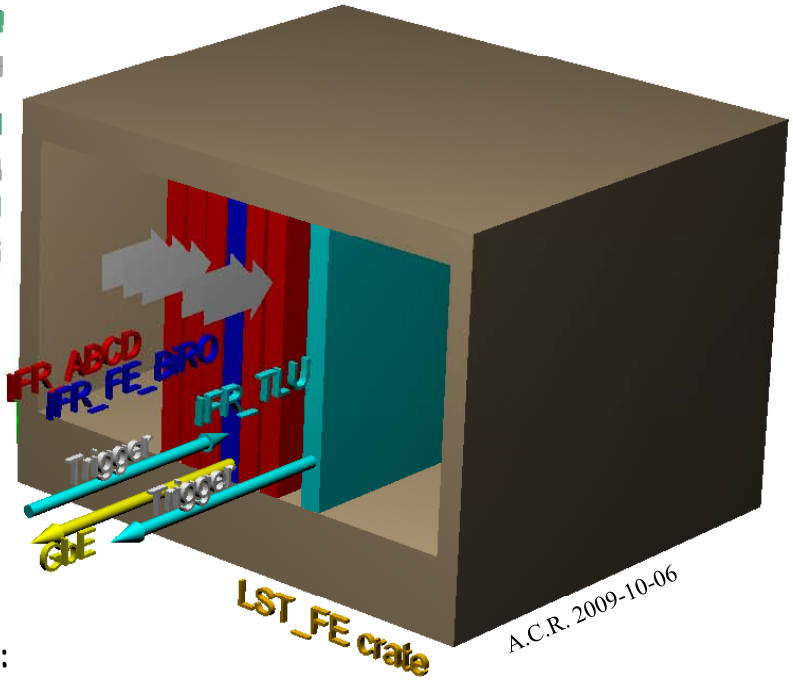
SuperB IFR (baseline design): in the barrel the scintillator bars are 4x2cm^2 in cross section and are only oriented in the Z direction. Each bar is READ OUT BY SiPM **AT BOTH ENDs**. The "hit" coordinates are found:
-in the PHI direction: by simply recording the ID of the scintillator bar producing a signal
-in the Z direction: by recording the times of arrival of the signals from the SiPM at each end of the detector bar. **The Z coordinate can then be determined off-line once the time zero of the event is known**

SuperB IFR electronics: 2010 Fermilab beam test results for the IFR prototype – a reminder

IFR prototype as a proof of principle

the concept....





SuperB IFR prototype:
- 4 layers of x-y scintillators, 1 cm thick, read in binary mode
- 4 layers of scintillators 2 cm thick, read in timing mode

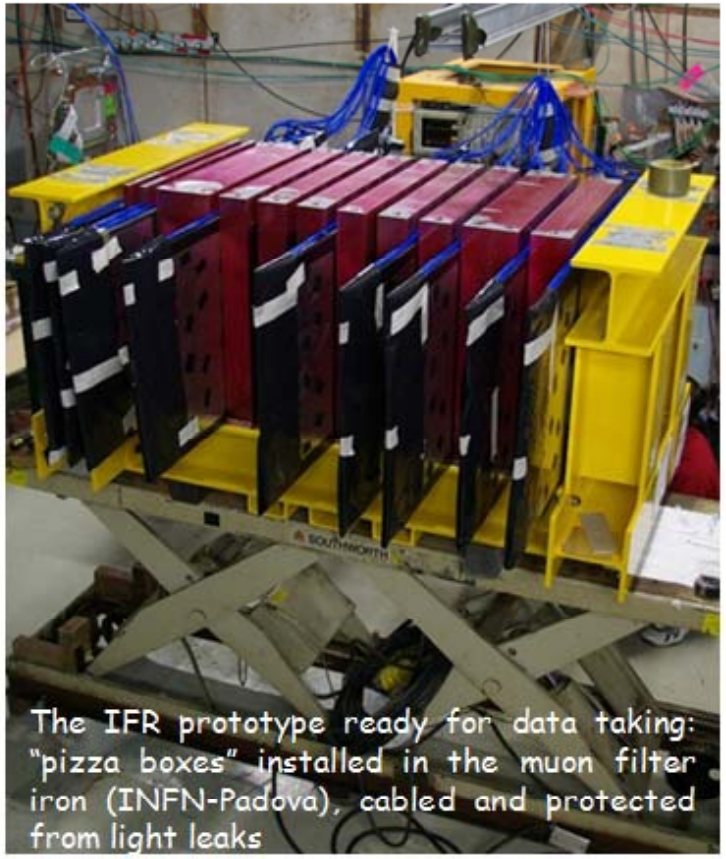
SuperB-IFR prototype readout electronics (baseline):
- "IFR_ABCD": sensor Amplification, Bias-conditioning, Comparators, Data processing: it samples the level of the comparators outputs @ >= 80MHz and stores it, pending the trigger request
- "CAEN_TDC": a multi-hit TDC design based on CERN HP-TDC; hosted in a VME crate and read out via a VME CPU or via a VME-PCI bridge to the DAQ PC
- "IFR_FE_BiRO": collects data from IFR_ABCD cards upon trigger request and sends it to DAQ PC (via GbE)
- "IFR_TLU": a module (Trigger Logic Unit) to generate a fixed latency trigger based on primitives from the IFR prototype itself or from external sources

IFR_FE_BiRO + IFR_TLU are now a single module

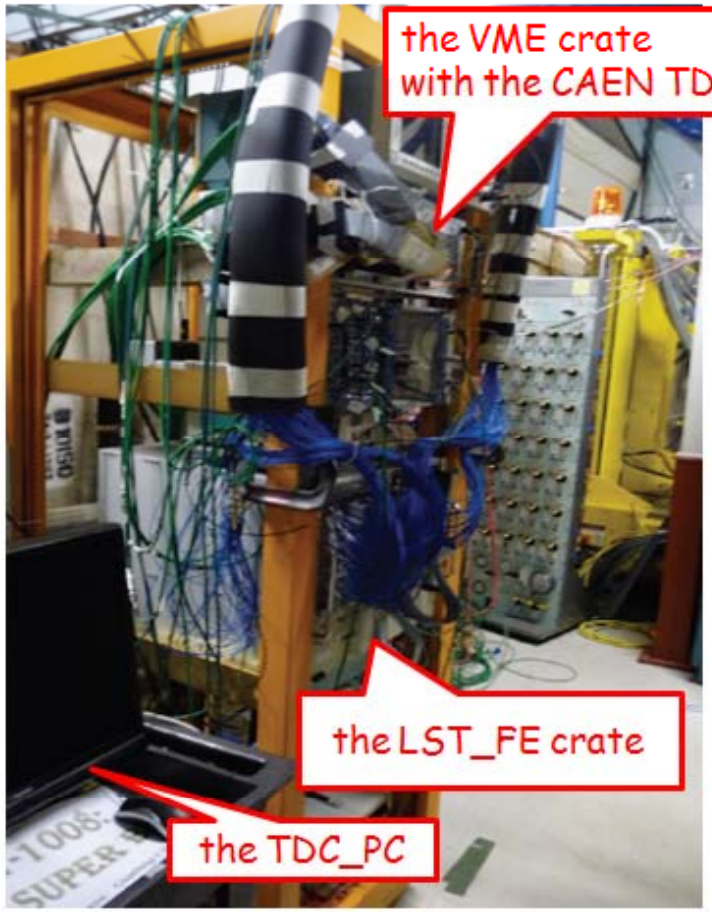
SuperB IFR electronics : Beam test of the IFR prototype electronics and DAQ system

...and the real thing!

pictures from G. Cibinetto, "Some note on the beam test" presented at this meeting

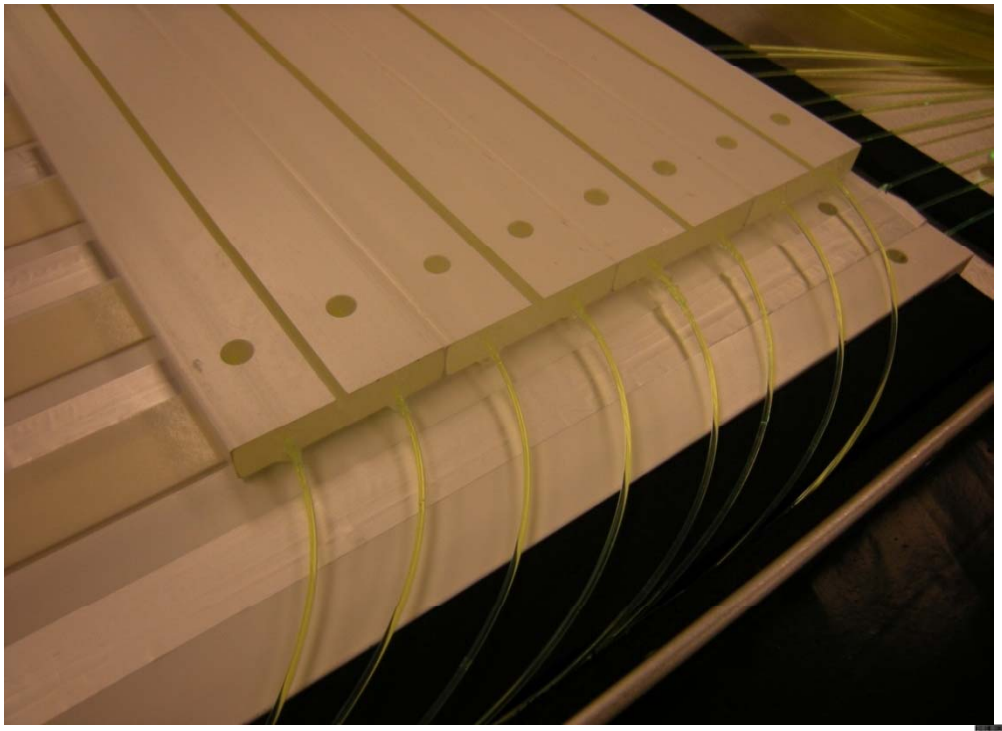


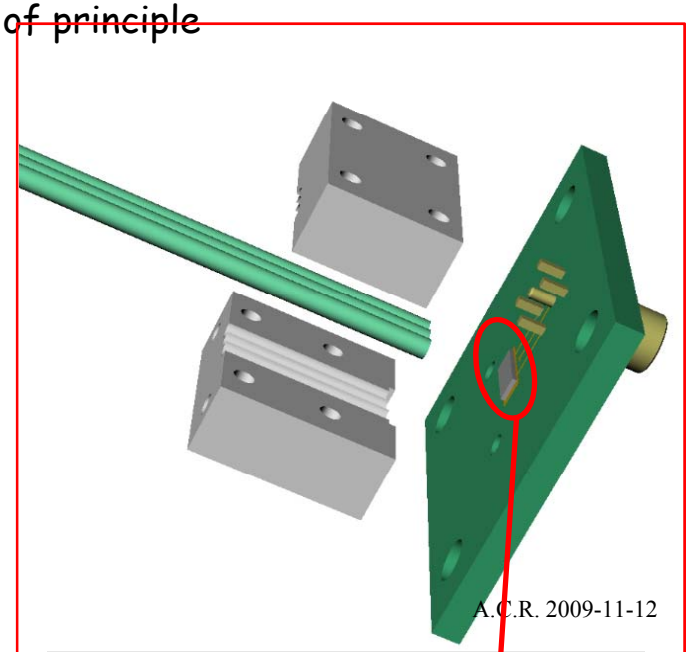
The IFR prototype ready for data taking: "pizza boxes" installed in the muon filter iron (INFN-Padova), cabled and protected from light leaks



SuperB IFR electronics: 2010 Fermilab beam test results for the IFR prototype – a reminder

IFR prototype as a proof of principle

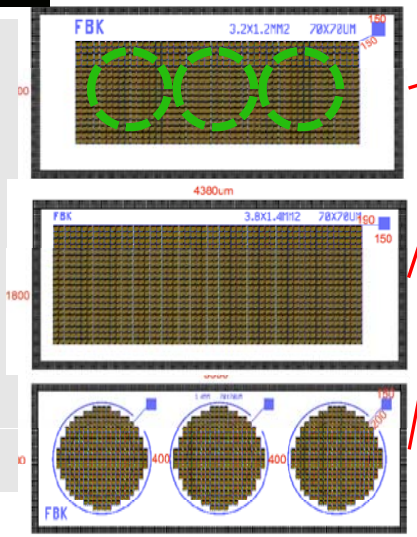




pictures/drawing from the prototype construction

SuperB IFR : the scintillating bars are equipped with wavelength shifting fibers (3 for each bar in the prototype), which are then coupled to a SiPM device by means of precisely machined plastic supports.

The prototype had BOTH:
-planes with 1cm thick scintillators mounted in 2 orthogonal layers
- planes with 2cm thick bars mounted in only one direction, for the TDC readout

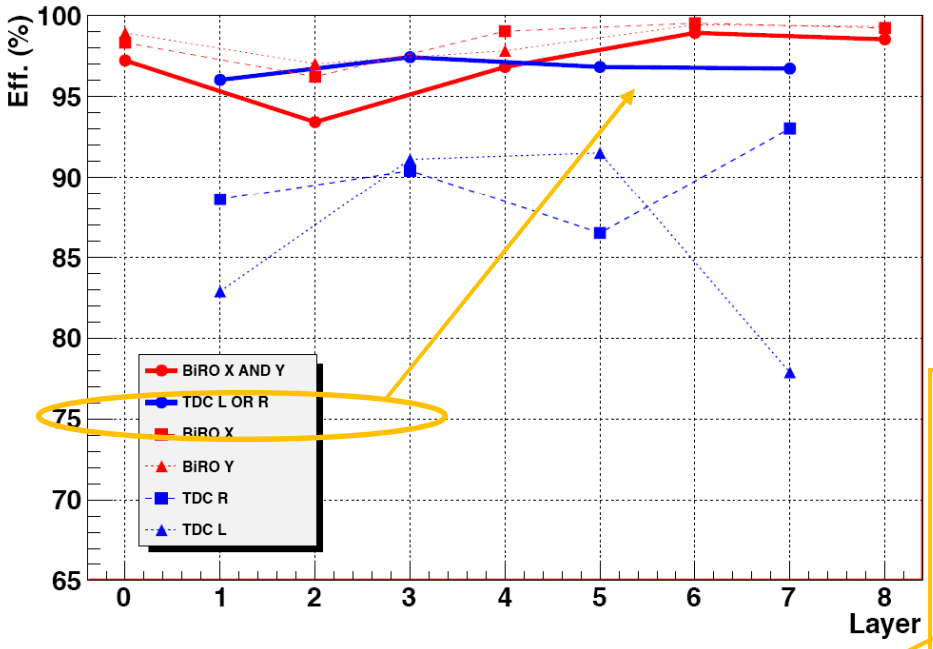


SiPM by FBK, Trento. 70x70um^2 cell size, n-on-p.

Bonding of the SiPM to the carrier PCB was performed at INFN Perugia thanks to G. Ambrosi, M. Ionica

SuperB IFR electronics : overview - IFR prototype as a proof of principle

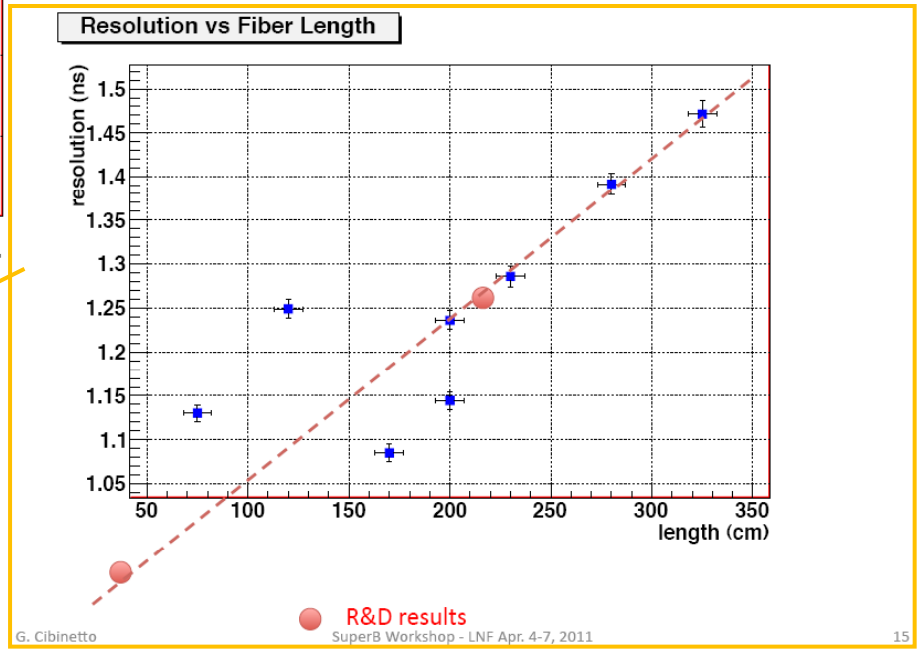
from "Prototype data analysis" by G. Cibinetto, presented at the XVI SuperB workshop in LNF



G. Cibinetto SuperB Workshop - LNF Apr. 4-7, 2011

The DAQ system performed well and the data recorded has been analyzed by a team of physicists from INFN-Ferrara and INFN-Padova. I extract a couple of slides from their presentations

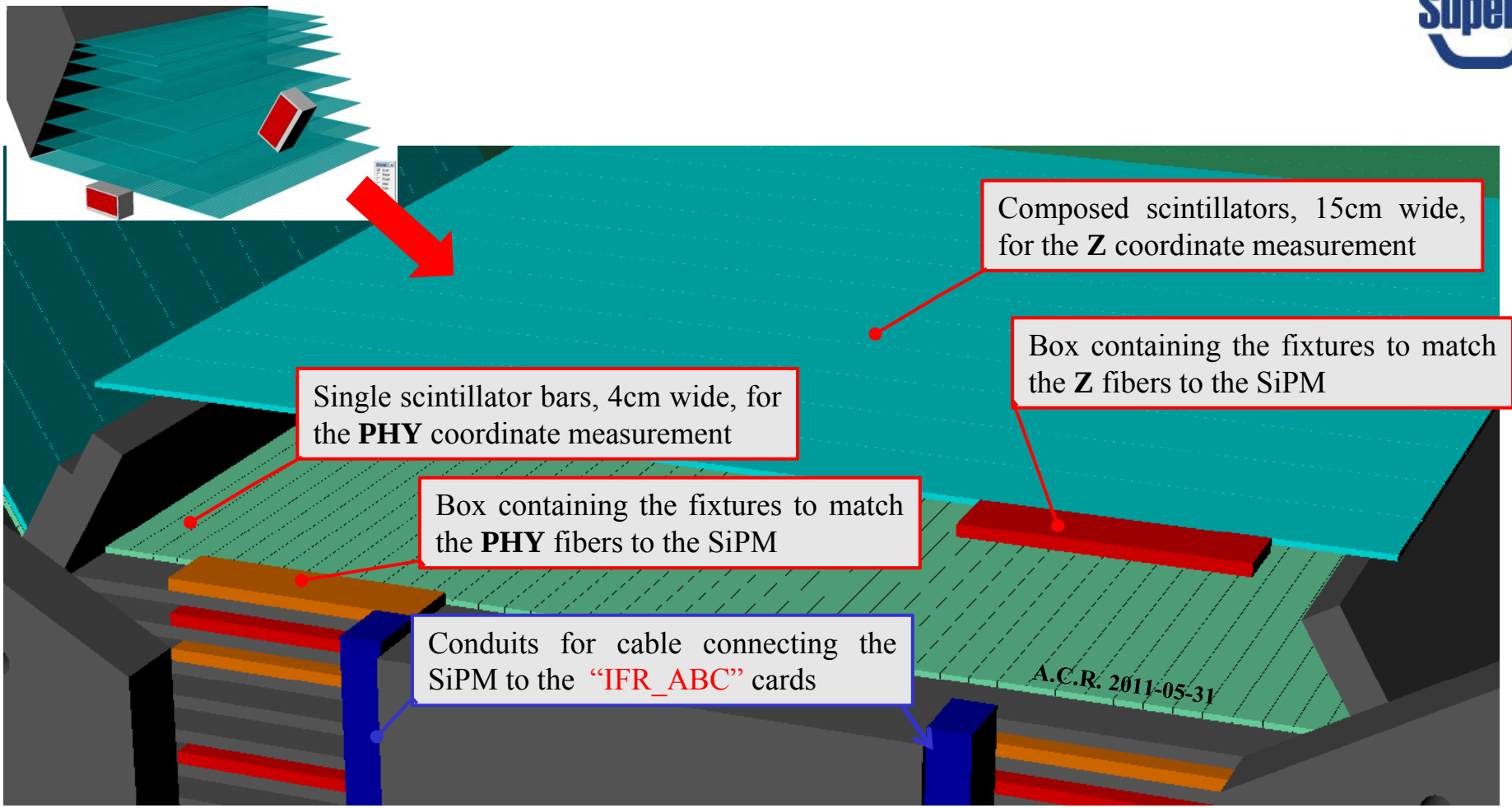
Z position resolution ≈ 25cm



The position resolution is within specification but
there are concerns that it would degrade with radiation damage of SiPMs and high track multiplicity

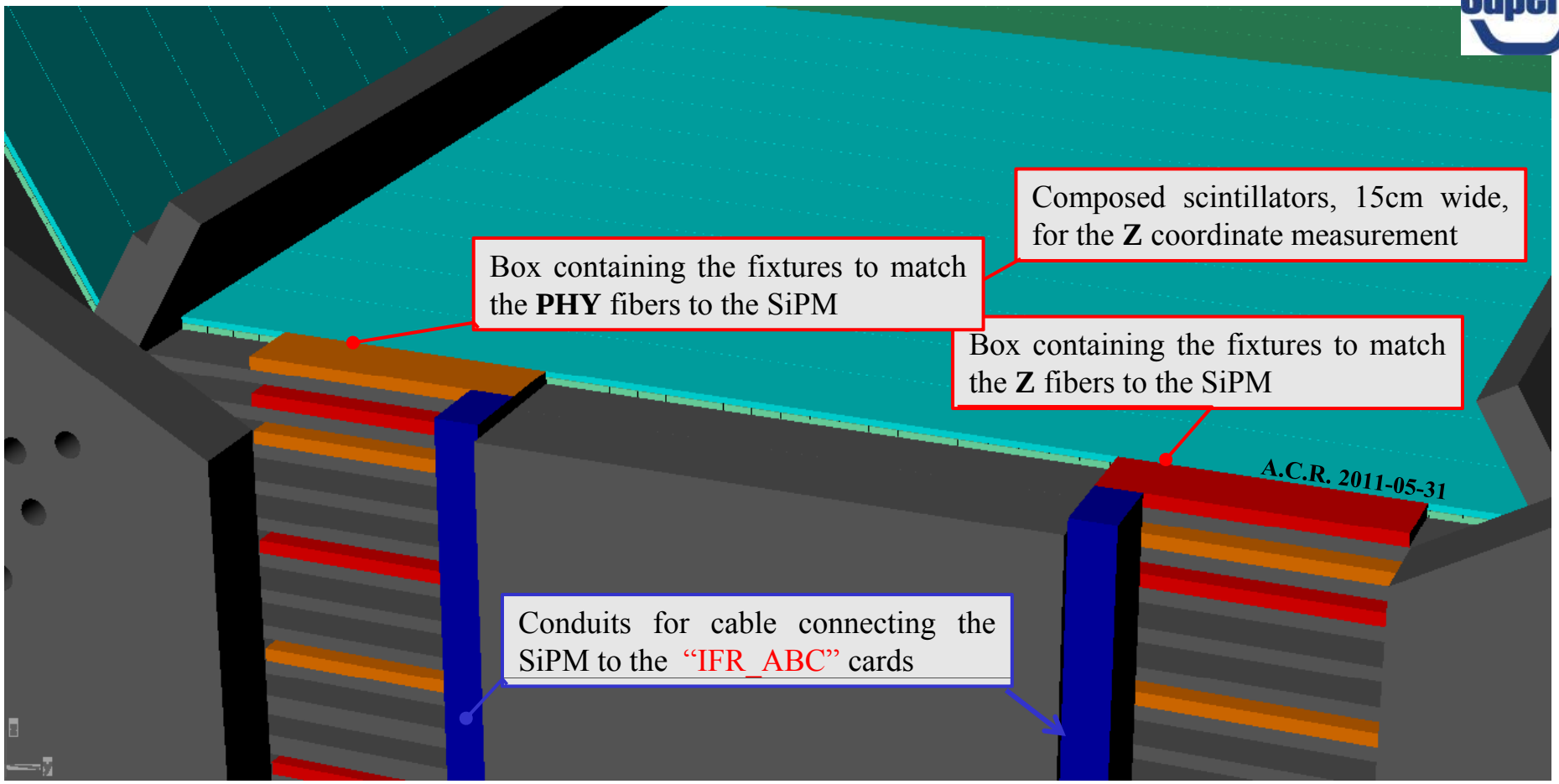
→

SuperB IFR electronics: exploring an all "binary mode" ("BiRO") readout for the IFR



Note: the Z and the PHY layers have been separated in this picture to show them distinct

SuperB IFR electronics: exploring an all "binary mode" ("BiRO") readout for the IFR



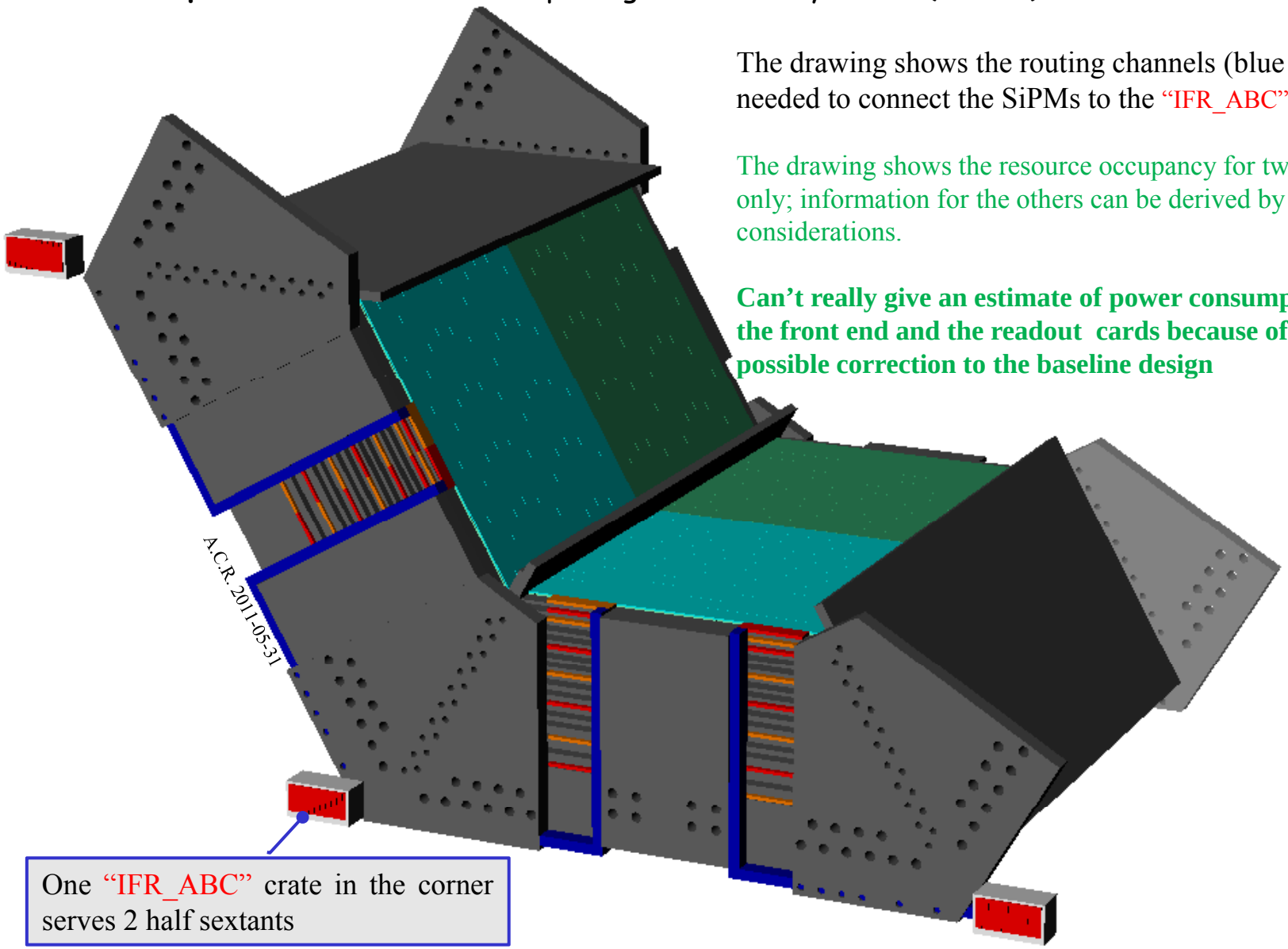
Note: the Z and the PHY layers are shown here with no separation.
The location of the boxes alternate at different layers because behind the boxes there are regions (not shown) of the scintillators dedicated to WLS fiber routing, which are regions of degraded efficiency.
By staggering the boxes, the lower efficiency regions don't line up and the efficiency loss is mitigated

SuperB IFR electronics: exploring an all "binary mode" ("BiRO") readout for the IFR

The drawing shows the routing channels (blue conduits) needed to connect the SiPMs to the "IFR_ABC" crates.

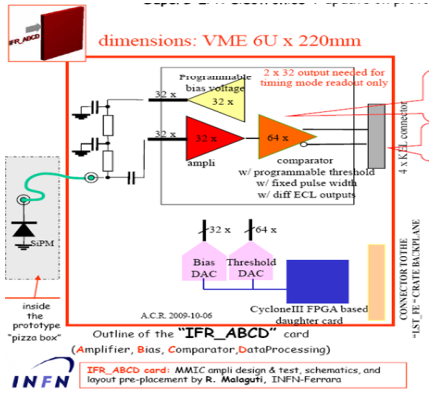
The drawing shows the resource occupancy for two sextants only; information for the others can be derived by simmetry considerations.

Can't really give an estimate of power consumption for the front end and the readout cards because of the possible correction to the baseline design



One "IFR_ABC" crate in the corner serves 2 half sextants

SuperB IFR electronics : from baseline to final design: exploiting available SiPM readout ASICs



The "IFR_ABCD" has proven to be a flexible and reliable design, easy to adapt to "p-on-n" as well as "n-on-p" SiPM devices. Its on board microcontroller allows for stand –alone operation and its amplifier monitoring outputs make the "IFR_ABCD" a good SiPM characterization tool.

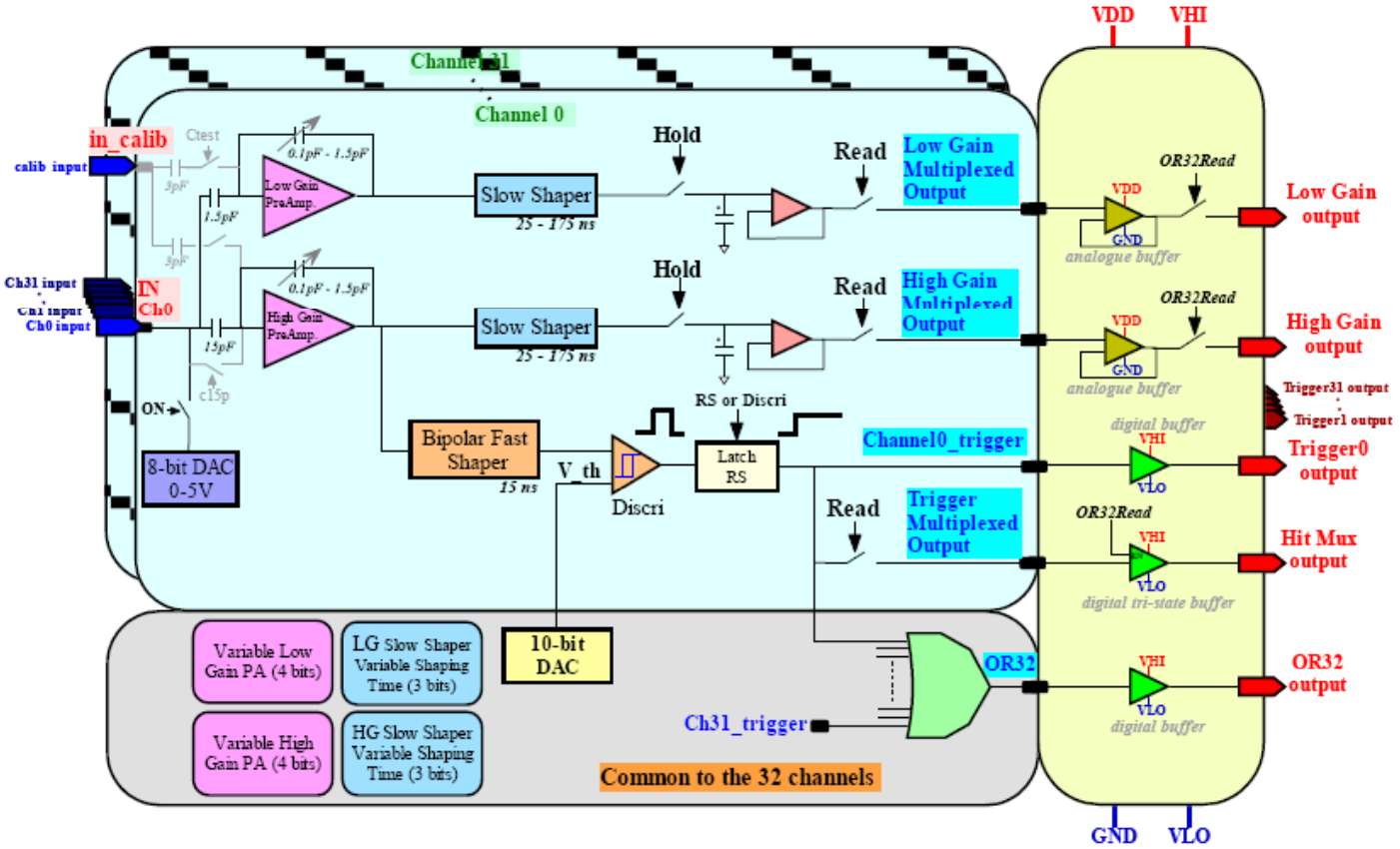
NEVERTHELESS WHEN PLANNING THE READOUT OF > 20.000 CHANNELS it is good to look for ASICs solutions, starting from existing ones. A good occasion was the:

Infact the present state of the art was very effectively described in:

"Review of ASIC developments for SiPM signal readout",
Wojtek Kucewicz, AGH- University of Science and Technology Krakow.

SuperB IFR electronics : from baseline to final design: exploiting available SiPM readout ASICs

One of the ASICs presented at the SiPM event was the "EASIROC" by the OMEGA group of LAL in Orsay.



It has an individual trigger output for each of 32 channels plus 32 individual bias setting DACs and a common threshold setting DAC.

!!! CAVEAT: the EASIROC was not designed to operate in a high radiation area

USER GUIDE Omega

EASIROC

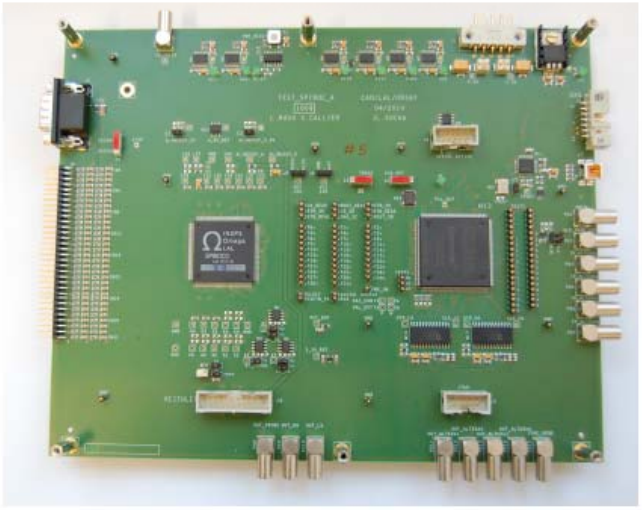
SOFTWARE & TEST BOARD USER GUIDE

Version: 11 April 2011

Abstract

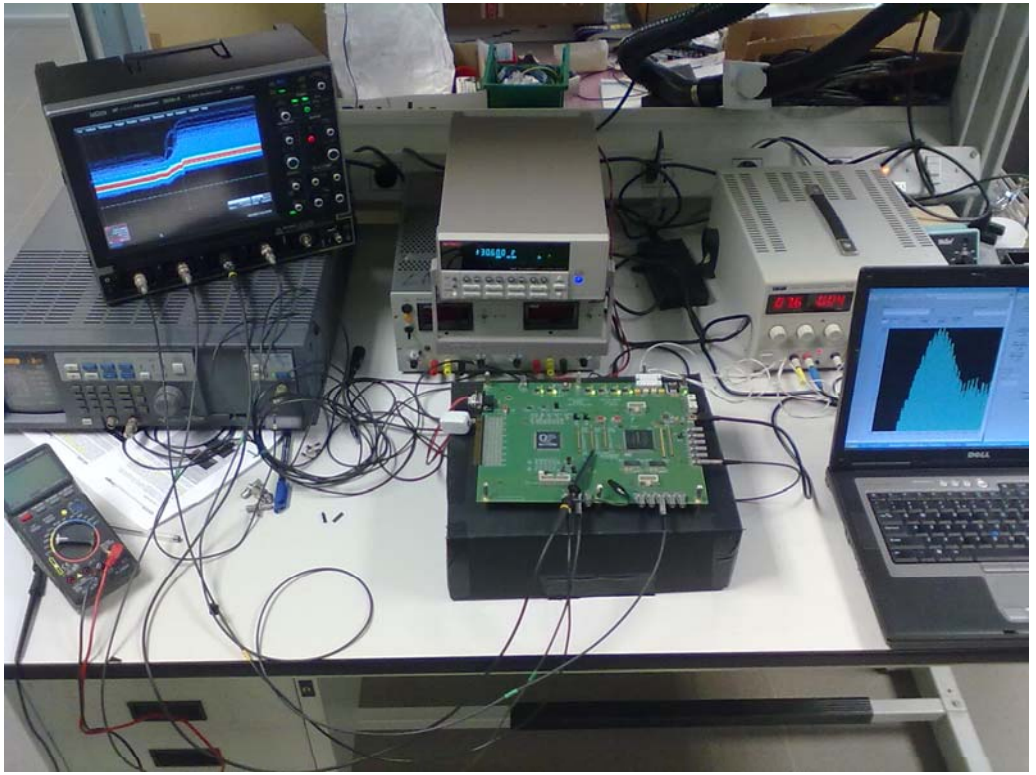
EASIROC (previously SPIROC0), standing for *Extended Analogue Silicon pm Integrated Read Out Chip*, is a 32-channel fully-analogue front end ASIC dedicated to the gain trimming and read-out of SiPM detectors.

This guide explains how to install & use the test board for EASIROC and how to operate with the associated software.

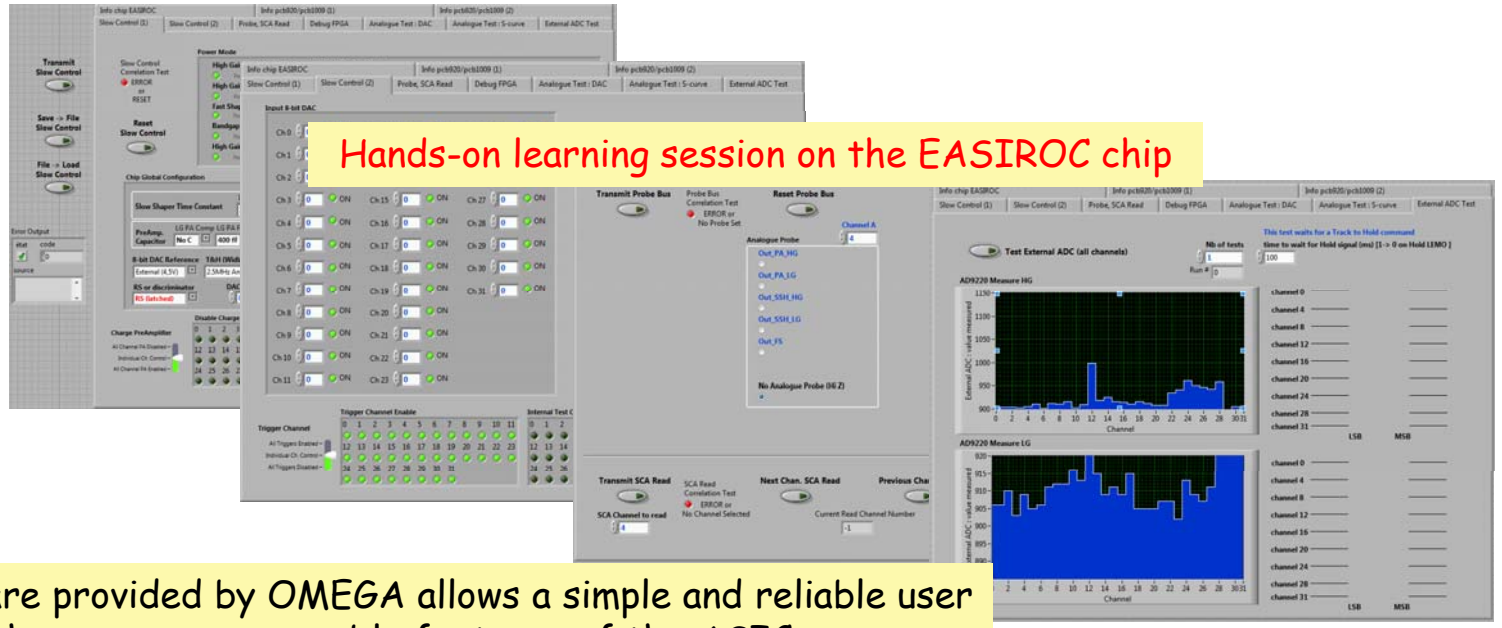


Orsay MicroElectronics Group Associated

Gisèle MARTIN-CHASSARD and Stephane CALLIER of OMEGA have provided us not only plenty of information but a complete hardware and software test system, which we have been using in Ferrara since a couple of weeks to learn "hands-on"



SuperB IFR electronics : from baseline to final design: exploiting available SiPM readout ASICs



Hands-on learning session on the EASIROC chip

The software provided by OMEGA allows a simple and reliable user control of the many programmable features of the ASIC.

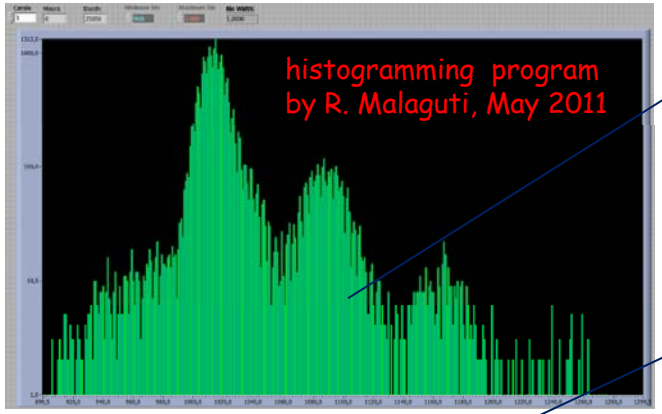
Step 1:
- Setup the EASIROC chip and look at signals

analog output monitored after the Sample and Hold
(with hold signal generated inside the on-board FPGA
after a slight modification by Roberto Malaguti, INFN-FE)

active low HOLD_n signal

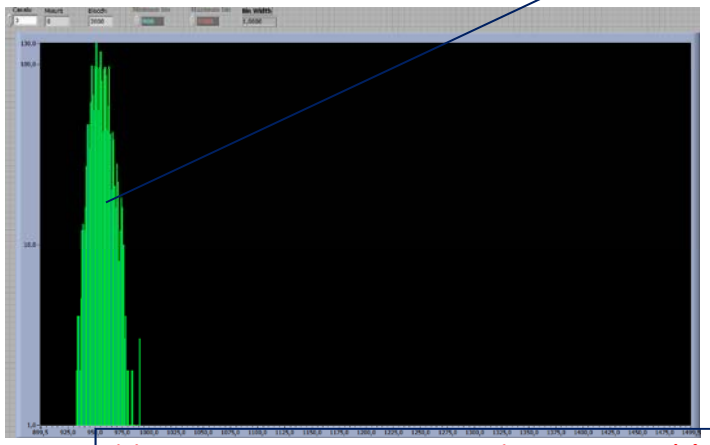
Trigger output associated to the tested channel.
The jitter we measured with respect to the light pulse shone on the SiPM was too high for the EASIROC to be used for TDC timing mode readout **but the trigger outputs are perfectly good for Binary Reaadout mode of the SiPM of the IFR**

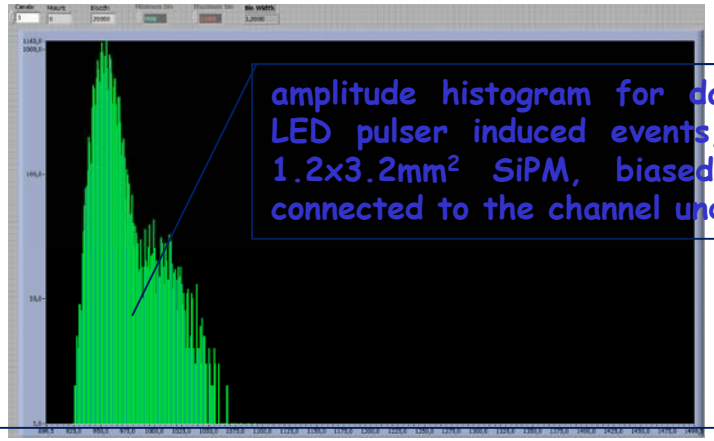
Step 2:
- use the 12bit ADCs of the test board to collect spectra of signals from the active device connected to the input



dark current amplitude histogram for an Hamamatsu 1x1mm^2 MPPC, biased at 69.84V, connected to the input under test

dark current amplitude histogram for an FBK 1.2x3.2mm^2 SiPM (biased at 30.90V to achieve a dark count rate of about 250KHz), connected to the channel under test





amplitude histogram for dark current + LED pulser induced events, for an FBK 1.2x3.2mm^2 SiPM, biased at 30.90V, connected to the channel under test

Note: our setup uses a 1m coax cable to connect the SiPM carrier PCB to the ORSAY test board. This and, possibly, the fact that the substrate of the SiPM (n-on-p device) is connected to the EASIROC input seems to introduce more noise in the SiPM case → MORE WORK NEEDED TO DECREASE INJECTED NOISE

THE ORSAY TEST BOARD ALSO SEEMS A NICE TOOL FOR THE LARGE SCALE CHARACTERIZATION OF THE SiPM FOR THE CONSTRUCTION OF THE IFR!!

While our prototype electronics (IFR_ABCD, IFR_BiRO, IFR_TDC) did not include any **radiation mitigation feature, these must be included, most likely, in the final design of the SuperB IFR readout system**.

Each sub-detector group is responsible for integrating radiation mitigation features in its sub-detector specific readout; this might involve the use of flash based FPGAs on the hardware side and the use of proper design techniques on the firmware side(TRM, hamming coding for FSM ..) eventually assisted by currently available CAE tools.

We intend to explore solutions based on Actel proASICs as the target FPGA for the IFR readout system and Mentor Graphics HDL tools specifically design to automatize the

The task of prototyping and characterizing under radiation the critical blocks of the IFR data acquisitions could be shared with engineers form AGH University of Science and Technology

Conclusions:

While the prototype electronics which was designed so far allowed us to build a working small scale prototype, when preparing for the final system we should aim for a front end design based on suitable ASICs.

Also, while waiting for final estimates on the radiation doses in and around the detector, we should be prepared to estimate the costs and the performance toll of designing the front end electronics and latency buffers using radiation mitigation techniques.
This might involve some development at the ASIC level to protect DACs and other critical digital block from SEU

In these tasks as well as in the large scale characterization of the SiPM devices needed for the construction of the IFR, the AGH University of Science and Technology in Krakow would be a very welcome partner.