Updates on the R&D for the SVT Front End Readout chips

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Summary

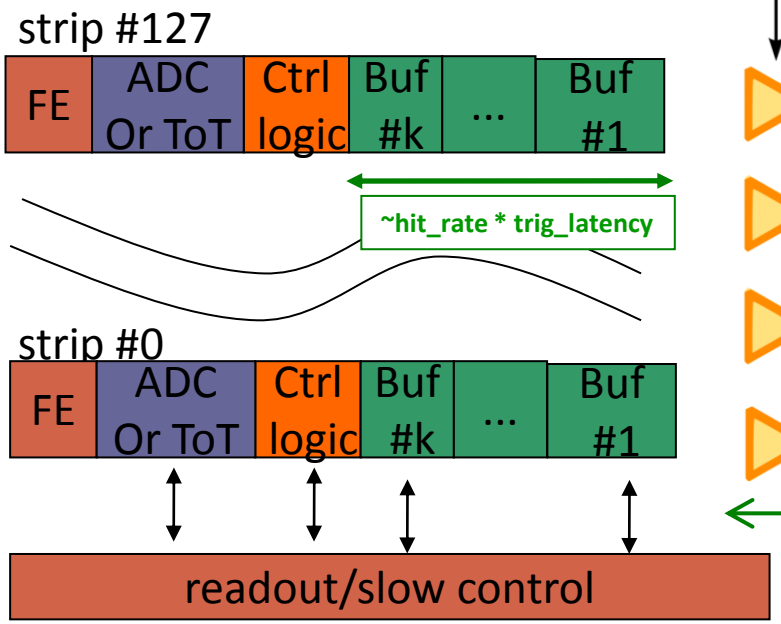
- Strip readout architecture
  - Investigated architecture
  - Preliminary simulations
- INMAPS matrix submission
  - Readout post synth. simulations and bug fixing
  - Layout updates
- Test Beam 2011
  - New chips integration on DAQ electronics
  - Integration in the TDAQ software

Strip Readout Architecture

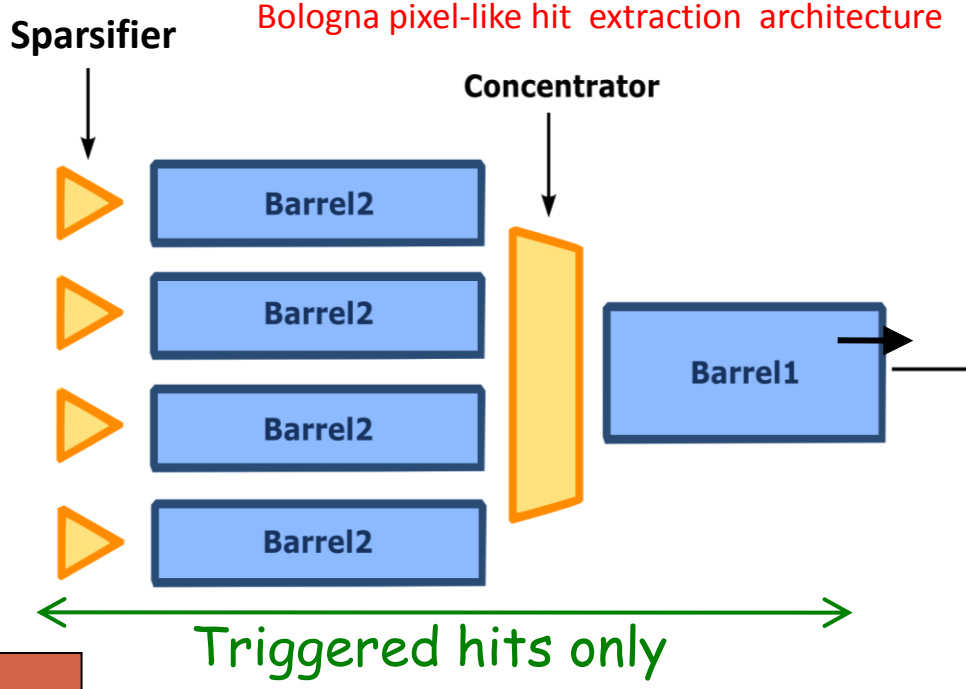
Preliminary studies

Strip readout architecture under investigation

Pre-trigger buffer array proposed by PISA
(F.Morsani G. Rizzo)



Bologna pixel-like hit extraction architecture



How many buffers?
How many barrels?

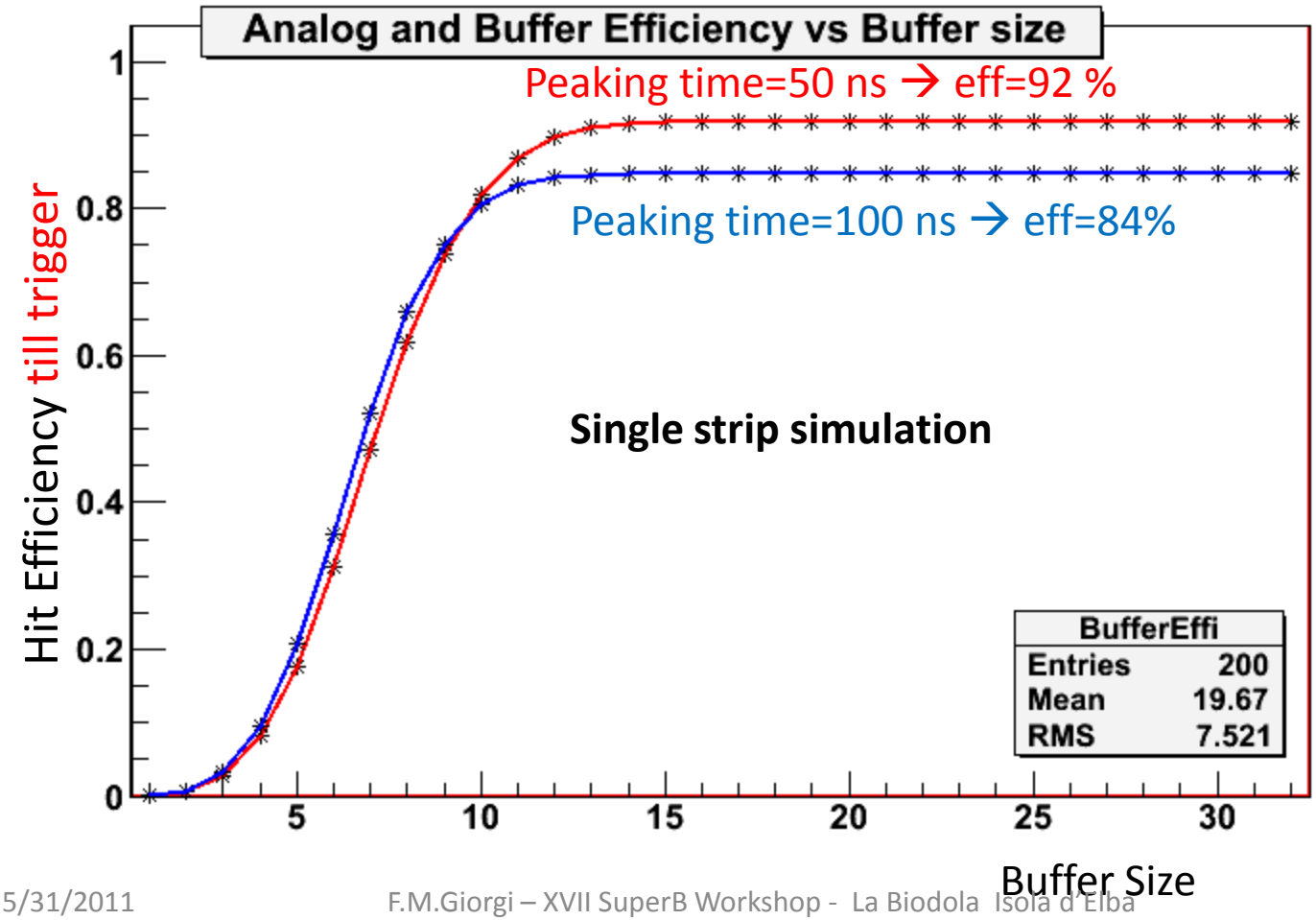
Asynchronous logic assumed:
Triggered event size not known a-priori
(thus readout time also)

Efficiency Study (by M. Villa)

- Parameter Space:
  - Trigger
    - frequency: 150 kHz (1.5 S.F)
    - jitter: 100 ns (the goal is to go down to 30 ns)
    - latency: 10 us (1.7 SF; LVL1 design is 6 us)
  - DAQ window: 100ns +2 Time stamps or 300 ns
  - Time stamping: 33 MHz (T(BCO)=30 ns)
  - Chip readout clock: 66 MHz (T(RDclk)=15 ns)
- Strip dead time equal to 2.4 peaking time
- Strip rates as given by Riccardo C. (5/13/11)
- High level simulation (C++) of MAIN features of a readout chip: Preliminary Toy Monte Carlo

L1 simulation: 687 kHz/strip

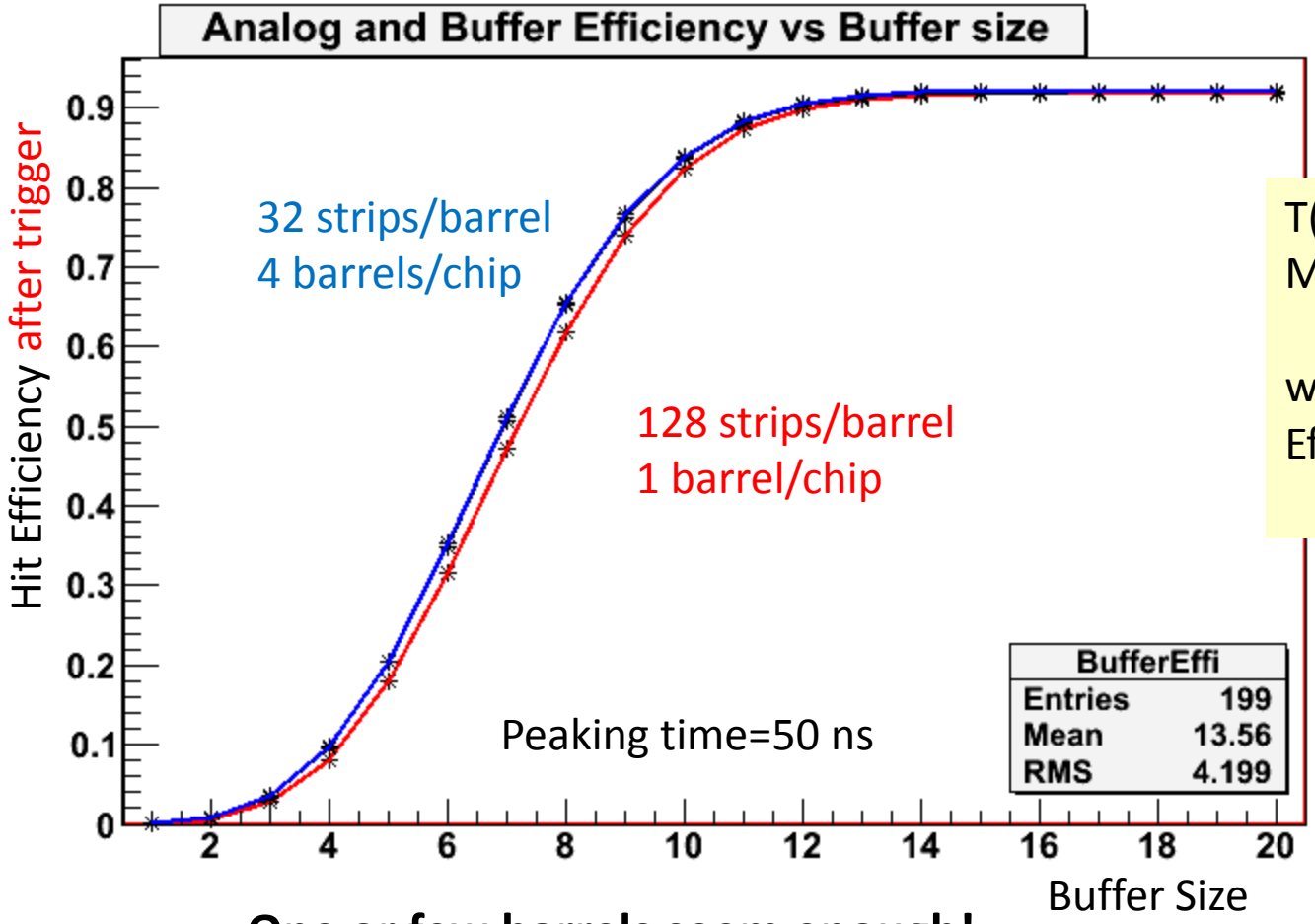
Inefficiency sources: Analog peaking time and limited buffer size.



MIP full charge release in the strip, no charge sharing → saturation efficiency underestimated.

Strip chip: how many barrels ?

Inefficiency sources: Analog peaking time, limited buffer size, sparsification time.



T(BCO)>2T(RD)
Mandatory!

when T(BCO)=T(RD)
Efficiencies at zero

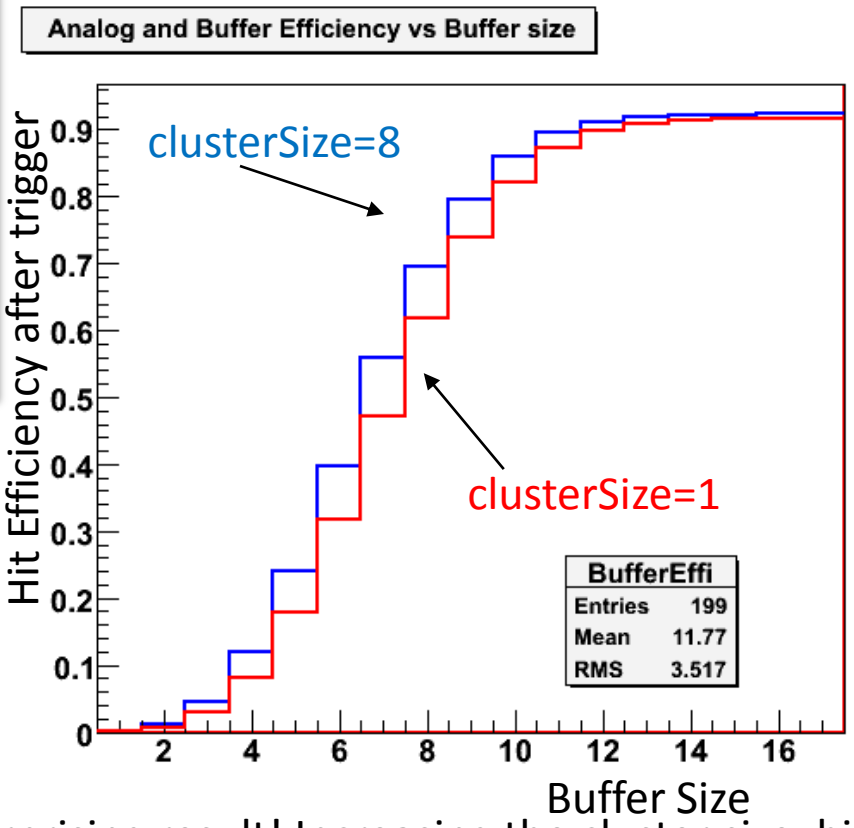
150 kHz trig rate
300 ns DAQ
time window

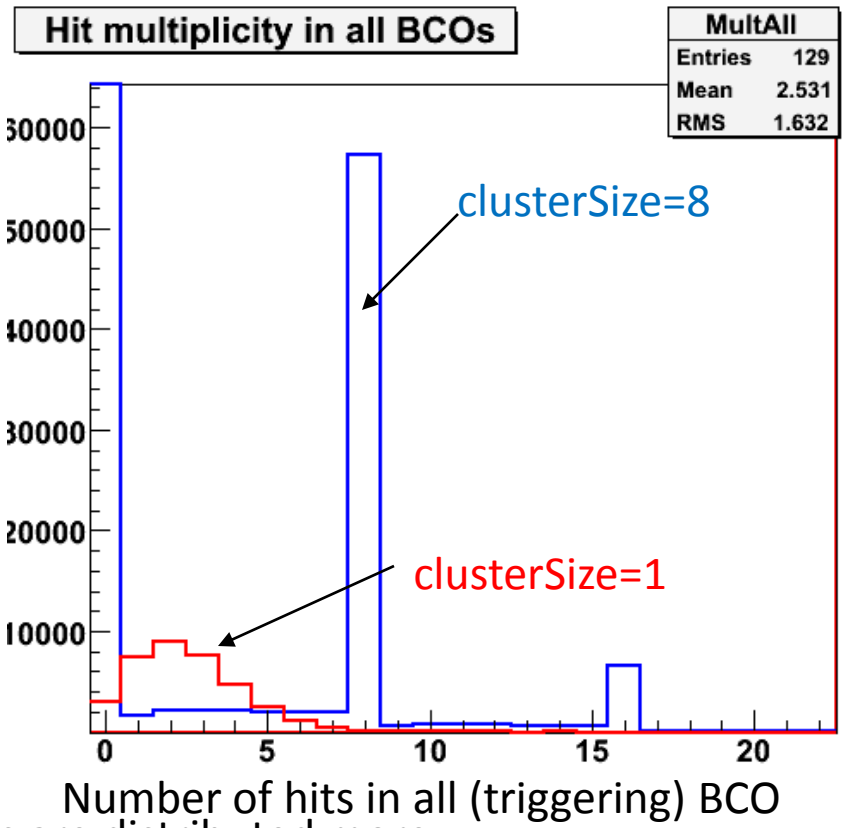
One or few barrels seem enough!

Cluster size effects

fixed hit chip rate
L1: 687 kHz/strip

Peaking time=50 ns, 128 strips/barrel, 1 barrel/chip



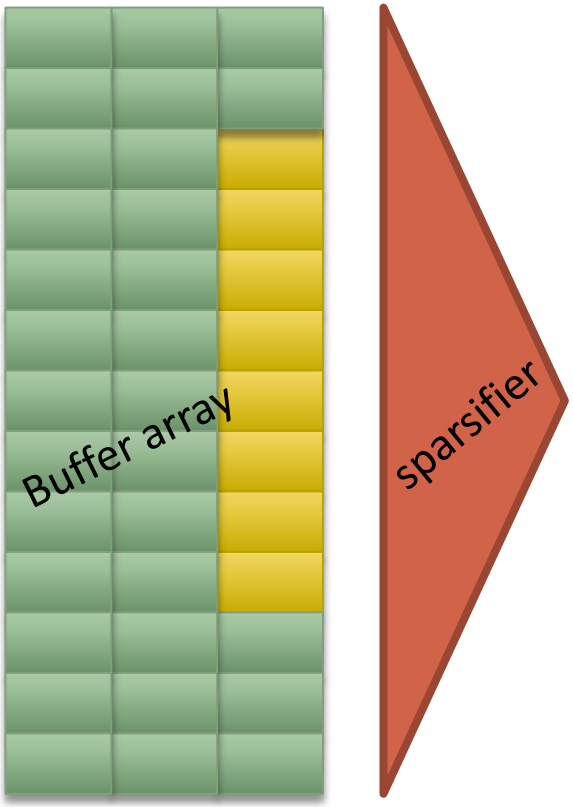


Surprising result! Increasing the cluster size, hits are distributed more uniformly along the strips. At a fixed hit chip rate, less buffers are needed!
Despite a longer reading time on triggering BCO for BCO with hits, they are rarer.

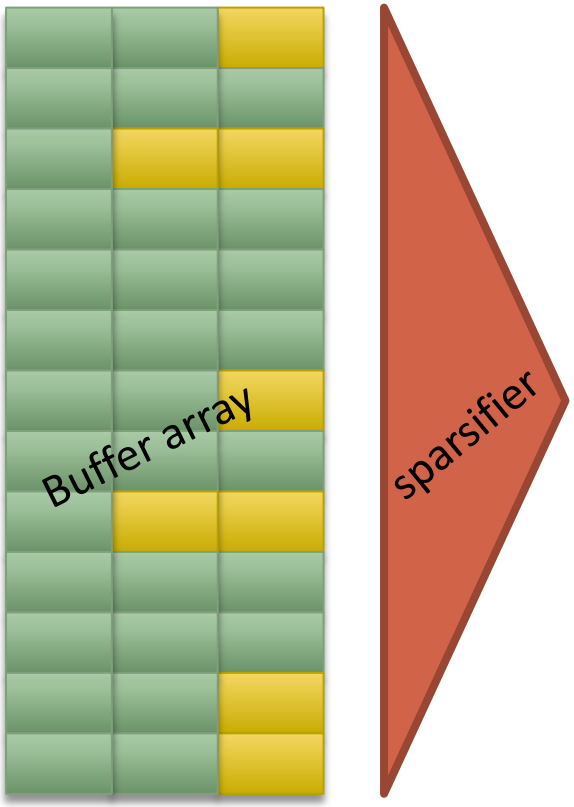
Cluster size effects

Same rate

Cluster factor 8



Cluster factor 1



More likely pile-up in buffers,
More buffering needed.

INMAPS 32x32 Matrix Submission

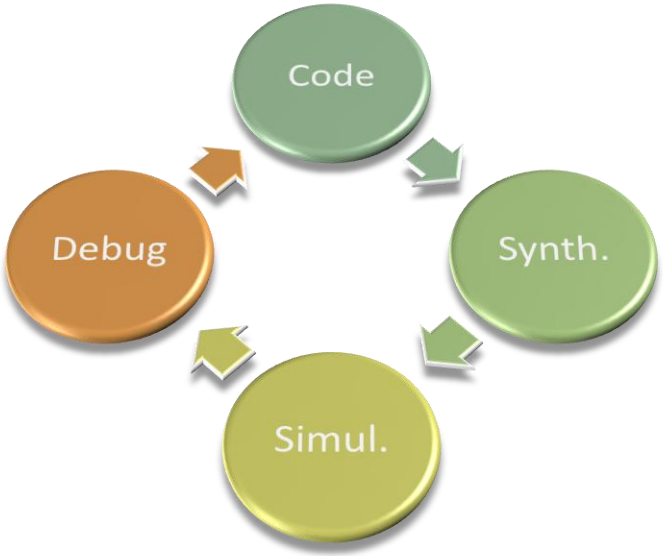
July 2011

The project

- CMOS 180 nm, 4-well process
- INMAPS pixel sensors (ref. to V. Re presentation)
- 32x32 pixels matrix (F. Morsani)
  - Column addressable with in-pixel TS selection
  - Parallel output
- Integrated readout, SQUARE architecture:
  - Synthesizable VHDL architecture model.
  - 2 sub-matrices control with parallel hit extraction
  - 1 column sparsification in 1 clock.
  - Cluster compression algorithm
  - Triggered and Data push working mode
  - Parallel output.
  - I2C-like slow control.

Implementation Updates: Post-synthesis Simulations

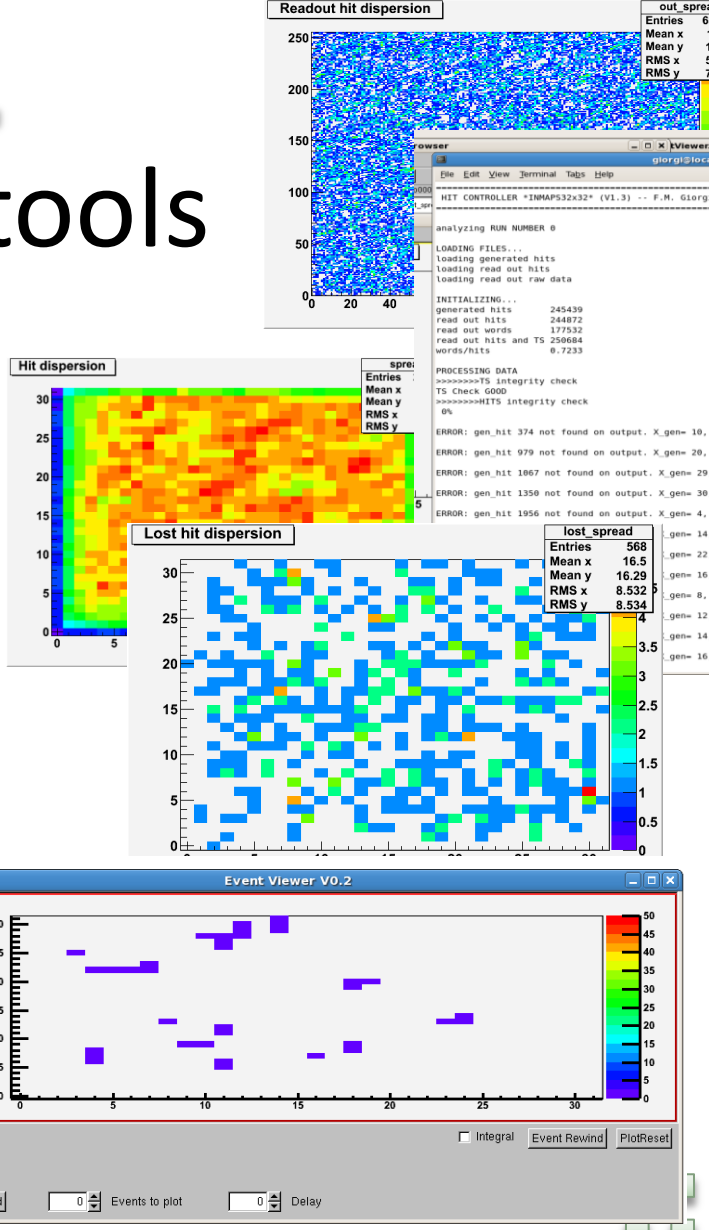
- Hit-by-hit cross-checking
- Apparent hits mismatch, hit logger fixed.
- Fixed matrix mask setting procedure (hold violations prevented the masks to set properly)
- Now behavioral and post synthesis simulations are in good agreement.



Simulation check tools

- Several debug tools were developed during last years to help the simulation checks compatible with all the architecture kind of data and with adjustable matrix size
  - VHDL Monte Carlo generator based on physics simulation parameters with efficiency estimations (latched hits/ generated hits)
  - Hit X-check (latched hits/readout hits)
  - Event display
  - Cluster analysis

After a fine tuning, they have been run also on post-synthesis simulation data and we found them very useful, again.



Implementation Updates: Layout

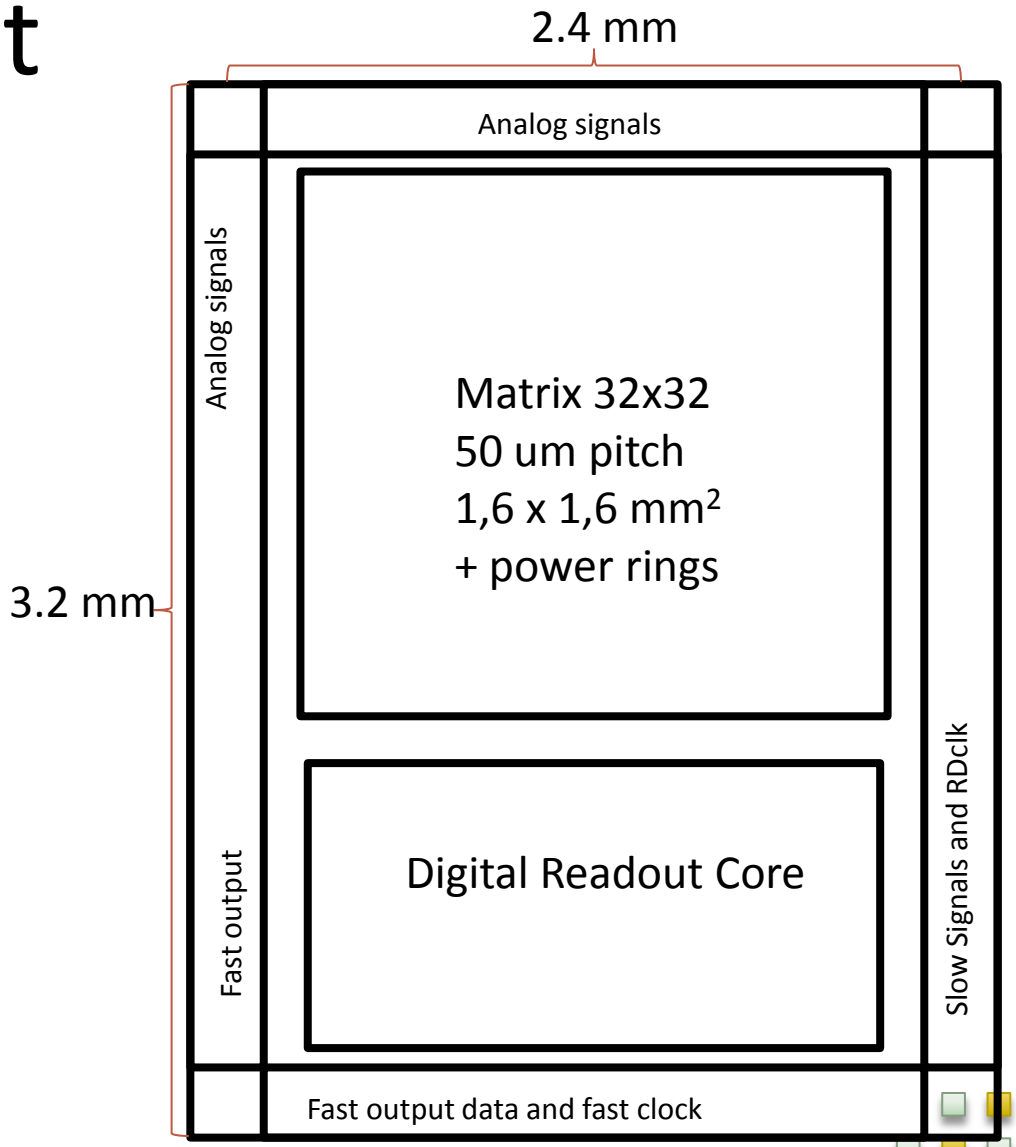
- The fixed revision of readout has been synthesized.
- The layout phase has started with encouraging results.
- Received the Matrix Object. To be placed.
- Placing and routing ~ 35 k cells.

Layout

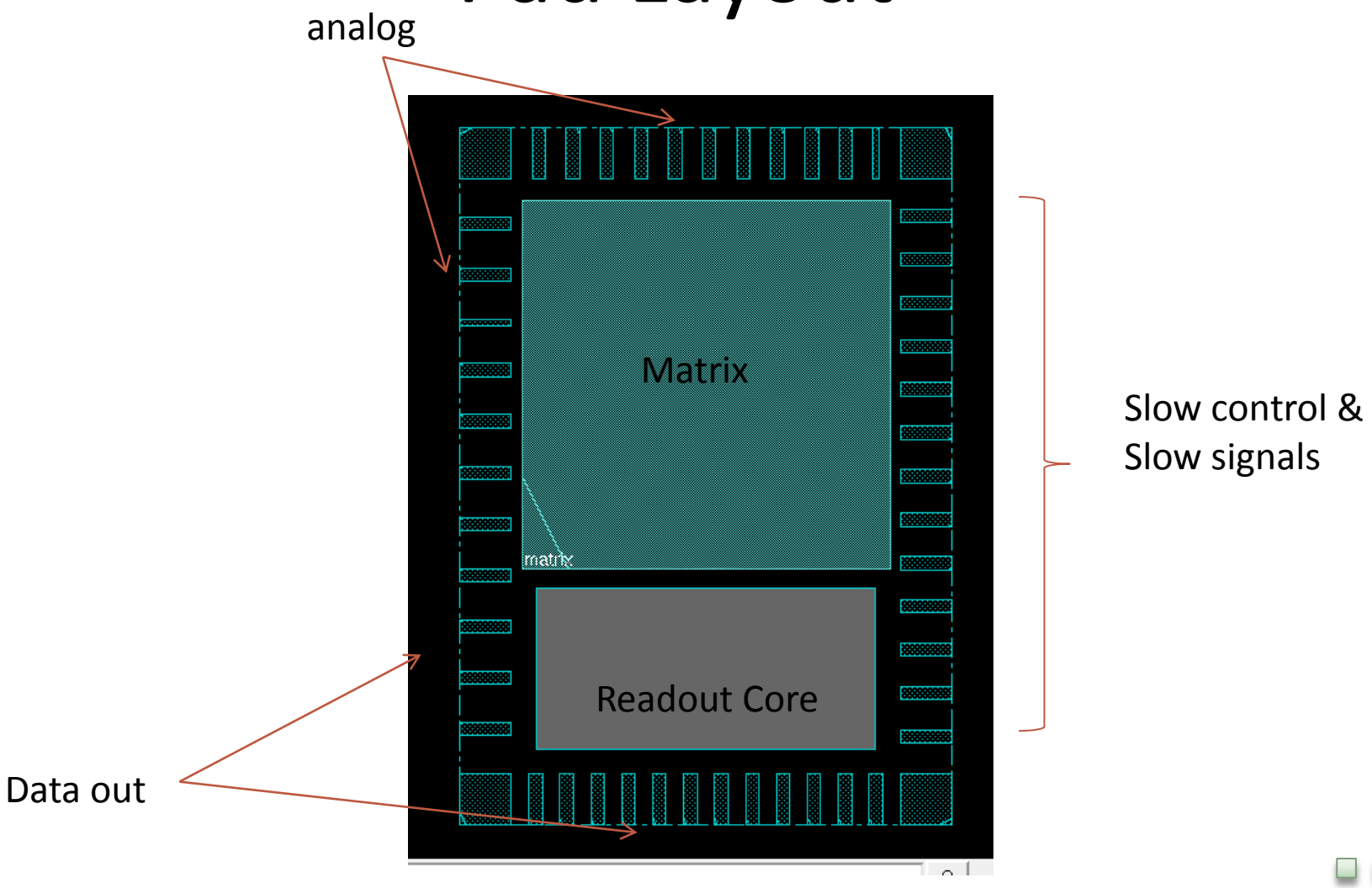
DIGITAL PADS
- Reset
- RDclk
- fast_clk
- BC_clk
- Trigger
- data_out[11:0]
- data_valid
- ML_ena
- GlobalFastOR
- SDA
- SCL
- chip_addr[2:0]

ANALOG PADS
- Sub
- Pixel_in
- Pixel_out1
- Pixel_out2
- Rif_in
- Rif_mir
- V_th
- RIF_FB

POWER PADS
- 2xVDD/VSS Core power
- 2xVDDO/VSSO Output power
- 2xAVDD/AVSS Analog power



Pad Layout


analog
Matrix
matrix
Readout Core
Slow control &
Slow signals
Data out

CERN Test Beam September 2011

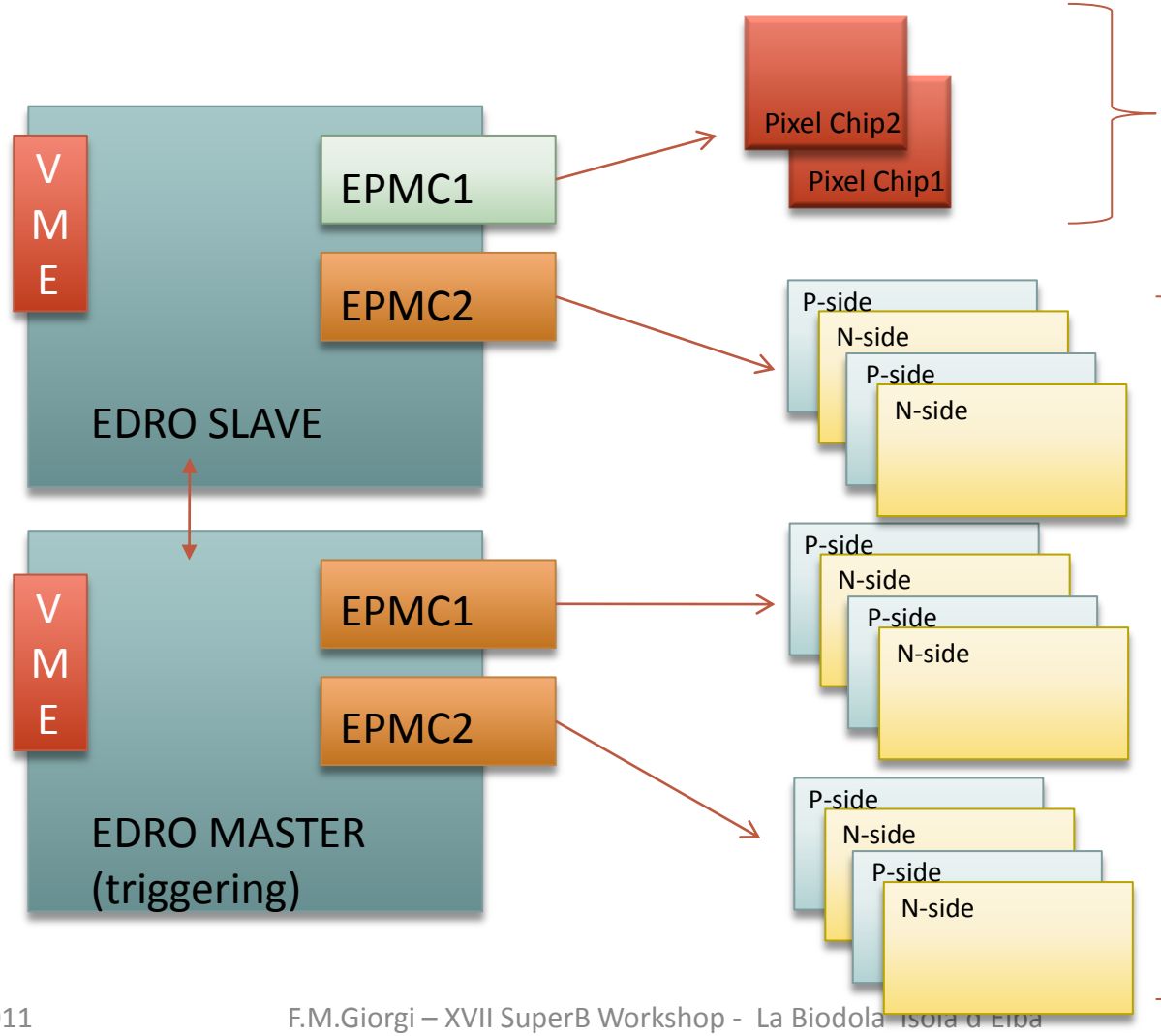
Bologna Updates

DAQ electronics

New flexibility required respect to 2008 test beam, different pixel chips with different readout implemented to be tested simultaneously.

- 2 EDRO boards
- 2 EPMC for each EDRO
- 2 Strip modules for each EPMC (4 sides)
- 6 FSSR2 chips for each strip module
  (same as sept. 2008)
- 1 EPMC devoted to DUTs to be chosen from:
  - EPMC_PIXEL: 2 data channels for DIGITAL pixels
  - EPMC_STRIP: 4 data channels for striplets/ strips
- Analog structures take another way to tape.

DAQ scheme (EPMC_PIXEL)

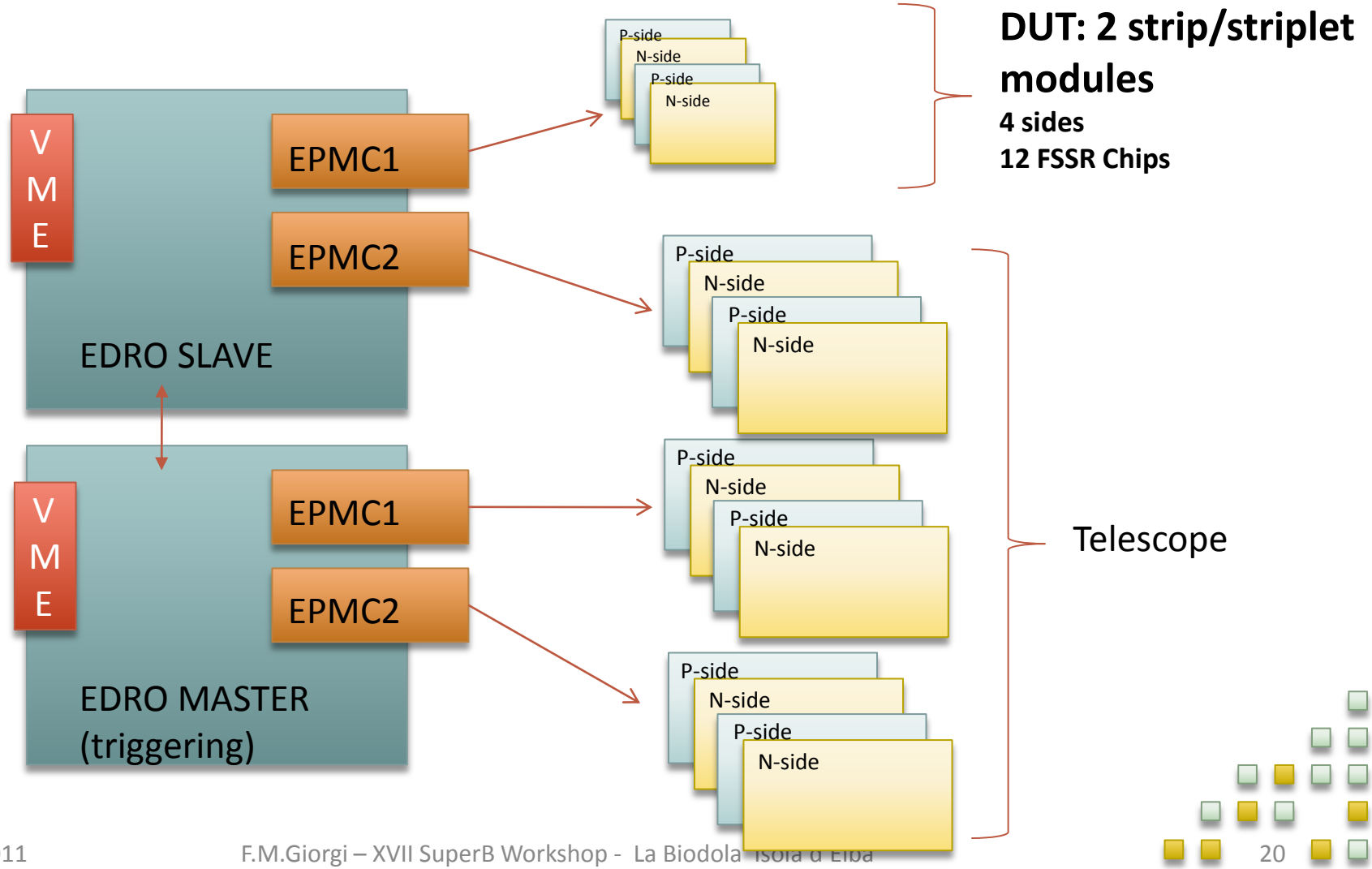


DUT: 2 Pixel chips:

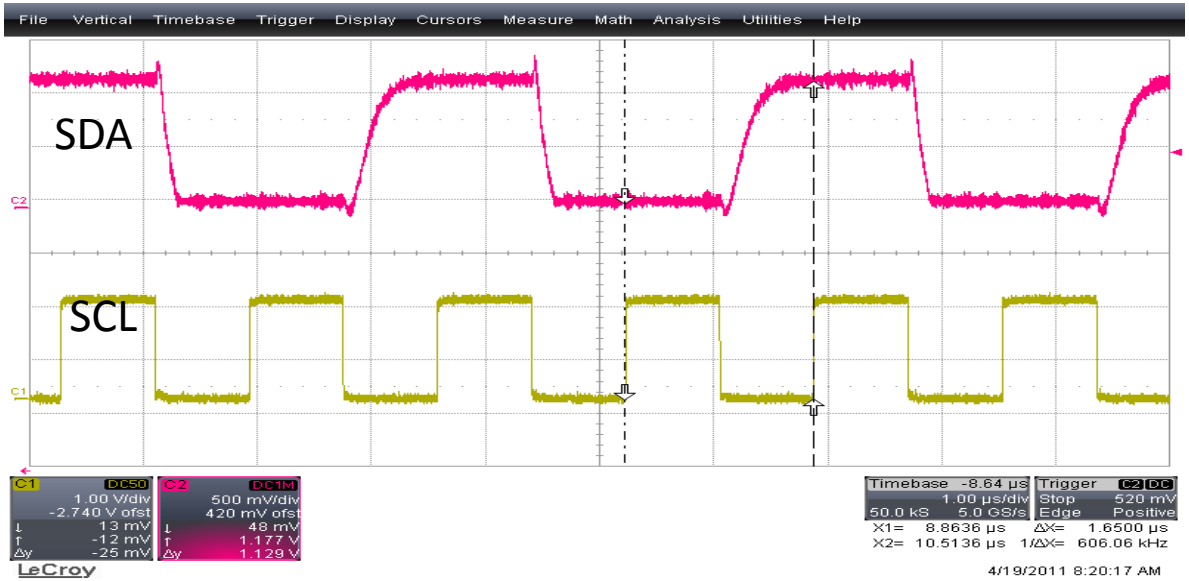
Choice between these chips
APSEL4D (AREO readout)
APSEL4D1 (AREO readout)
APSEL3D (AREO readout)
APSEL3D_TC (AREO readout)
SuperPX0 (SORTEX readout)

Telescope

DAQ scheme (EPMC_STRIP)

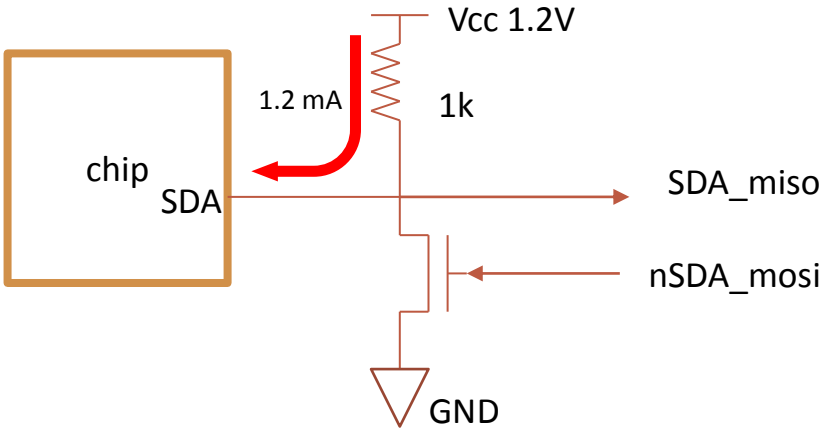


EPMC firmware test
Basic SPX0 communication



Tested SPX0 I2C communication with new EPMC firmware.

In figure 600 kHz, tested OK up to 1.2MHz



TDAQ integration

- The new EPMC modular firmware for pixels established new TDAQ control interfaces
- Integration of the new interfaces in software started.
- Integration in the GUI configurator started as well.
- Perugia people now in Bologna integrating in the global TDAQ
- Remotely operable table received from Torino, now in Bologna for the July tests. New movt. features to be added in automatic logs.

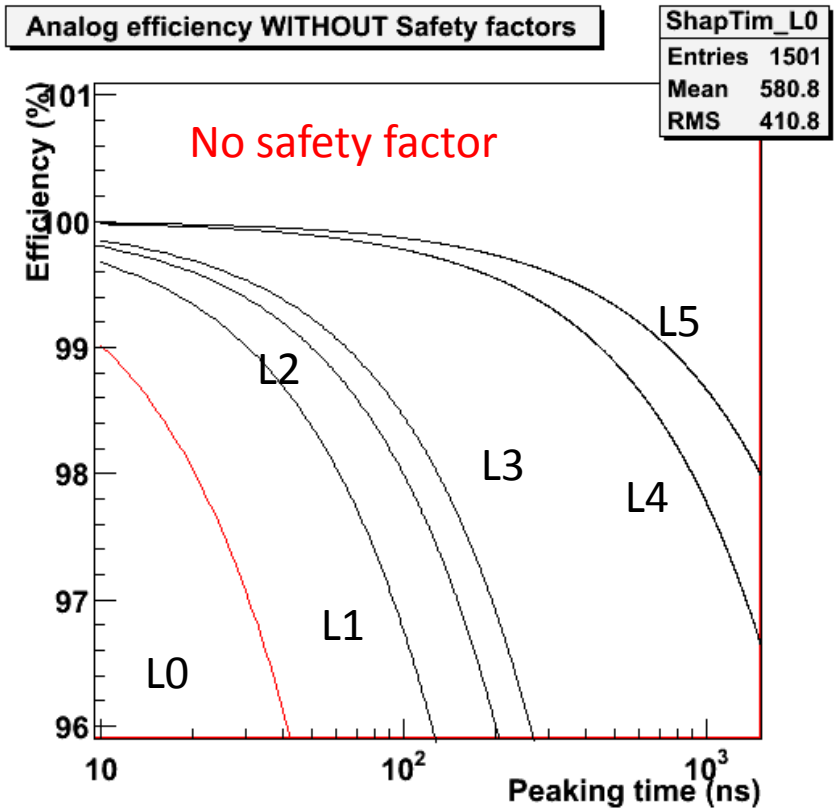
Conclusion

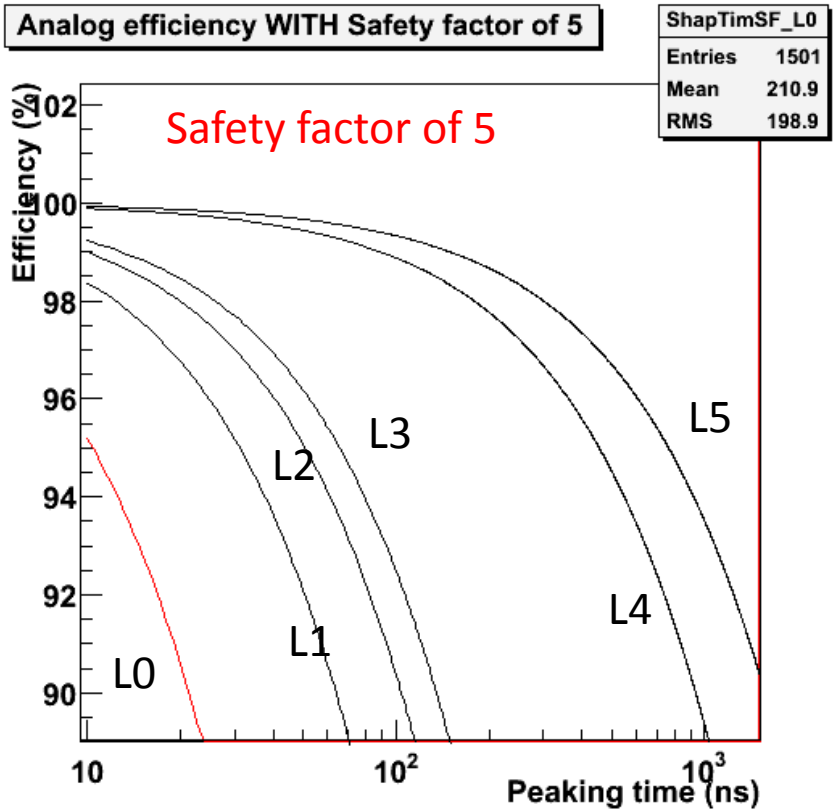
- Mini Monte Carlo on proposed striplets readout architecture pointed out (L>=1):
  - Required buffer depth depends on peaking time, 20 is enough for a 50 ns peaking time.
  - One ore few barrels are enough
  - Clusters helps: clustered events require shorter buffers
- INMAPS submission
  - Some bugs fixed after post-synthesis simulations (the majority in the test bench code, rather than in the readout core)
  - Layout implementation started
- September Test Beam
  - New EPMC firmware deployed
  - Communication tests successful with SPX0 chip.
  - TDAQ software integration started .

Back-Up

M. Villa

Efficiency vs Peaking time





97.6% eff → Tp(L1)=74 ns

97.6% eff → Tp(L1)=15 ns

Strip Rates

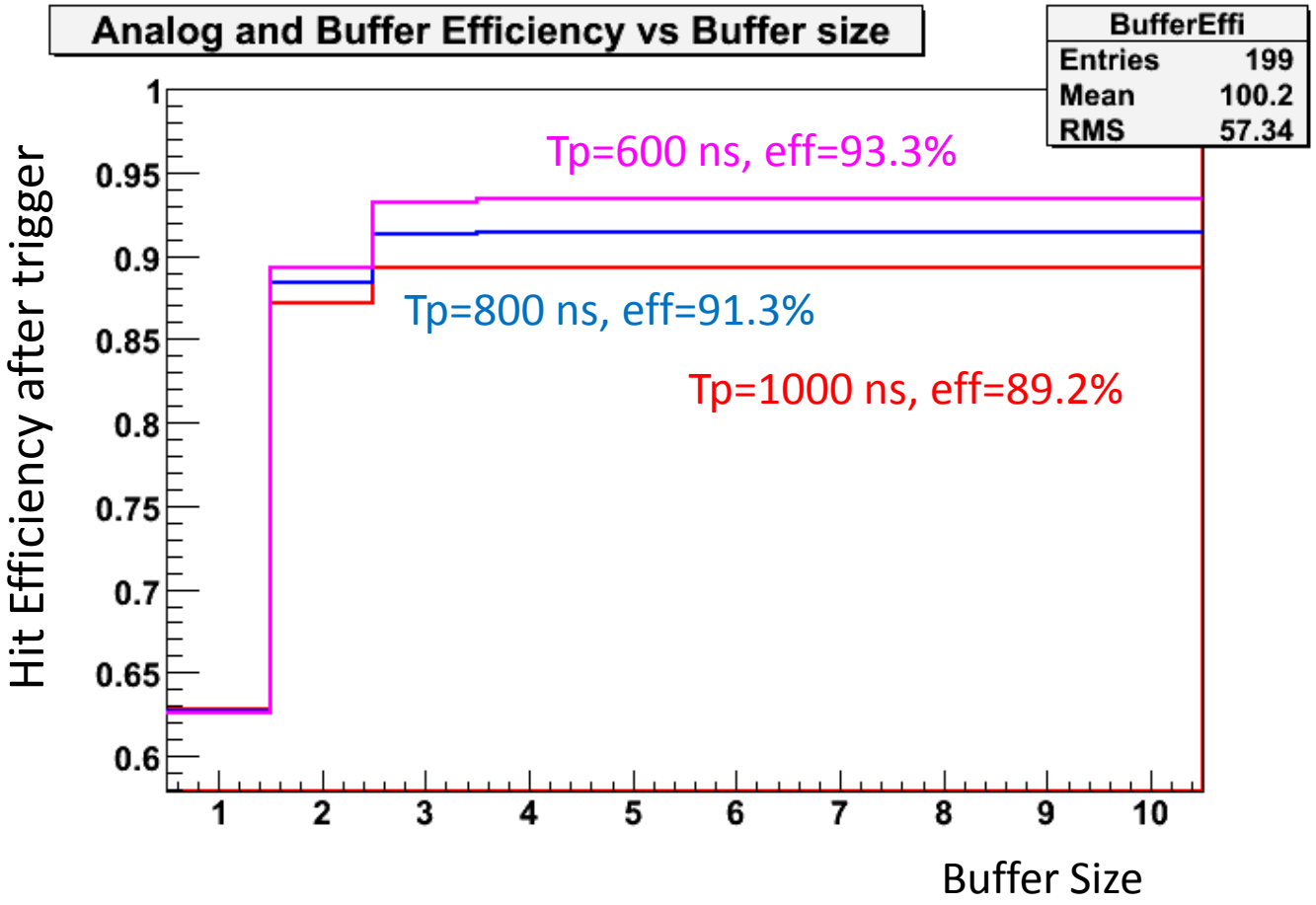
- Strip rates as given by Riccardo C. (5/13/11):

new values	old values
• L0: 2060 kHz/strip	~ =
• L1: 687 kHz/strip	(268 kHz/strip)
• L2: 422 kHz/strip	(179 kHz/strip)
• L3: 325 kHz/strip	(52.5 kHz/strip)
• L4: 47 kHz/strip	(21.9 kHz/strip)
• L5: 28 kHz/strip	(18.7 kHz/strip)

Max peaking times (ns) at fixed strip efficiency

Target strip efficiency	97.6%		95%		91%	
	SF=5	SF=1	SF=5	SF=1	SF=5	SF=1
L0	5	25	10	52	19	95
L1	15	74	31	156	57	286
L2	24	120	51	253	93	466
L3	31	156	66	329	121	605
L4	215	1077	455	Max	836	Max
L5	361	1807	763	Max	1403	Max

L4: 47 kHz/strip but longer deadtimes

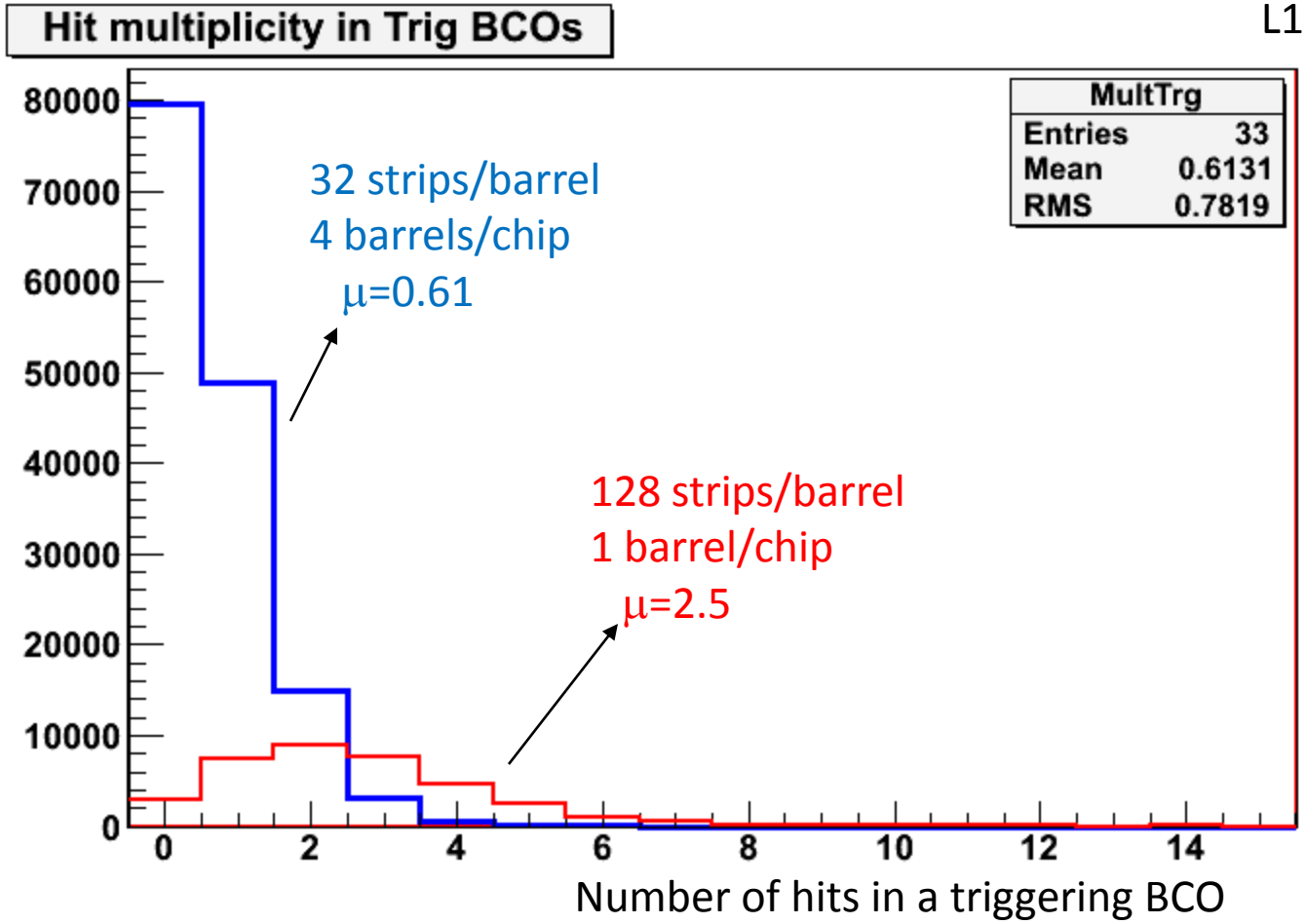


For outer layers (smaller hit rate) the buffer size is not a problem: 5 buffers/strip seem enough. The dominant parameter is the analog dead time.

M. Villa

Hits in triggered BCO

L1: 687 kHz/strip



Even with just one barrel, the average multiplicity is LOW.

If T(BCO)>2T(RD) there is enough time to read the hits out

Efficiencies vs rate and dead times

Layer	C_D [pF]	t_p [ns]	ENC from R_S [e rms]	ENC [e rms]	Hit rate/strip [kHz]	MMC Efficiency
0	11.2	25	220	680	2060	(0.732)
1	26.7	50	650	1190	687	**0.917**
		100	460	930		**0.841**
2	31.2	50	830	1400	422	**0.948**
3	45.8	50	1480	2130	325	**0.960**
4	52.6	1000	340	820	47	**0.893**
5	67.5	1000	500	1010	28	**0.934**

Pessimistic: Cluster size 1, no charge sharing, worst peaking time

Conditions: 20 buffers, 150 kHz trigger rate, 300 ns time window for all layers.
Buffer overflow on Layer 0