XVII SuperB Workshop and Kick Off Meeting:
SVT Parallel Session

Update on HDI design and peripheral electronics in Milano

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on behalf of INFN and University of Milan

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  - Test on data rate on ~ 1m length cables
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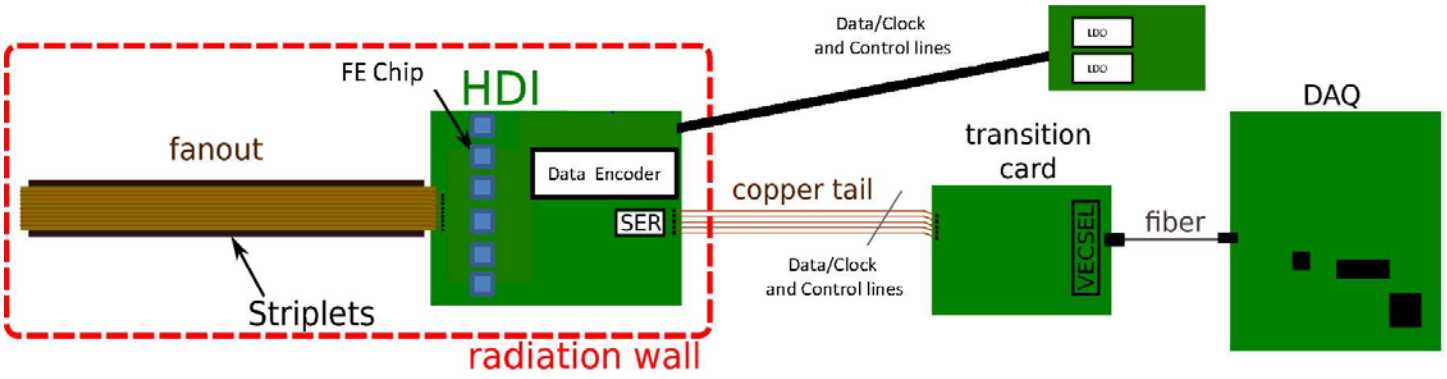
Data / Power Chain



NOT to scale

- **The baseline system has been considered**
- **The goal is to develop a chain which is moderately dependent from the Layer 0 “detector/FE chip” choice**
  - The Layer 0 chain is taken as example, the outer layer should be able to use a “similar” data/power chain

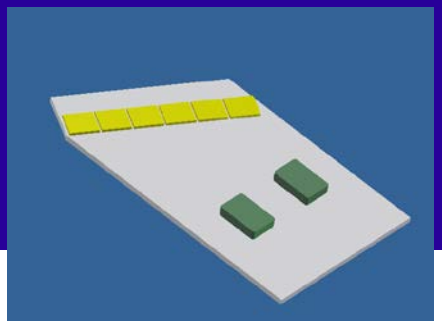
Bus / Fan-out status (1 of 2)

- **No substantial progresses from March**
  - The final layout has been updated following latest CERN suggestions
    - Opening on the ground/power planes have been enlarged and re-positionated
    - Bonding procedure (Bus to Sensor and FE chip) needs to be reviewed with Pisa
  - A sign-off meeting is planned for next week
  - Production is supposed to take 4-5 weeks
    - CERN under pression from LHC upgrades

Bus / Fan-out status (2 of 2)

- **Search of commercial partner is on going**
  - **Two possible firms have shown interest**
    - One firm is in France, while the other is in Italy
    - Both company will start from a thin commercial Copper/Kapton tape (5 um / 25 um) and pattern the layout by etching
    - They have experience with minimum lines/space resolution of 50/50 um (twice the baseline for striplets) over 10 cm lenght as a maximum
  - **Neither of them have ever done 25/25 um**
    - Only CERN shop has ventured in such a fine pitch
    - Industrial experience on kapton is limited

SuperB HDI (1 of 3)



Technology for SuperB HDI: AlN thick film hybrid

Irregula shape is not an Issue

Detector fan-out is glued on the hybrid edge and chips inputs are wire bonded to the fan-out.

Five conductive layers (3 power/ground layers, 2 for signal)
However, each additional signal layer for HDI-0 will “degrade” planarity and line resolution

New layout rules
- layer thickness ~ 65 µm (5% tolerance *)
(15 um conductor and 50 µm dielectric)

•Thickness usually decreases during oven curing

• Line size/space: inner signal layer >100/100 um (typical 150/150 um), 200/200 um TOP layer

• Pads 200 x 200 um*2

• Vias 200 um, space between via ~ 250 um

SuperB HDI (2 of 3)

Some Open Issues	
No systematic impedance control	Limited possibility to change the dielectric layer thickness with the standard process. By print screening company prefers a standard "3 pass" procedure → dielectric thickness ~ 50 um. Some avenue to be pursued: a) evaluate the usage of dielectric in tape (predefined thickness) → limited choices of thick film materials compatible with AlN b) Mix AlN and Al2O3 film materials. Possible after the first power/ground layer.
Clock lines were "qualified" by try and test in Babar	Difficult prediction of Z → dielectric constant usually not well specified by material manufacturer (ex. in next slide)
Some prototypes were produced to master the technology	Same approach to be pursued. Of particular interest is the implementation of differential lines (digital signal ~ 150-250 MHz) Prototype: small substrate (length counts), two layer (plane and one signal), array of lines of minimum size (number to be defined)

SuperB HDI (3 of 3)

Mechanical Properties Comparison

Table 1

Property	AlN	BeO	Al203
Dielectric constant	8.9	6.7	9.8
Dielectric loss	0.0001	0.0003	0.0002
Resistivity (Ohm-cm)	$>10^{14}$	$>10^{14}$	$>10^{14}$
Thermal cond. (W/mK)	170-200	260	36
CTE (ppm/C)	4.6	8.5	8.2
Density (g/cm3)	3.30	3.85	2.89
Bending strength (mPa)	290	230	380
Hardness (GPa)	11.8	9.8	14.1
Young's mod (GPa)	331	345	372

Complete Thick Film Material System

DuPont offers a complete system of thick film materials designed to take advantage of the excellent thermal properties of AlN (see **Table 2**). The thick film material performance is consistent across different substrates from major vendors.

Additional technical information is available in the AlN Material System Selector Guide.

Table 2
Thick Film Materials for Aluminum Nitride

	AlN Resistors					
Product	AN592	AN599	AN610	AN615	AN620	AN630
Chemistry	Pd/Ag	Pd/Ag	RuO_2	RuO_2	RuO_2	RuO_2
Resistance	200 mΩ	1 Ω	10 Ω	50 Ω	100 Ω	1 KΩ
TCR (ppm/C)	+300 to +400	±100	±150	±150	±150	±150
	AlN Conductors and Dielectric					
Product	AlN44	AlN11	AlN21	AlN23	AlN33	AlN71
Chemistry	Diel	Ag	Ag/Pt 100:1	Ag/Pt 3:1	Ag/Pd 10:1	Au
Solderable						
62/36/2	N/A	X	X	X	X	N/A
10/88/2	N/A	X	X	X	X	N/A
Platable	N/A	X	X	NT	X	N/A
Brazable	N/A	X	X	NT	X	No
Wirebondable						
Au	N/A	X	X	N/A	NT	X
Al	N/A	NR	NR	NR	NT	X

Dielectric (crossover)

Based on current customer surveys, a crossover dielectric will meet many of the applications for AlN substrates. Our major effort was focused on tuning the TCE of the composition to better match with that of the substrates, while at the same time making the film dense and hermetic. Good adhesion of the film on AlN substrates was also observed after firing in an ambient atmosphere. Electrical properties of the film met all the requirements as a crossover dielectric. Table II summarizes the properties of the dielectric.

Resistors

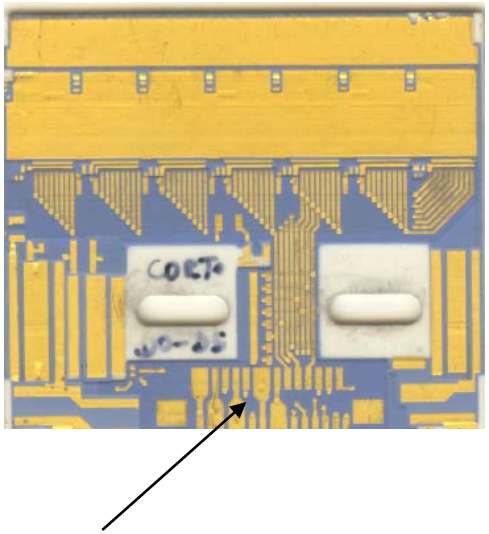
A new Pb-free resistor series, referred to as ALN6X, has been developed to produce stable high performance resistors on AlN substrates with the new Ag-based conductors. Resistor values range from 100 mΩ to 1 kΩ/sq. ALN59 (100 mΩ) and ALN60 (1 Ω) are based on a Pd/Ag

Table II
Characteristics of crossover dielectric

Fired thickness (μm)	40-45
Cosmetic	Blister free
Dielectric constant (1 MHz)	< 10
tan δ (1 MHz)	< 0.5%
Insulation resistance	> 10E + 12 Ω
Breakdown voltage	> 25 V/μm
Compatibility	Au and Ag-based
Stewardship	Pb, Cd and Ni free

The dielectric constant is specified only as an upper limit.
In the dielectric are present organic vehicles.
During the initial drying process (at ~150 C) the organic vehicle evaporates and the paste becomes a semi-solid phase mixture of dielectric and binder. Only proper curing will eliminate completely the residue.

HDI … looking at Babar



High density connector should be chosen to connect power and signals to the “tail” **(Berg, Panasonics, etc…). Height after matching ~ 1.2 mm**

The HDI must keep some/all the functionalities previously implemented:

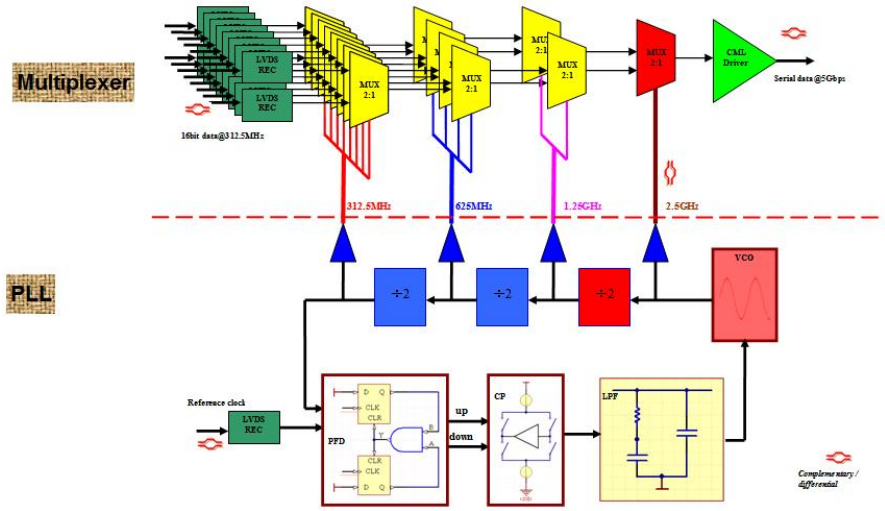
1. Analog and digital powers. At least two different power supplies: analog and digital.
2. Two different current return, one for the digital current (DGND) and one for the analog current (AGND)
3. Each power line must be locally filtered
4. Two redundant sets of differential clock and command lines must given to all the chips and terminated so as to match with the characteristic impedance of the “tail”
5. Redundant differential data lines must be connected
6. Each HDI must host and provide connections to one resistive temperature monitor.

…. More

+ High speed data need to be transferred on the HDI

- → **Data formatted from FE to “Data Encoder”**
- → **16:1 LOC 1 Serializer**

Low Speed / Low Power Serializer



The block schematic of the SMU LOC1 shows that the typical power of the chip (~ 500 mW at 5 Gbps) has a substantial contribution coming from the PLL circuit.

A “Tunable” Serializer (data rate from 2.5 to 5 Gbps) can be obtained by changing the PLL.

The goal is to reduce the power to ~ 250 mW at 2. 5 Gbps

Simulation results indicate that (courtesy of SMU) :

	LOCs1 (mW)	low power design
CML Driver	96	50%
PLL	173	80%
Others	187	30%

The final design/prototyping phase of this Low Speed /Low Power IC did not start, yet.

SMU has received expression of interest by other experiment for such a development

SMU is looking into opening a collaboration on such IC (technology is 0.25 um Silicon on Sapphire)

Data/Clock and Control Cables

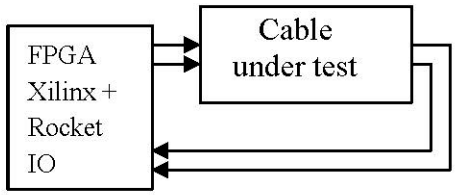
Kapton tail is probably not a solution for SuperB

- data speed is much higher than before
- differential/coaxial lines are not usually designed in flat circuits

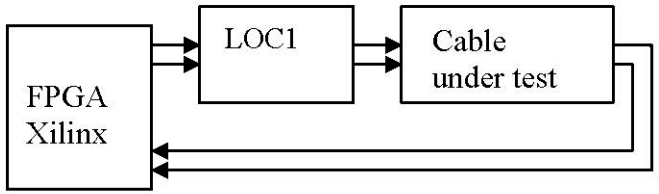
Some small and flexible cables have been selected and tests are on-going

Some preliminary results are shown

- the reference lenght has been chosen ~ 1m
- the test has been performed using
  - Xilinx FPGA + Rocket IO as a reference
  - Xilinx FPGA + LOC1 serializer as a comparison

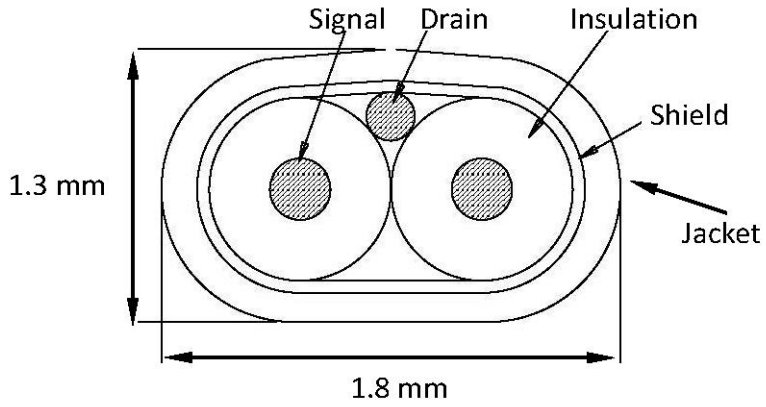


Configuration 1



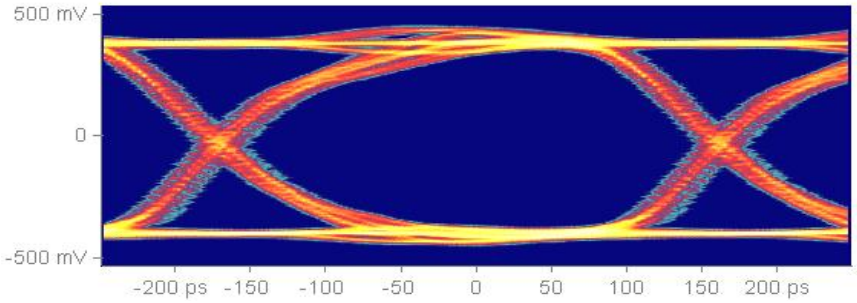
Configuration 2

Data/Clock and Control Cables (2 of 3)

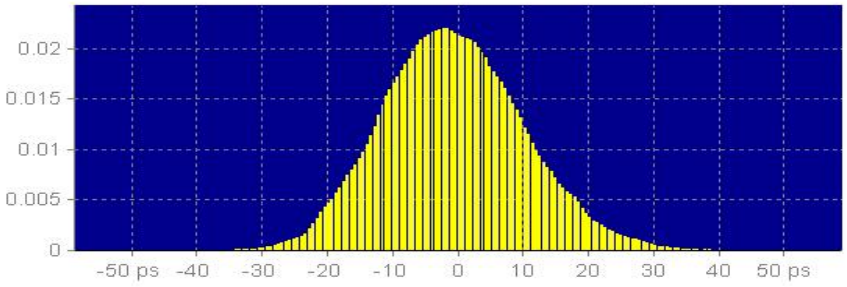


Signal: 30 AWG, Solid Copper Clad Aluminum
Differential Impedance ~ 100 Ohms +/- 5%
Capacitance: 16 pF / ft
Propagation Delay: < 2 ns/ft

The preliminary measurements show that LOC1 can drive such a cable without substantial degradation even without pre/post emphasis

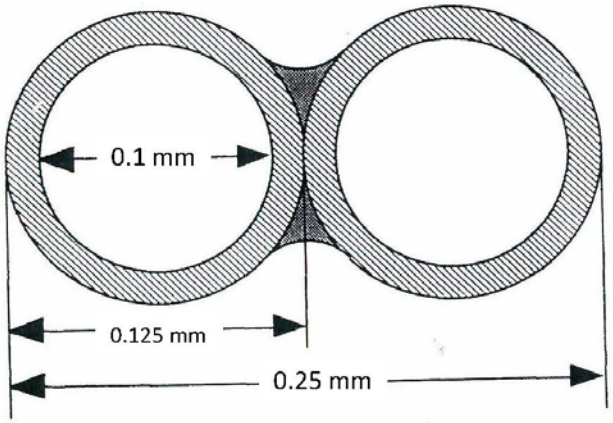


Eye diagram



BER probability density function

Data/Clock and Control Cables



Signal: 39 AWG, Bifilar magnet wires (Cu)
Differential Impedance: to be measured
Capacitance: 75 pF/m
Propagation Delay: to be measured

Dielectric costant: 2.1

Twisting is not needed for such a small wire

It probably can be purchased in tapes with multiple wires

- mechanical stress to be performed
- bending radius (no deformation) not known

Electric test not yet started

- difficult to make proper connection to test set-up

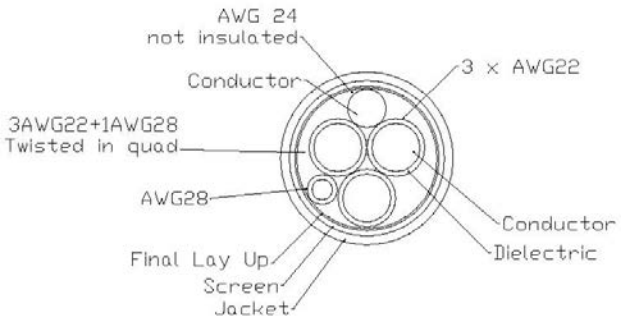
Transition card

No activities on designing the transition cards

However some preliminary study on the ”power distribution”:

- micro power cables made by siltem isolated quad twist multi strands AWG22 wires has been acquired and are going to be tested
- the idea is to define relatively soon the requirements for LDO regulator to be placed ”near” the HDI
- such LDO will use sense lines to ”predict” exact voltage to the load.

First parameter to be defined is Max Tolerable Voltage at load to avoid FE chip damage in case of failure
→Based on technology → for 0.13 um ~ 2.0 Volt
→For calculation ”zero current consumption” is assumed, i.e no drop on power cables
→Drop on round trip must be used
→Power lines are shared on more than IC .... Worst current ....
→Sense failure protection scheme must be ”fast”



AWG 22 (made of 37 x 0.114 mm individual wires)
Resistance nom.: 5.08 Ω /100 m
(or 16.25 Ω /100 m for Cu clad Al)
Diameter: 0.78 mm

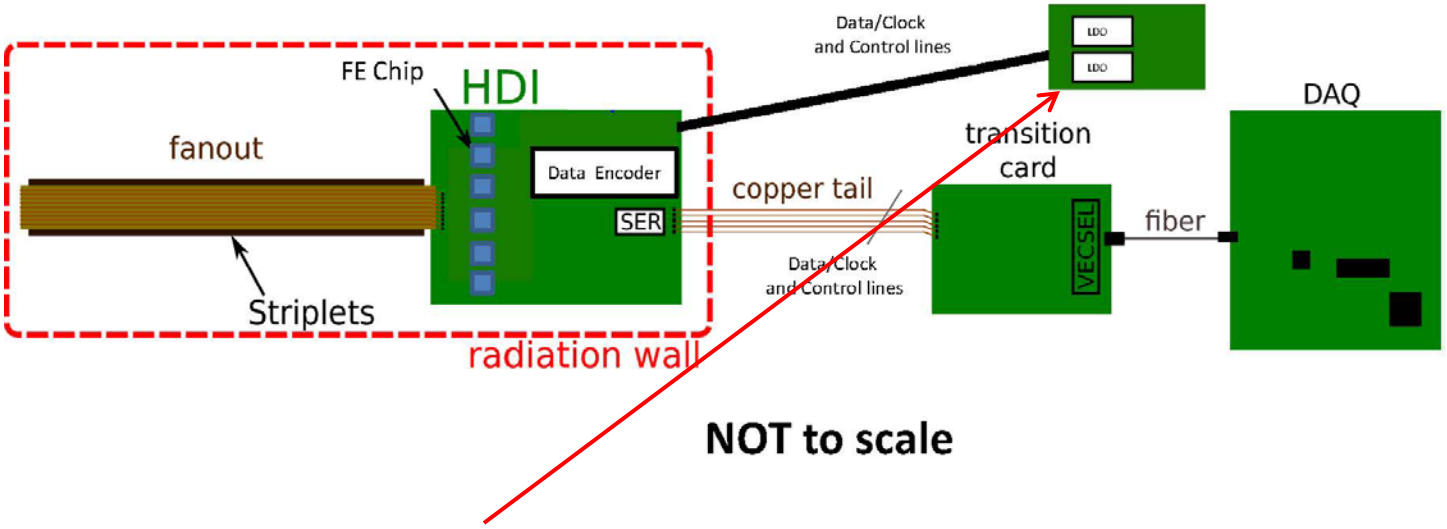
Not advisable to use smaller size cables (fragile, heating)

For HV we could use AWG 30 and up.

Drop estimate

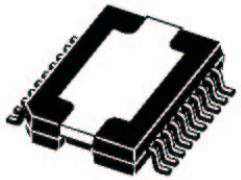
Recipe for calculation:
- Worst current on a power cable → ?
- Max drop allowed from LDO to end of sense lines → ?

Results: Size of wires and max distance from load !



Size needed for PCB ~ 5 x 8 cm, it needs moderate cooling

Possible radhard LDO …. from CERN



PowerSO-20 (Slug-up)

Main Features of the ST regulator:

Max current 3 A

Input Voltage < 14 V

Adjustable output voltages from 2 to 12 V

Typical dropout voltage of 0.5 V @ I= 1 A

1.5 V @ I= 3 A

Over-temperature protection

Over-voltage protection

Over-current protection

ON/OFF external control by means of a TTL signal (Inhibit line)

Short circuit control

Load regulation: better than 1%

Remote sensing operation Requires large size return wire!

Output noise voltage: < 300 μV rms (10 Hz – 10 MHz)