Hybrid pixel developments for the ALICE Inner Tracking System upgrade

XVII SuperB Workshop and Kick Off meeting

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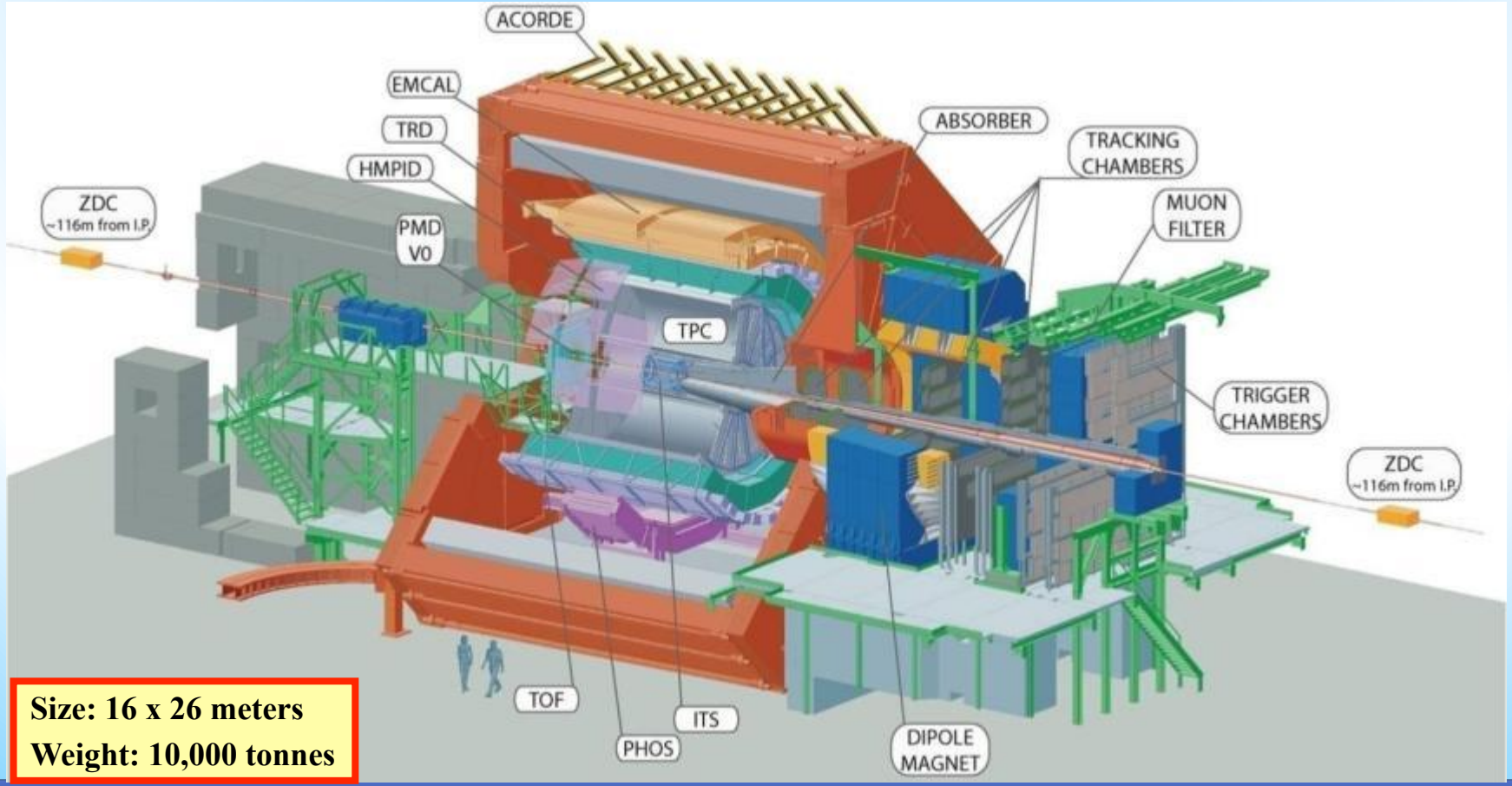
Outline

- Introduction
- ITS upgrade
- Hybrid Pixel R&D activities:
  - Thin planar sensor
  - Thin active edge planar sensor
  - Front-end chip thinning
  - Polyimide MicroChannel cooling
- Conclusions

The ALICE experiment

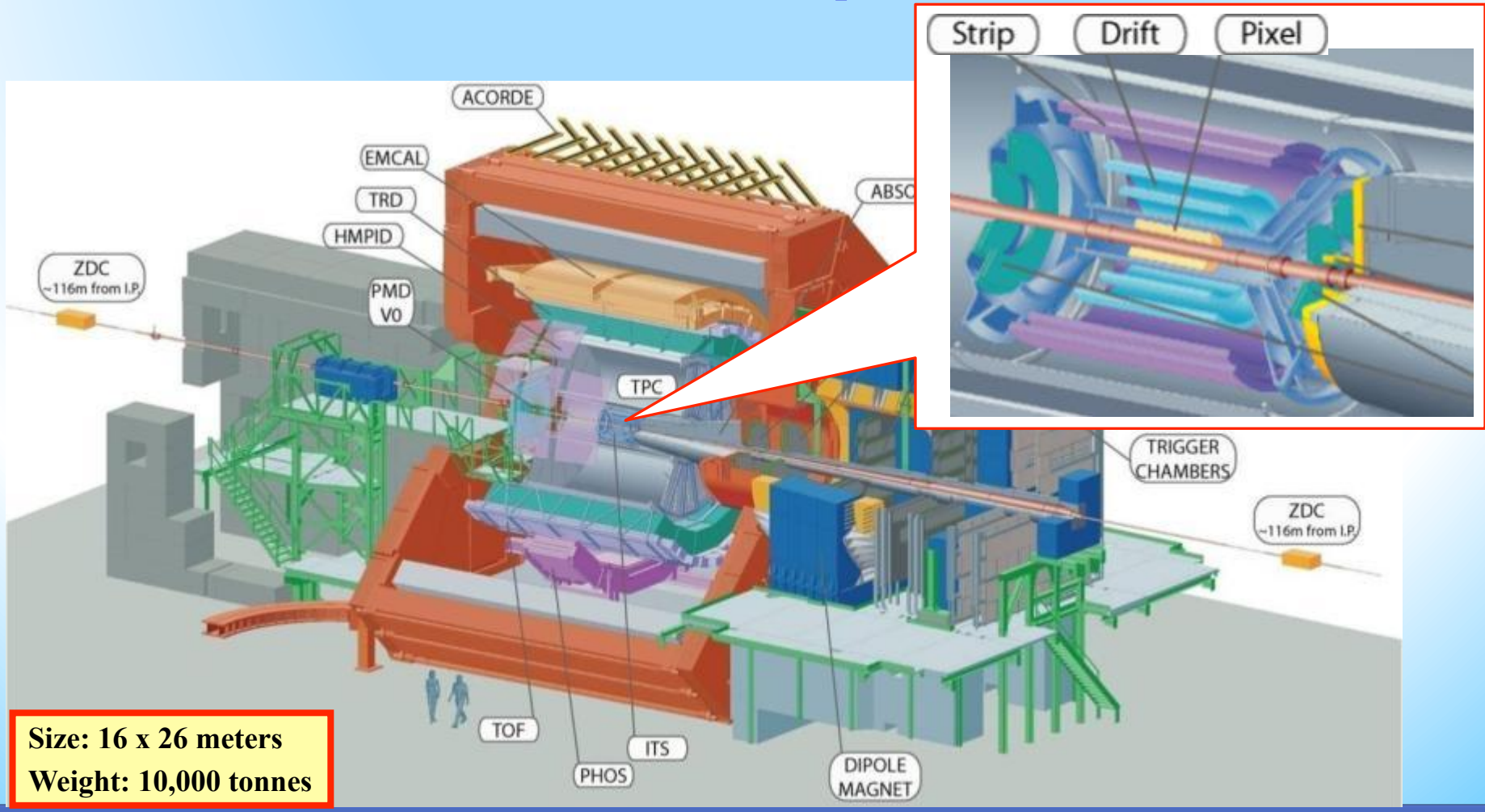
- **Ultra-relativistic nucleus-nucleus collisions**
  - study behavior of strongly interacting matter under extreme conditions of compression and heat
- **Proton-Proton collisions**
  - reference data for heavy-ion program
  - unique physics (momentum cutoff <100MeV/c, excellent PID, efficient minimum bias trigger)



Size: 16 x 26 meters
Weight: 10,000 tonnes

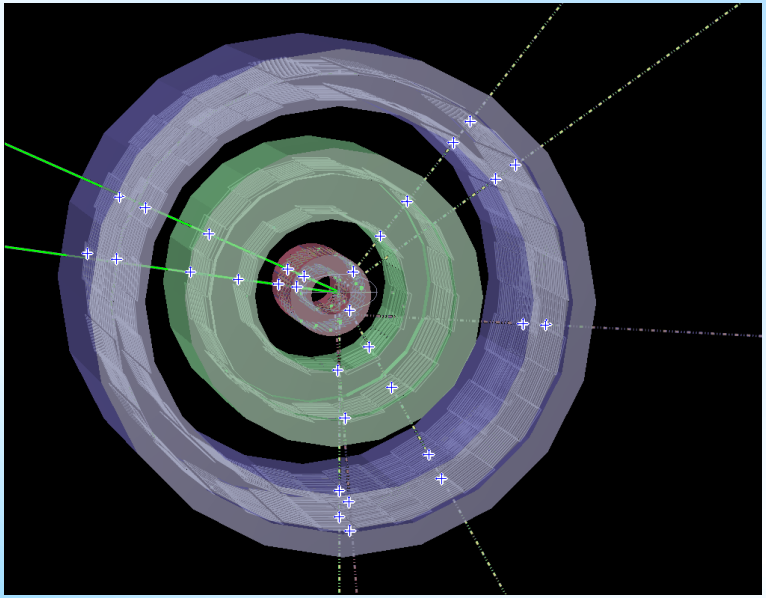
The ALICE Inner Tracking System

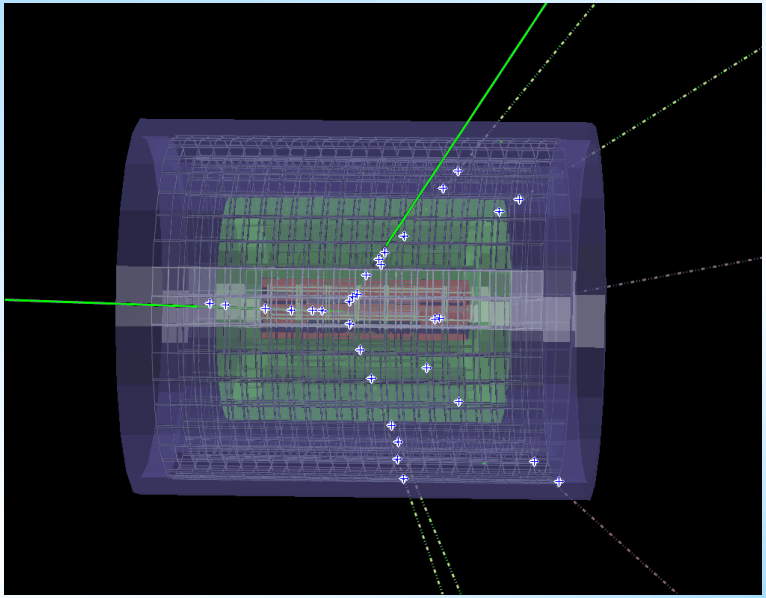
- **6-layer barrel**
- **3 different silicon detector technologies,** 2 layers each (inner → outer):
  - **Pixels (SPD), Drift (SDD), double-side Strips (SSD)**



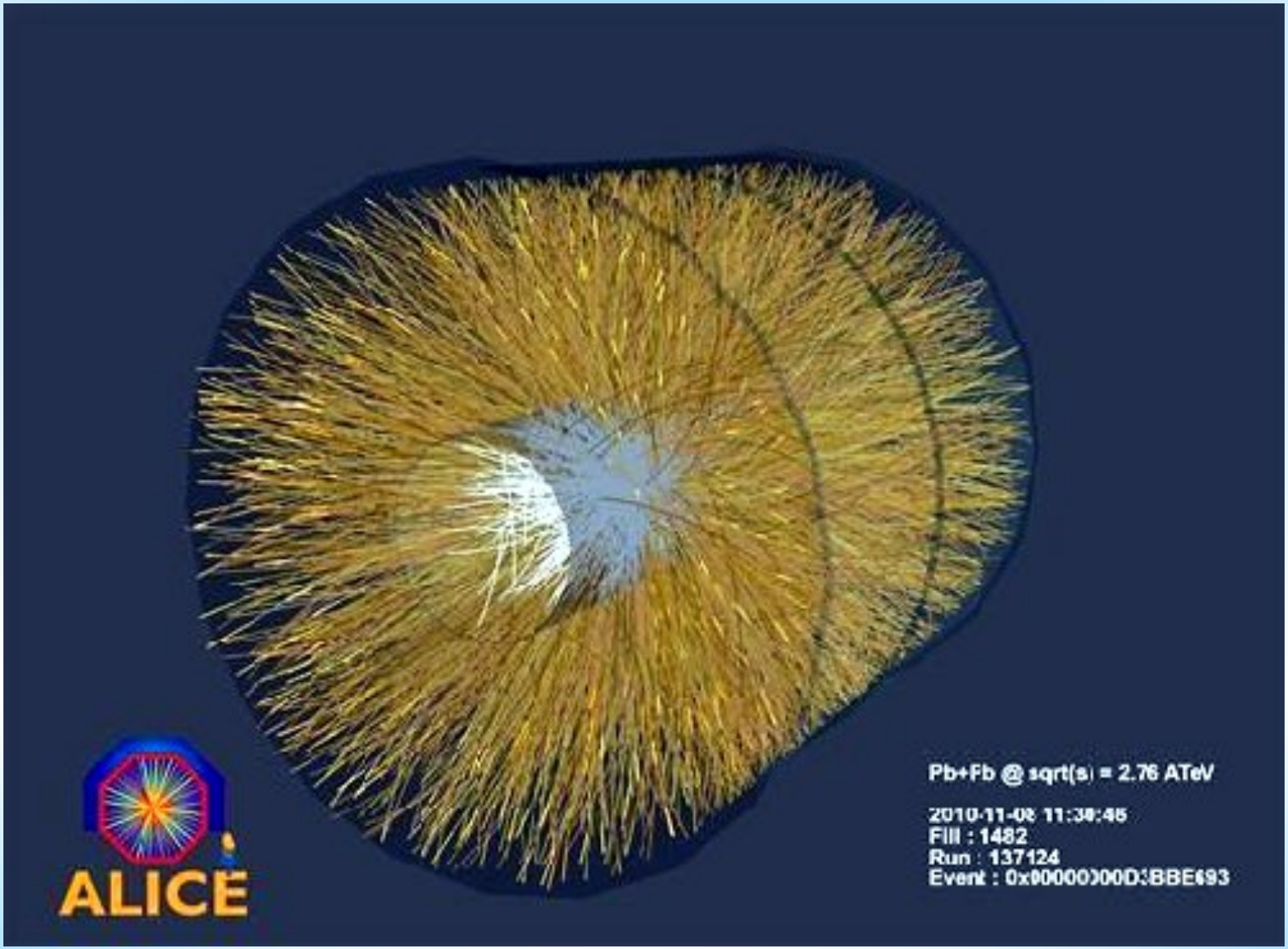
The ALICE Inner Tracking System

Layer	Det.	Radius (cm)	Length (cm)	Surface (m^2)	Chan.	Spatial precision (μm)		Cell (μm^2)	Max occupancy central PbPb (%)	Power dissipation (W)	
						rϕ	z			barrel	end-cap
1	SPD	3.9	28.2	0.21	9.8M	12	100	50x425	2.1	1.35k	30
2		7.6	28.2						0.6		
3	SDD	15.0	44.4	1.31	133K	35	25	202x294	2.5	1.06k	1.75k
4		23.9	59.4						1.0		
5	SSD	38.0	86.2	5.0	2.6M	20	830	95x40000	4.0	850	1.15k
6		43.0	97.8						3.3		





Pb-Pb event


ALICE
Pb+Pb @ sqrt(s) = 2.76 ATeV
2010-11-08 11:38:45
Fill : 1482
Run : 137124
Event : 0x00000000D3BBE693

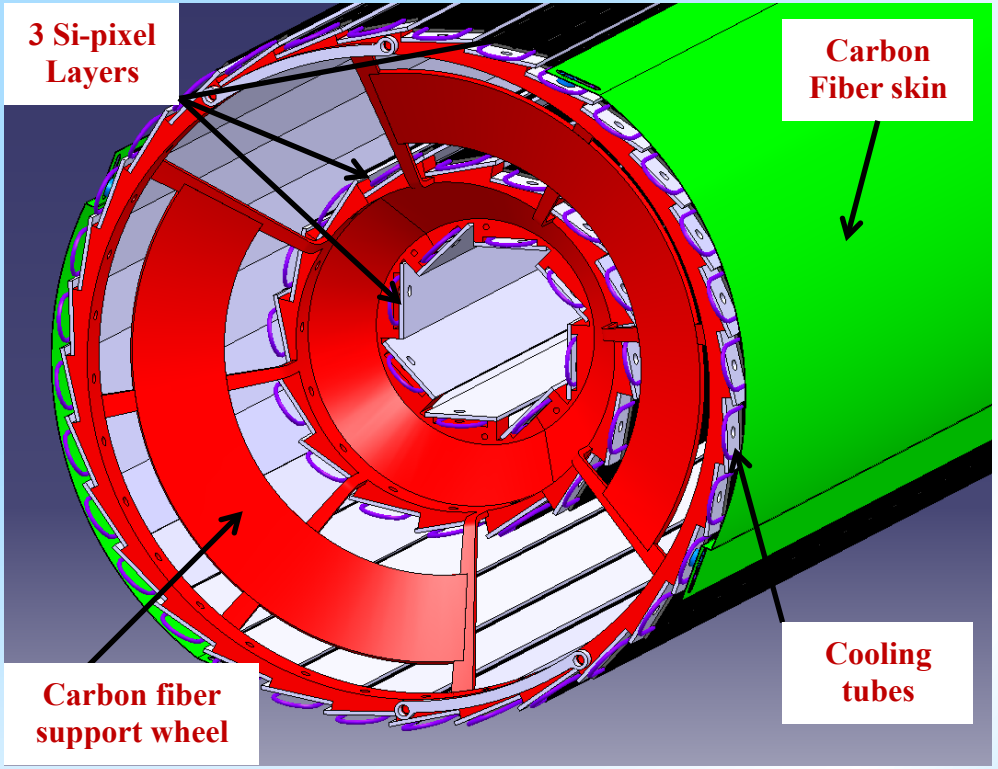
ALICE ITS Upgrade

- ***Aims to extend the ALICE physics capabilities for the identification of short-lived particles containing heavy quarks through reconstruction and identification of the displaced vertex at mid-rapidity and enlarge the acceptance to larger rapidity***

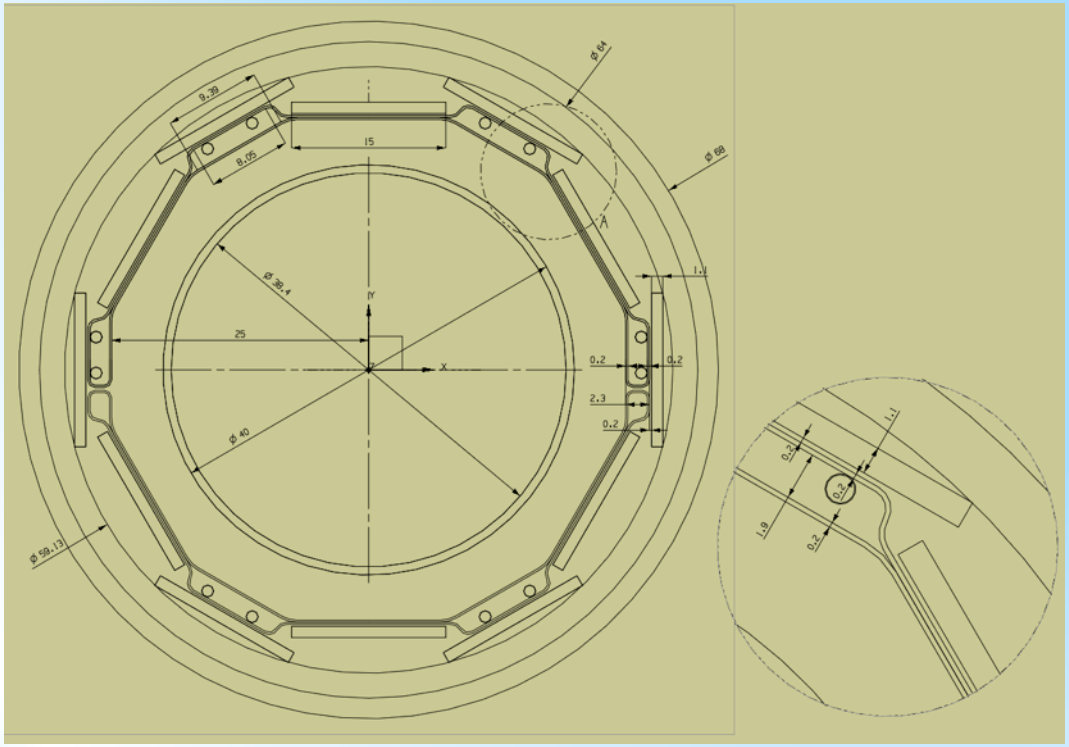
- Improve the impact parameter resolution to ≈50 μm up to very low p_T
  - ① Get closer to the Interaction Point
    - ✓ Radius of the innermost PIXEL layer < 25mm (at present 39mm)
      - reduce beam pipe radius to 20mm (at present 29mm)
  - ② Reduce material budget, especially innermost layers (at present ≈1.1% X_0)
    - ✓ Reduce mass of silicon, power and signals bus, cooling, mechanics
    - ✓ Monolithic Pixels
  - ③ Reduce pixel size, mainly for medium/high p_T (at present 50μm x 425μm)
- Improve standalone tracking and PID capabilities
- Improve readout and trigger capabilities
- Acceptance at Forward and Backward rapidity
- Exchange/replacement capability and spatial mapping

Basic idea of the Pixel Barrel

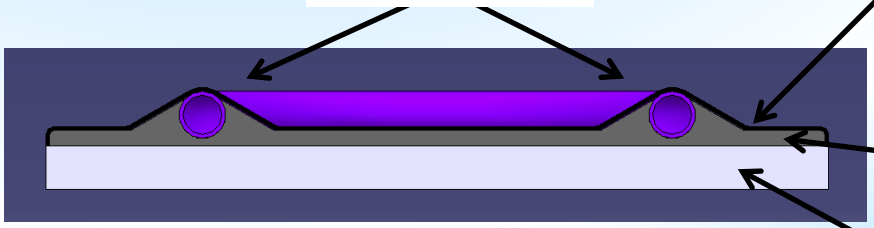
- 3 layers of Si-pixel detectors
- As close as possible to the interaction
  - beam pipe radius = 20mm
  - innermost average radius = 23mm
- Low material budget (< 0.5% X_0)
- Acceptance $|\eta| = 1$
- Power consumption < 0.5 W/cm^2
  - several cooling options
- All services from one side
  - fast extraction (winter shutdown) for fixing



Basic idea of the Pixel Barrel



Innermost layer cross-section



Single module cross-section

Pixel Detector R&D

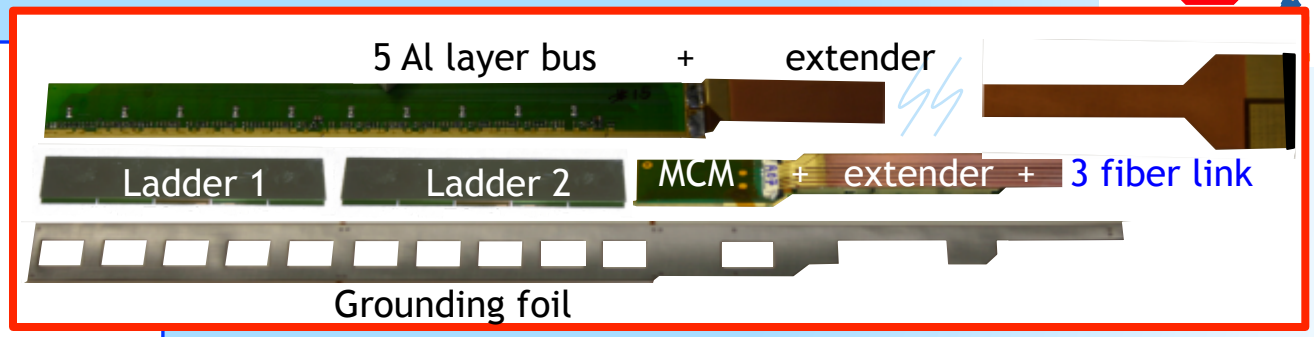
- Two main technologies are being evaluated for the Pixel Barrel:

  - **Monolithic pixel detectors**
    - MIMOSA, INMAPS, LePix
    - Lower material budget and larger area (low cost)
      - ✓ radiation tolerance and readout speed to be evaluated

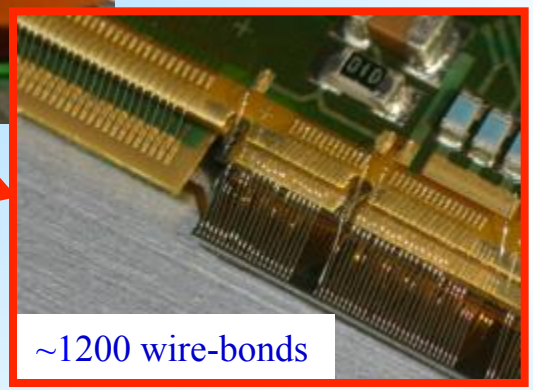
  - **Hybrid pixel detectors**
    - "State-of-the-art" of pixel detectors at LHC
    - R&D
      - ✓ Material budget
        - thinning of the silicon substrates: sensor and front-end chip
        - reduce overlaps between modules: active edge, 3D
        - multilayer flex and cooling
      - ✓ Low cost bump-bonding
      - ✓ Low power FEE chip

ALICE Pixel Overview

- ✓ 2 layer barrel
- ✓ Total surface: ~0.24m^2
- ✓ Power consumption ~1.5kW
- ✓ Evaporative cooling C_4F_{10}
- ✓ Room temperature
- ✓ Material budget per layer ~1% X_0

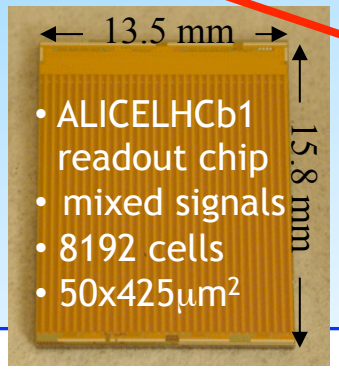


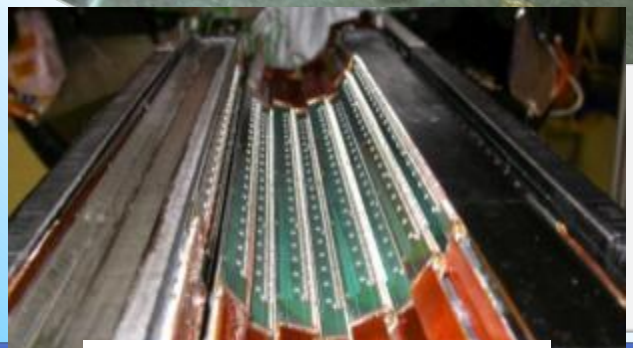
Half-stave



~1200 wire-bonds

Outer surface: 80 half-staves



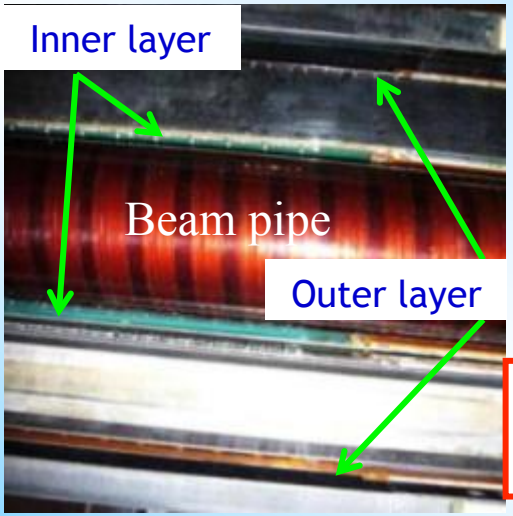


Inner surface: 40 half-staves

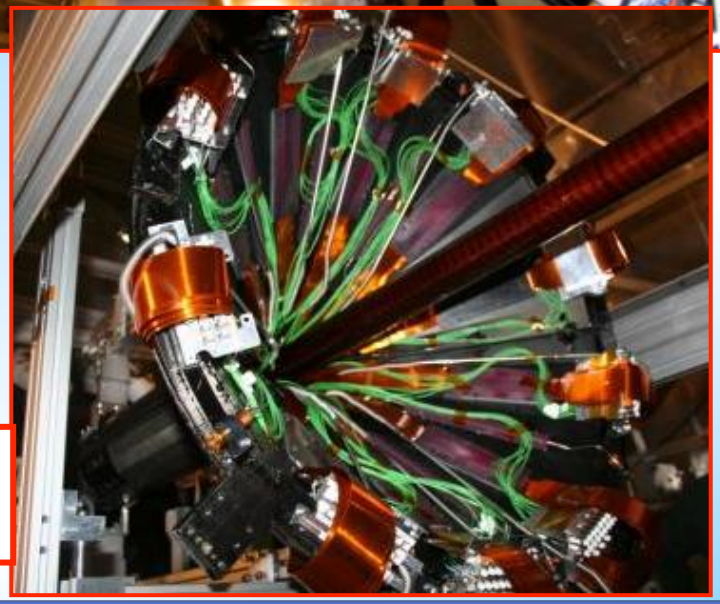
- ➢ **Unique L0 trigger capability**
  - Prompt FastOR signal in each chip
  - Extract and *synchronize* 1200 FastOR signals from the 120 half-staves
  - User defined programmable algorithms

ALICE Pixel Overview

- The Silicon Pixel Detector was installed in ALICE in Jun'07

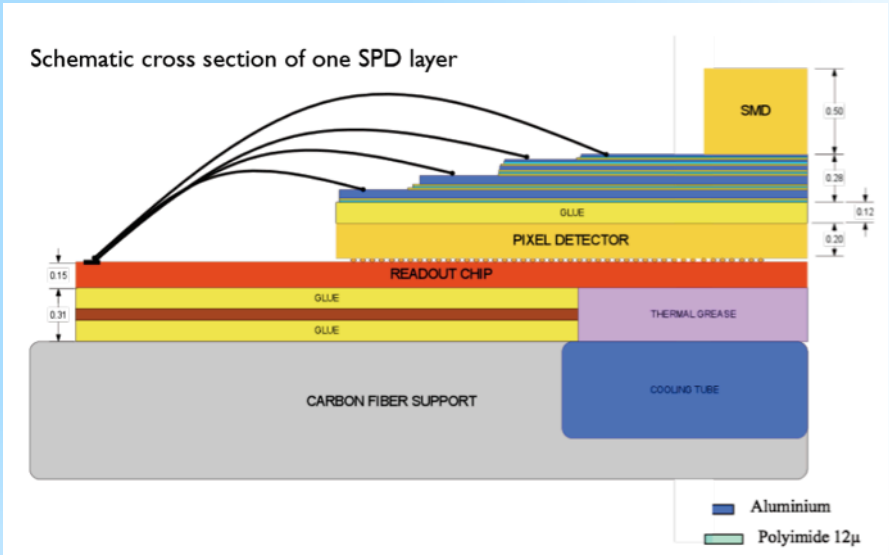


Minimum distance inner layer-beam pipe ≈5 mm



ALICE Pixel Material Budget

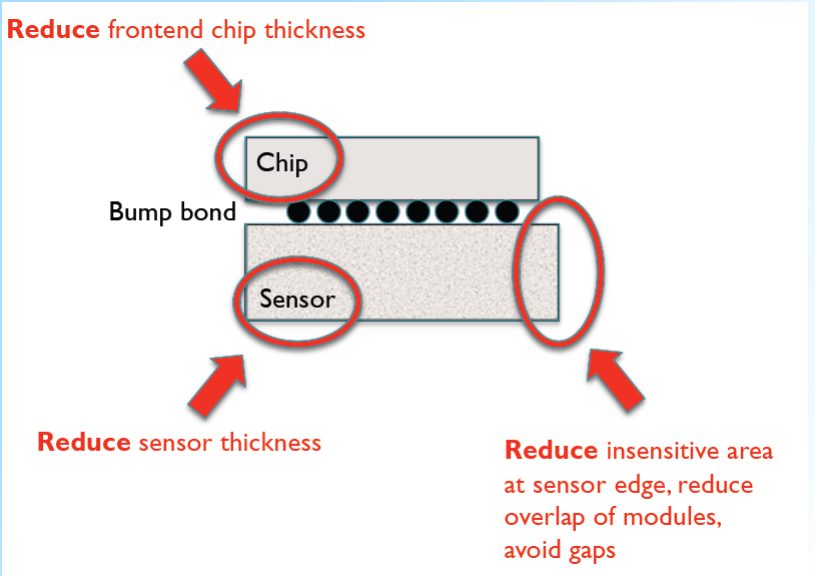
- Contributions to one current Pixel layer
  - Carbon fiber support: 200 μm
  - Cooling tube (Phynox): 40 μm wall thickness
  - Grounding foil (Al-Kapton): 75 μm
  - Silicon pixel chip: 150 μm ➡ 0.16% X_0
  - Bump bonds (Pb-Sn): diameter ~15-20 μm
  - Silicon sensor: 200 μm ➡ 0.22% X_0
  - Multilayer Al/Kapton pixel bus: 280 μm ➡ 0.48% X_0
  - SMD components
  - Glue (Eccobond 45) and thermal grease



Two main contributors: silicon and multilayer flex (pixel bus)

Hybrid Pixel R&D: Material Budget

- How can the material budget be reduced?
  - Reduce silicon front-end chip thickness
  - Reduce silicon sensor thickness
  - Reduce interconnect bus contribution
    - reduce power
  - Reduce edge dead regions on sensor
    - reduce overlaps to avoid gaps
  - Review also other components
    - average contribution ~0.02%



- What can be a reasonable target
  - **Hybrid pixels overall material budget: 0.5 % X_0**
    - ✓ **silicon: 0.16% X_0 overall** (100μm sensor + 50μm front end chip), at present 0.38%
    - ✓ bus: 0.24% X_0, at present 0.48%
    - ✓ others: 0.1% X_0 overall, at present 0.24%
  - Monolithic pixels: 0.3÷0.4% X_0 (e.g. STAR HFT)

Hybrid Pixel R&D: Material Budget

- **To reduce the silicon contribution to the overall material budget**
  Threefold activity
  - Thin Planar Sensor based on the current ALICE layout
    - ✓ bump-bonded to present ALICE front-end chip for testing
  - Thin Planar Active Edge Sensor based on the current ALICE layout
    - ✓ bump-bonded to present ALICE front-end chip for testing
  - Thinning the existing ALICE front-end chip
    - ✓ Bump-bonded to standard ALICE sensor 200 μm thick for testing
  - And then combine them

Hybrid Pixel R&D: Thin Planar Sensor

- Procurement, Processing and Handling of ≈100μm thick wafers is an issue

- Alternative:

  Epitaxial Wafers to be thinned during the bump-bonding process

  - Epitaxial wafers provide a mean to use very thin sensor wafers

    ☞ carrier wafer "included for free"

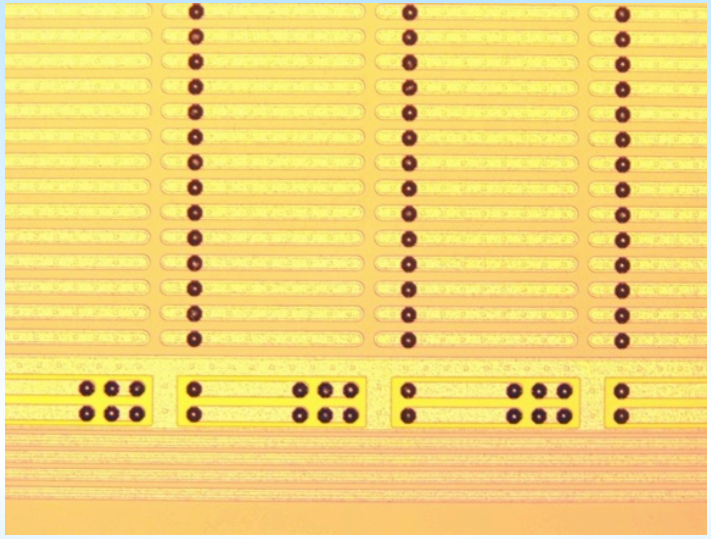
  - First tests of epitaxial sensors by PANDA (D. Calvo et al.) [*see NIM A 595(2008)*]

- **ALICE Epi-Pixel sensor**

  - Goal: achieve a sensor thickness of 100 μm (~ 0.11% X_0)
  - Test with the ALICE pixel front-end chip (optimized for 200μm sensor)
  - Epitaxial wafers produced by ITME (Poland)
    - Substrate thickness 525μm, doping n/Sb, resistivity 0.008-0.02 Ωcm, <111>
    - Epitaxial layer thickness 95-105μm, doping n/P, resistivity 2000±100 Ωcm

ALICE Epi-Pixel Sensor

- 5 sensor wafers fabricated at FBK
- 3 wafers processed at VTT
  - successfully through all process steps, including thinning and back side patterning
  - Overall thickness: 105-115 μm (i.e. epi layer + ≈10 μm)
- 5 singles flip-chip bonded to the current ALICE pixel front-end chip
  - electrical tests: ~30 nA at 20V at RT, min. threshold ~ 1500 el., ~30 missing pixels



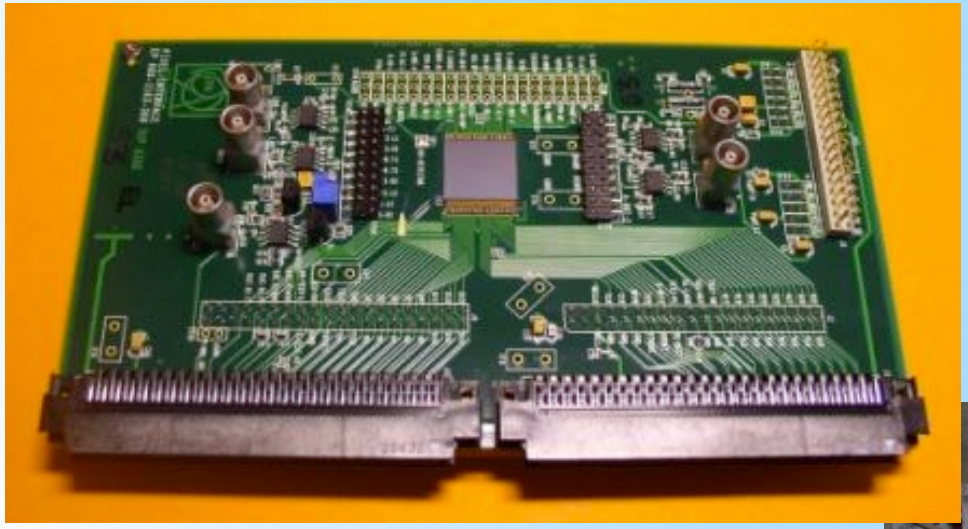
Beam Test of Epi-Pixel detector

- Beam test of ALICE Epi-Pixel detector
  - November 2010
  - CERN SPS: positive beam (pions, protons), 350 GeV/c, up to 10^4 particles/spill
  - Duty cicle 49s, Flat top ≈ 9s, Trigger rate ≈3KHz
  - ALICE 3D-Pixel detector samples were also tested
    - Double-sided Double-Type Column (DDTC) from FBK multi-project wafer

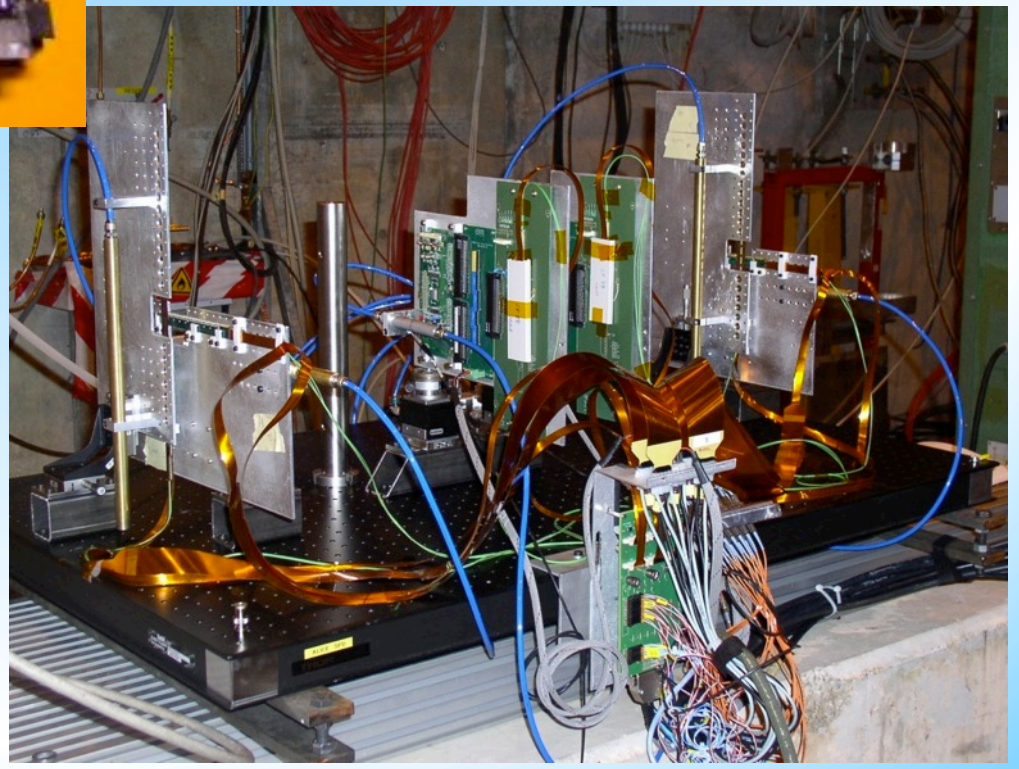
- Tracking Telescope
  - 4 ALICE standard Pixel detector arranged in 2 stations
    - each station contains 2 pixel detectors arranged in cross-geometry
      - ✓ pixel cell dimensions 50 x 425 μm^2
    - Estimated tracking precision ≈10μm both in x and y directions

- Trigger
  - Self-triggering: FastOr logic combining the information from the tracking planes

Beam Test Set-up



Single assembly mounted on test card



SPS beam test set-up

Beam Test Measurements

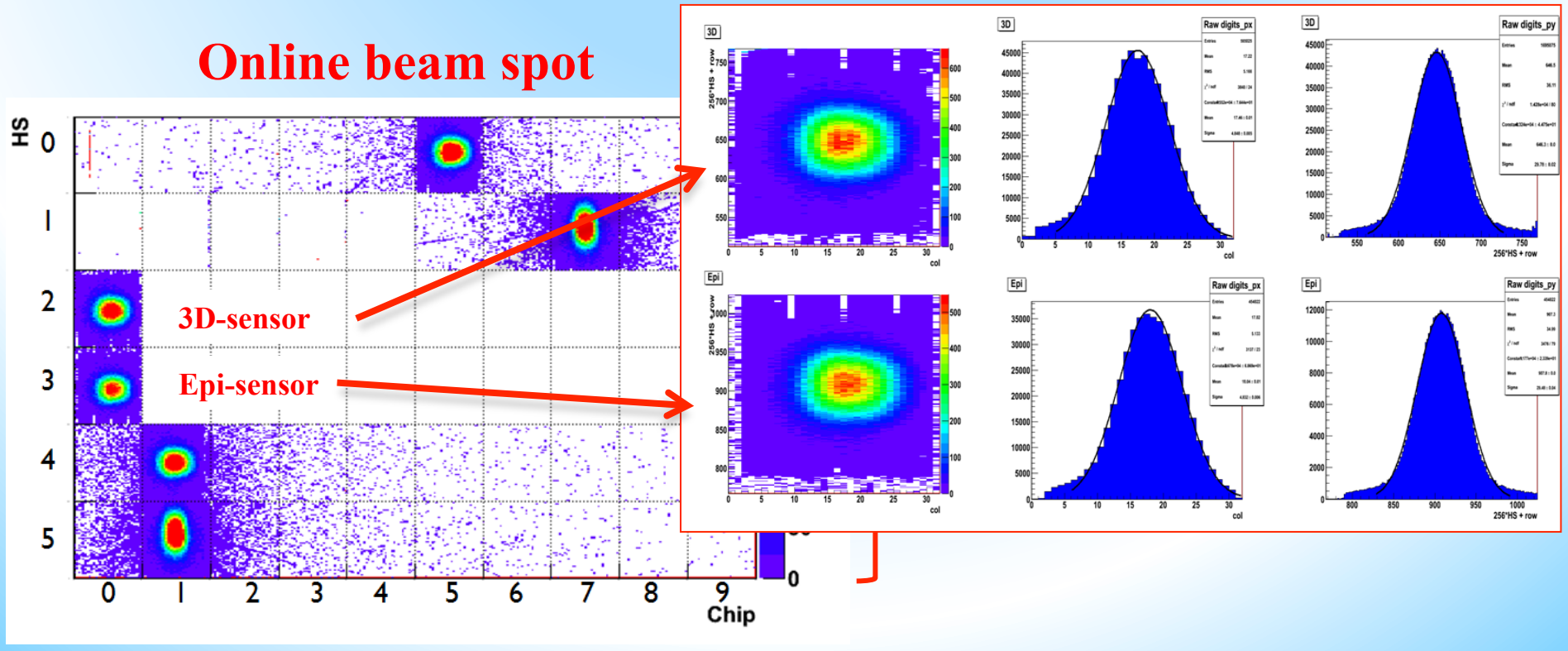
Objectives

- Track Efficiency
- Cluster size
- Space accuracy

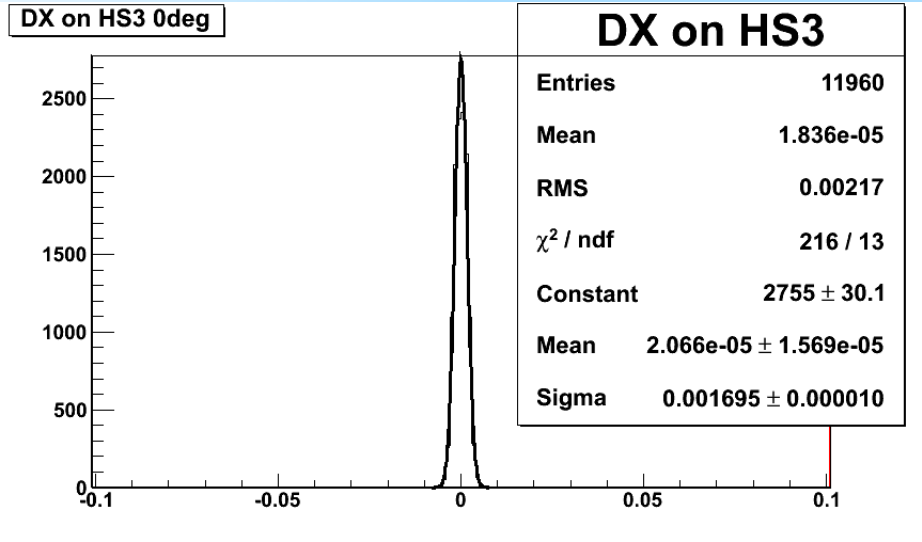
VS

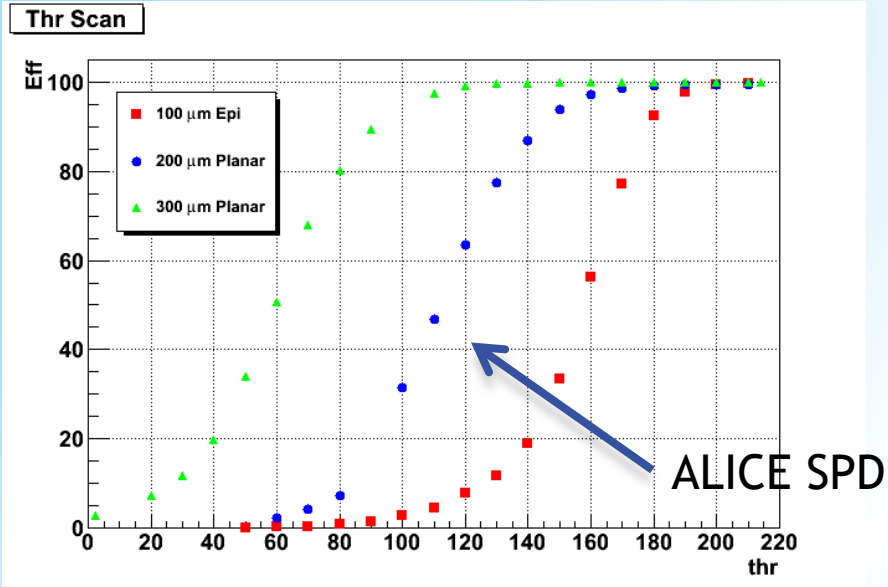
- Depletion Voltage
- Threshold
- Particle Crossing Angle

Online beam spot



Residuals and Efficiency



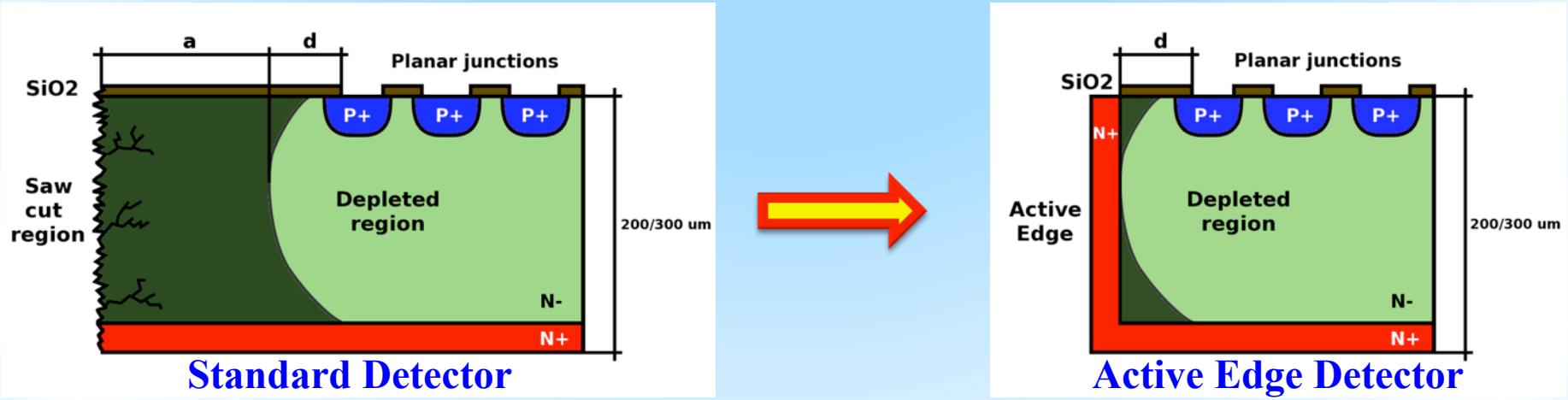


- *NIM paper in preparation*

Thr (DAC)	Thr (el.)
200	3000
190	3600
180	4200
170	4800

Planar Pixel Sensor with Active Edge

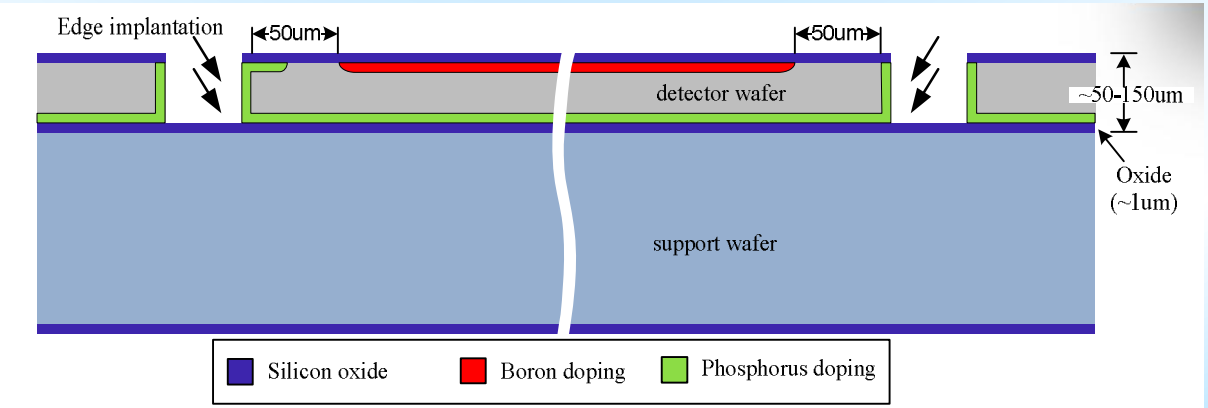
- **Standard detectors**
  - Dead region (cracks and damages) **a + d ≥ 500 µm**
- **Active edge to limit dead region**
  - Cut lines not sawed but etched with Deep Reactive Ion Etching (DRIE) and doped



- **R&D in collaboration with FBK**
  - Within the MEMS2 agreement FBK-INFN
  - Epitaxial wafer in order to achieve an Active Edge 100µm thick Planar Sensor

Active Edge Detector

- **Main process steps and critical issues**
  - Attach support wafer
    - ✓ provides mechanical support after trench etching (SOI, wafer bonding, …)
  - Trench opening by Deep Reactive Ion Etching (DRIE)
    - ✓ dimensional aspect ~1/20, deep etching (200-230 μm)
  - Inside trench doping
    - ✓ solid source technology
  - Trench filling with polysilicon
    - ✓ spin coating with standard photoresist is challenging due to trench
  - Remove devices from support wafers (after bumping in case of pixel sensors)



Active Edge Detector

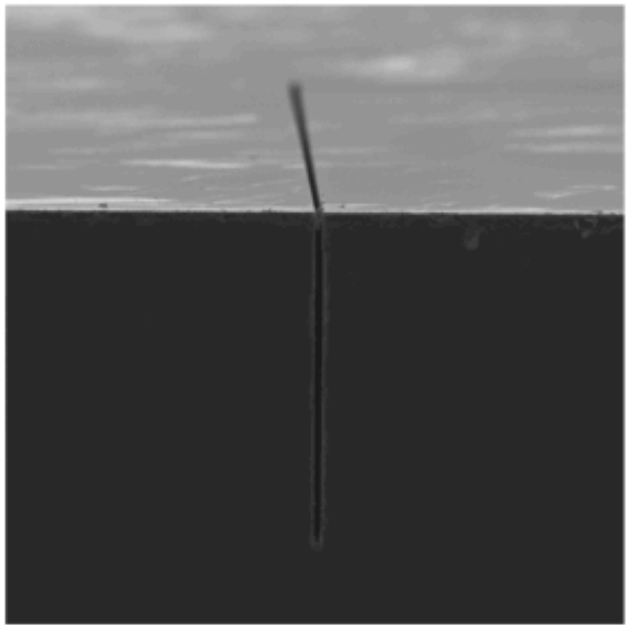
TRENCH DEFINITION AND ETCHING

M. Boscardin

Trench Etching

- DRIE process
- Depth:
  - ✓ Throughout the processed wafers, i.e. ~200 ÷ 250 µm
- Width:
  - ✓ ~5 µm
  - ✓ minimize the width of the trench to facilitate polysilicon filling

4,5µm wide
220µm deep



Capability to etch a trench more than 220micron deep and only 4,5micron wide

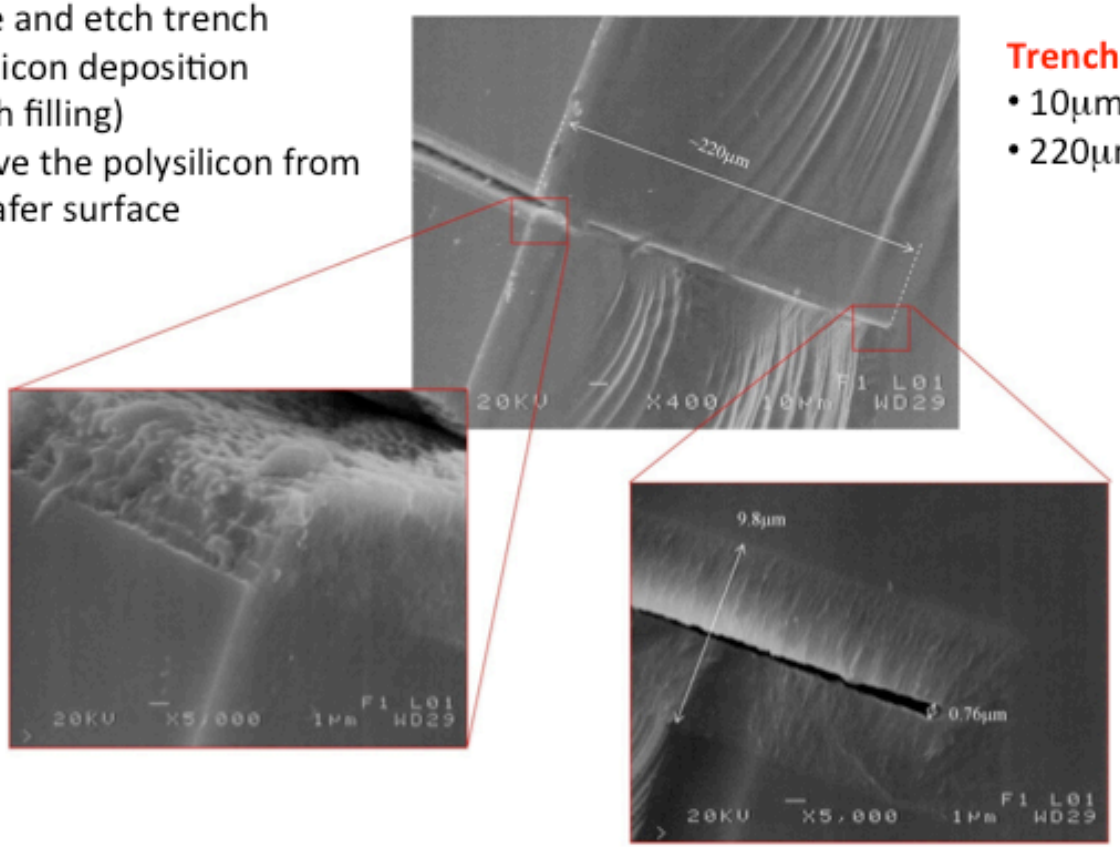
Active Edge Detector

TECHNOLOGY : POLYSILICON TRENCH FILLING

M. Boscardin

Process

- Define and etch trench
- Polysilicon deposition (trench filling)
- Remove the polysilicon from the wafer surface



Trench :

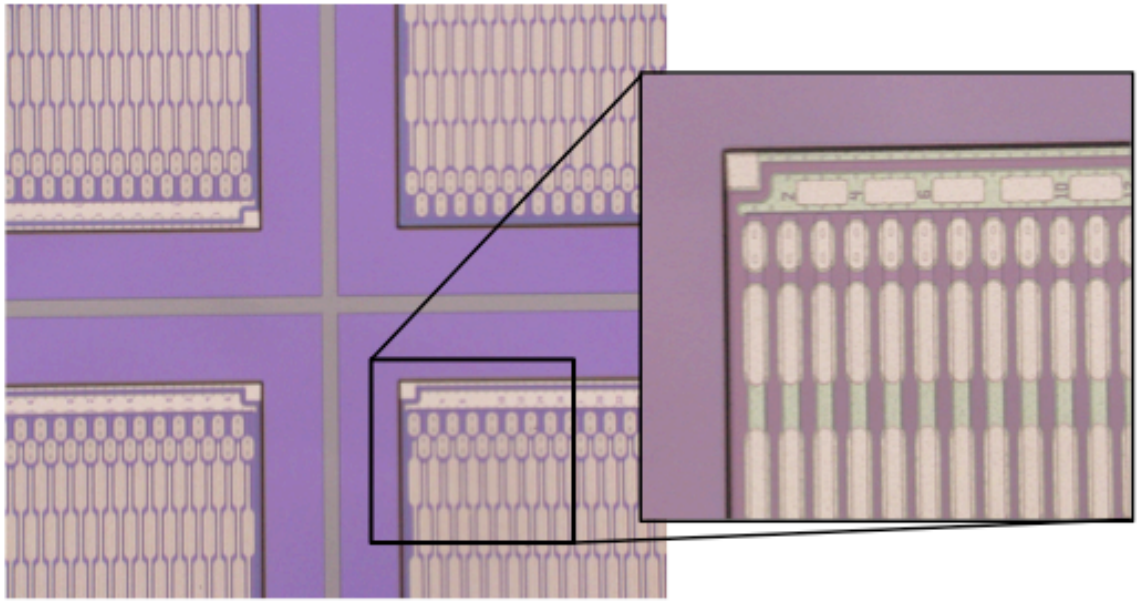
- 10µm wide
- 220µm deep

Active Edge Detector

First FBK batch on active edge tecnology:

M. Boscardin

First batch at FBK on active edge technology



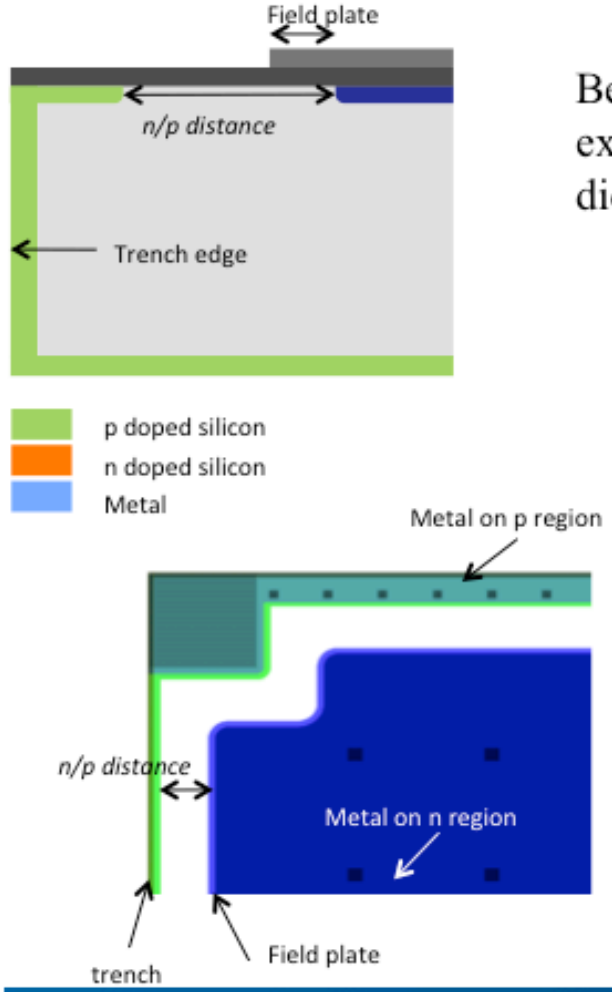
- For more infos see:

  "Development of planar detector with active edge" , M. Povoli et al. doi: 10.1016/j.nima.2011.04.050

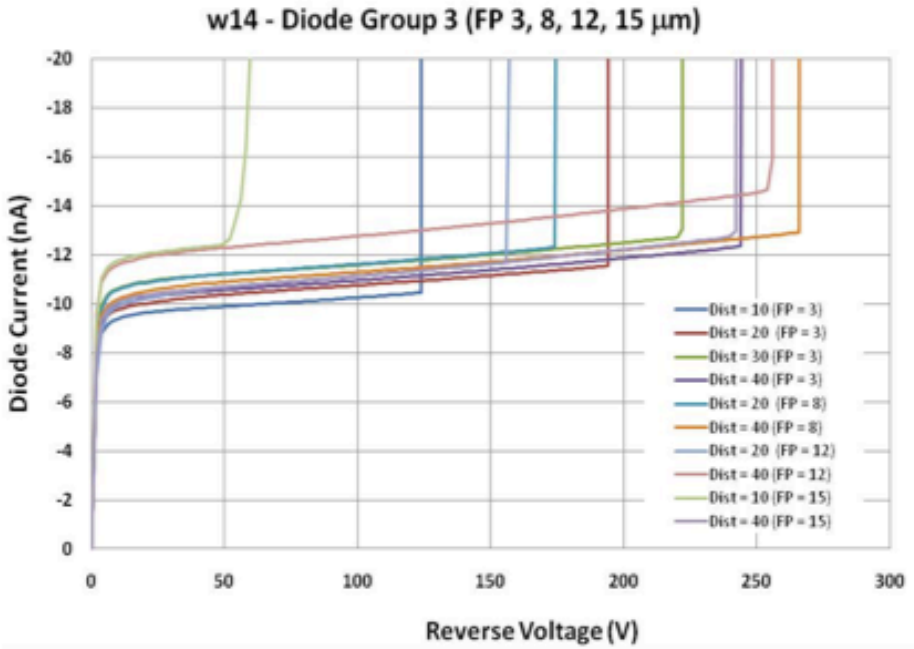
Active Edge Detector

First FBK batch on active edge tecnology

M. Boscardin



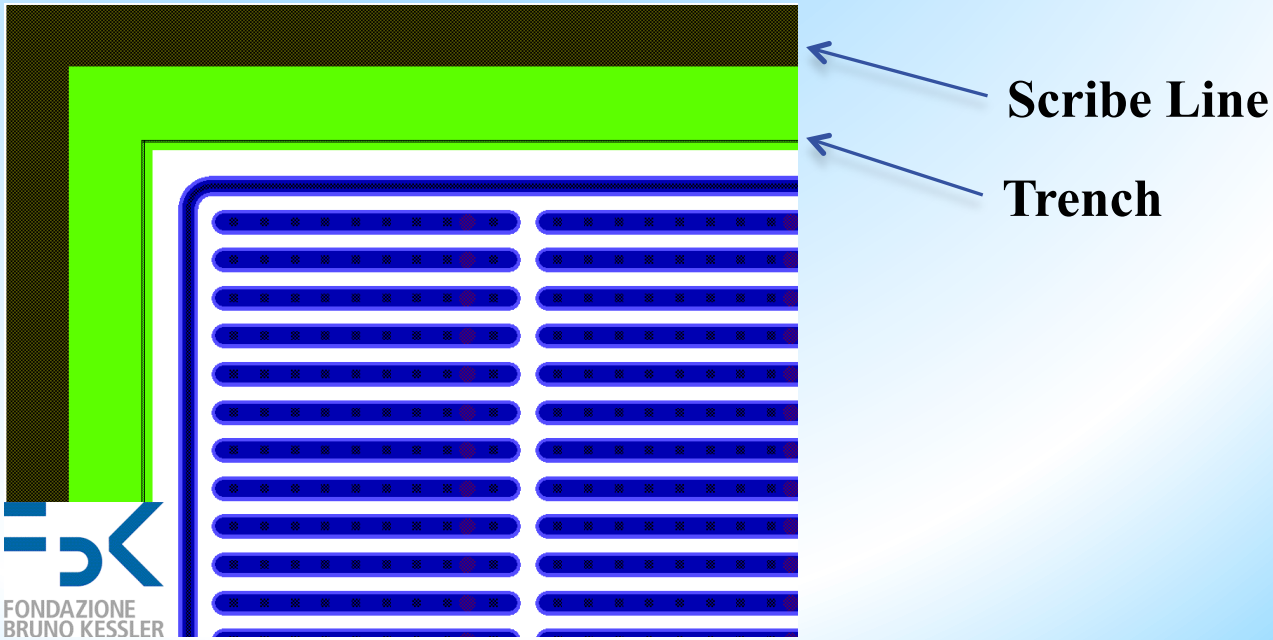
Behavior of I/V characteristic of trenched diode: as expected, the V_{bk} depends on the distance between diode and trench as well as the field plate spread



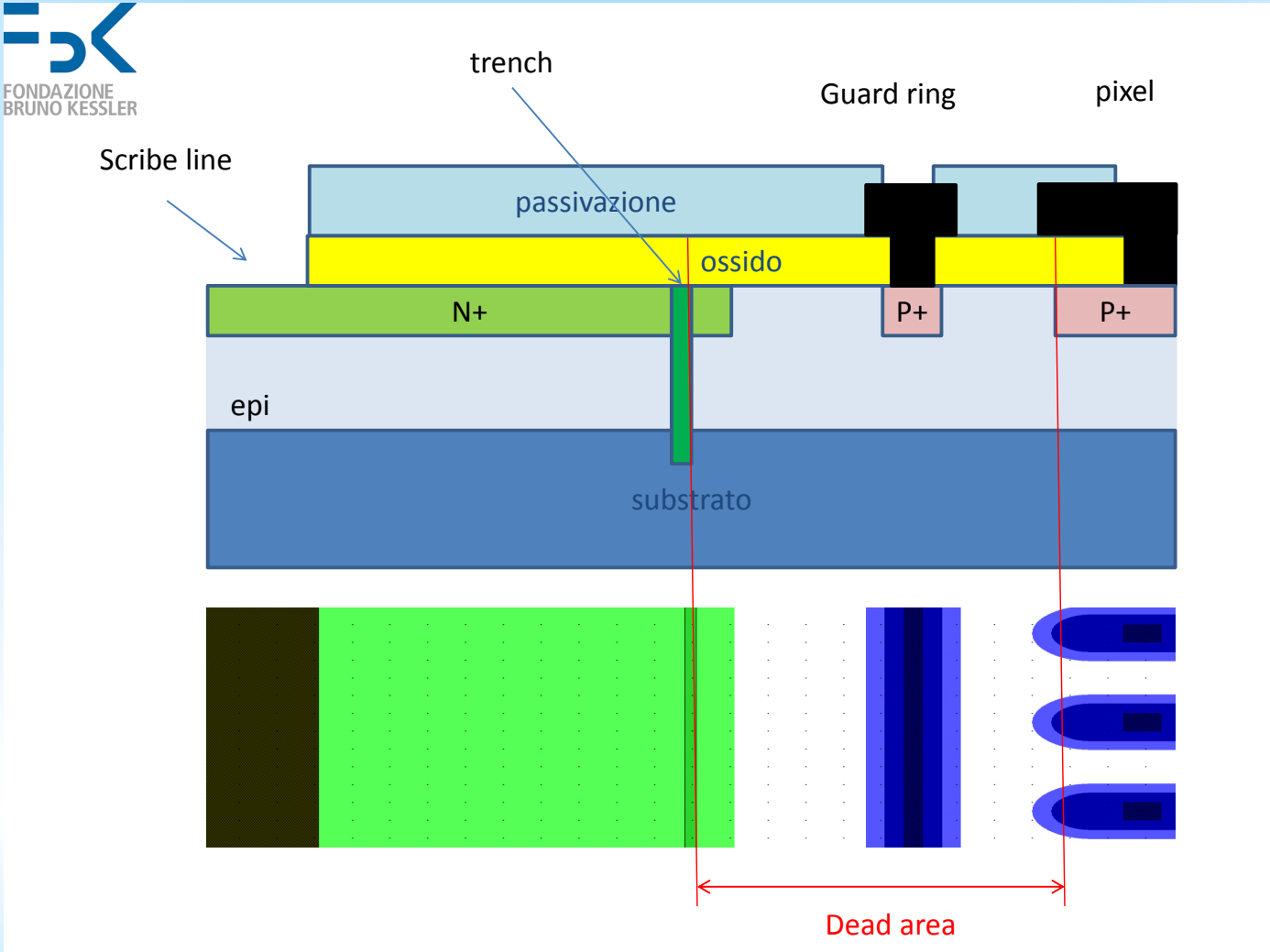
ALICE Pixel with Active Edge

- Recall ALICE Epi-Pixel detector
  - Planar pixel sensor on epitaxial high resistivity silicon wafer
    - ✓ Remove the bulk by back-grinding after the bumping to achieve a ~100 μm thick sensor

- Combine with the capability to etch a trench to achieve an **Active Edge Thin** pixel detector

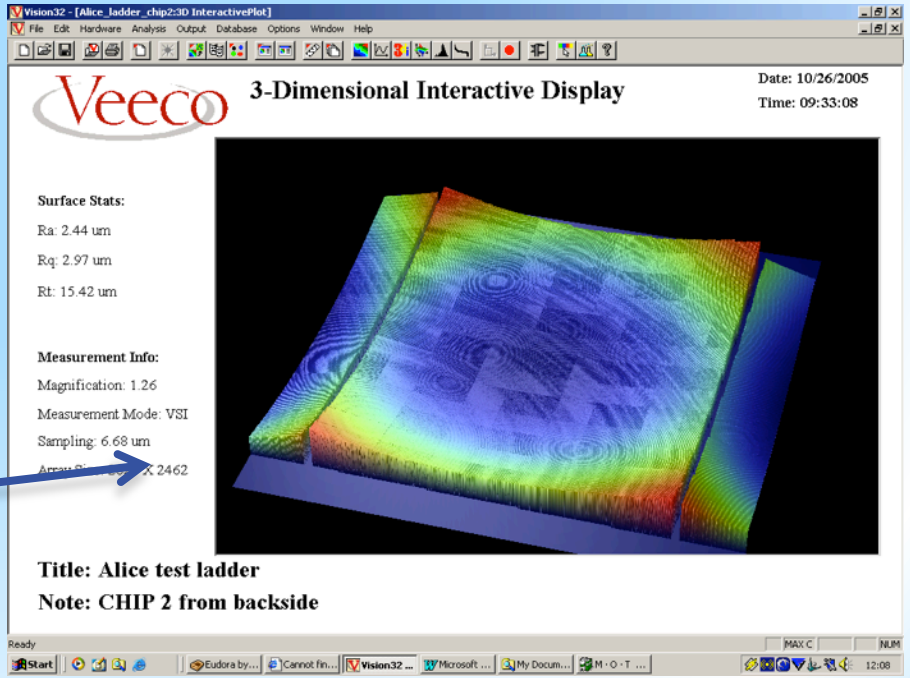


ALICE Pixel with Active Edge



Front-end Chip Thinning

- Current ALICE chips: 150 µm thinned during bump bonding process
- Thickness reduction will make inherent stresses come out stronger
- First experience during the ALICE production
- Thinning process needs to be well studied and tuned to produce coherent results



S. Vahanen, VTT

Front-end Chip Thinning R&D

➢ **Study using dummy components with IZM Berlin**

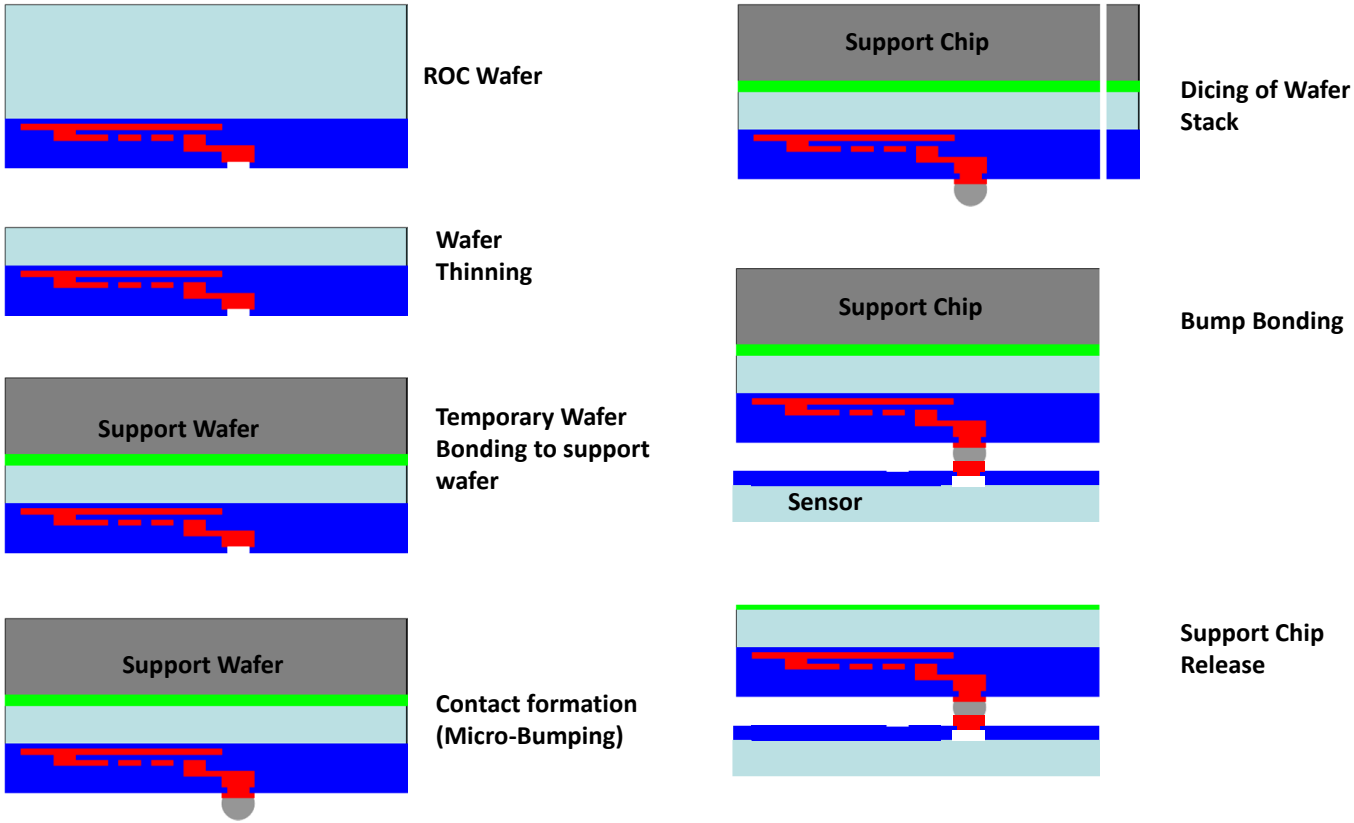
- Hybrid detector dummy components, i.e sensors and chips, based on ALICE layout
- Specific IZM process for thinning:
  - Glass support wafer during full process
  - Laser release of the support wafer
- Sensor wafers (200 μm) in processing, ASIC wafers ready in 4 weeks
- First components back by end July 2011

	Si sensor [μm]	X_0 [%]	ASIC [μm]	X_0 [%]	X_0 total [%]
First R&D step	200	0.22	50	0.05	0.27
R&D target	100	0.11	50	0.05	0.16

Front-end Chip Thinning R&D

Thin Chip Assembly – Temporary Support Approach

Process Flow



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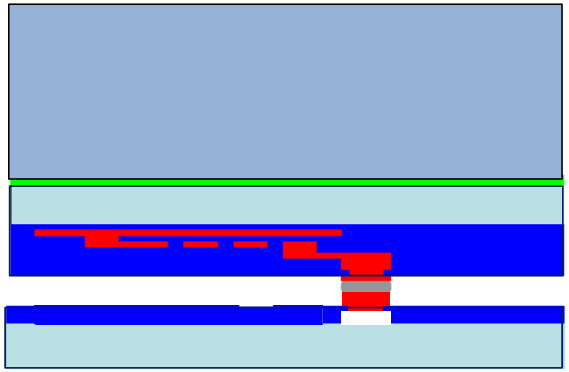
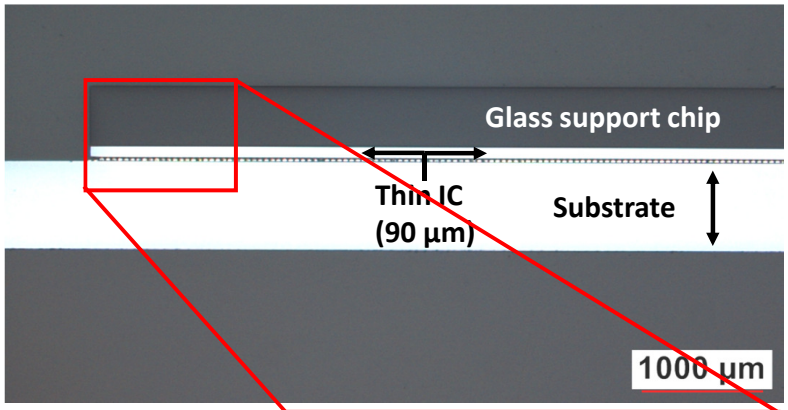
Thin Chip Assembly – Temporary Support Approach

Laser Debonding using UV-Release Glue

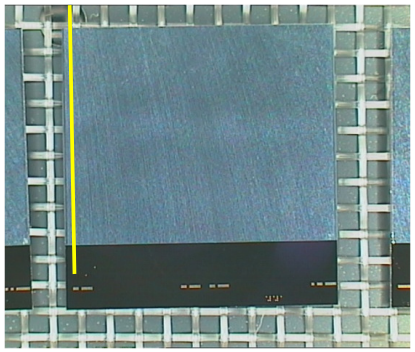
1. Step: Flip Chip Assembly of Chipstack

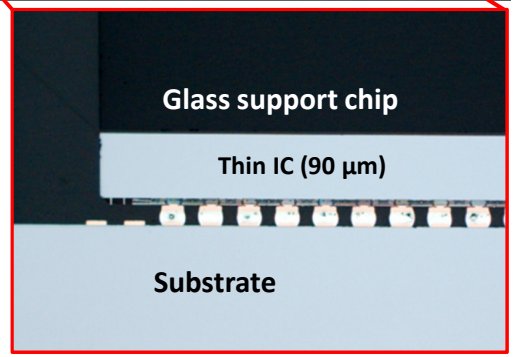




Left:
Chip after bump bonding
size 14x11 mm² (2x1 FE-I3)

Right:
Cross section of the first bump row
(yellow line)





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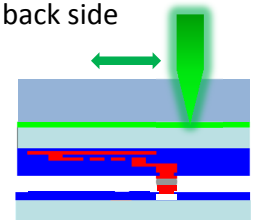
Thin Chip Assembly – Temporary Support Approach

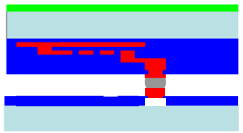
Laser Debonding using UV-Release Glue

2. Step: Support Chip Release

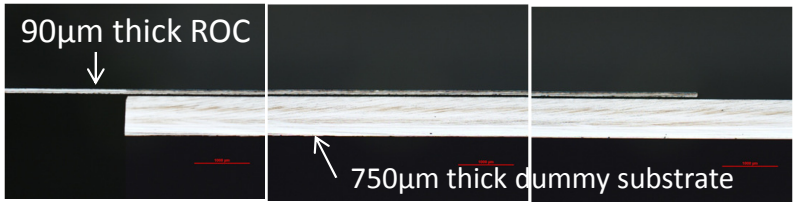
1. Laser scanning of back side

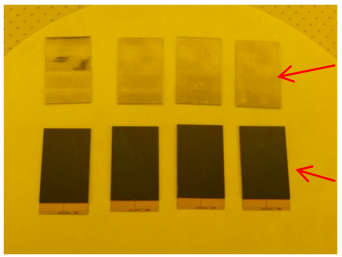


2. Carrier chip release



Side few on 14 x 11 cm² (Double ROC ATLAS FE-I2 reticle) dummy module after carrier chip release





Released glass carrier chip

Thin chip module (ROC side down)

14 x 22 cm² (Quad ROC ATLAS FE-I2 reticles) dummy modules after carrier chip release

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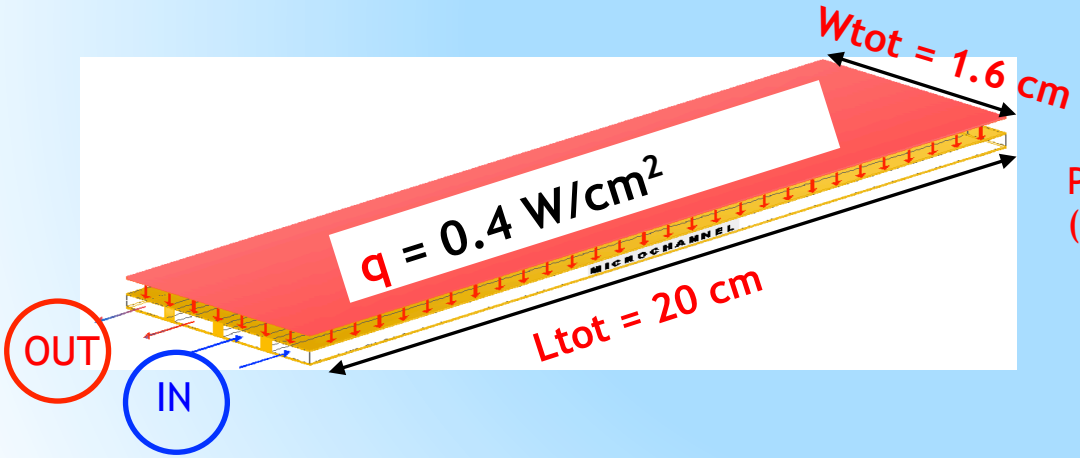
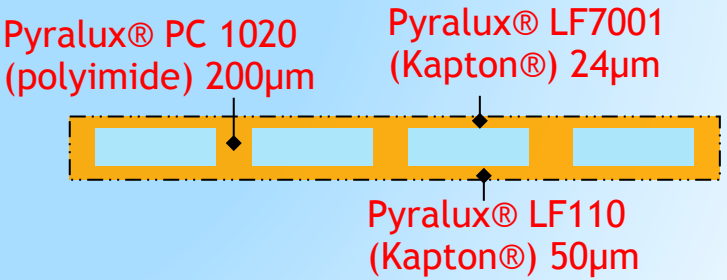
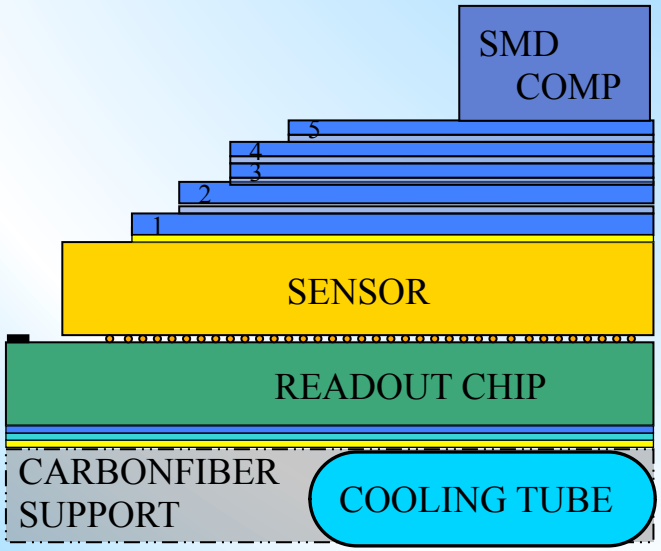
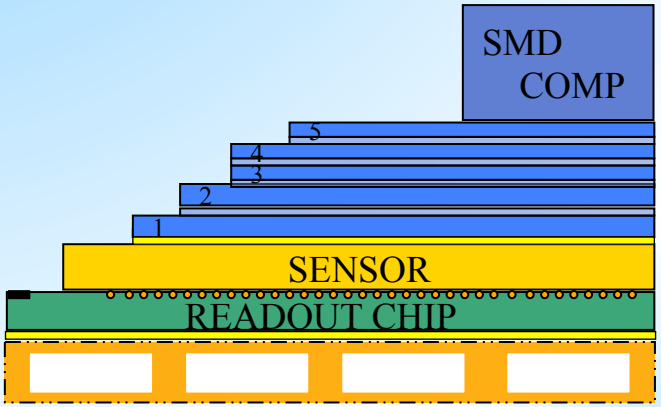
Polyimide MicroChannel cooling



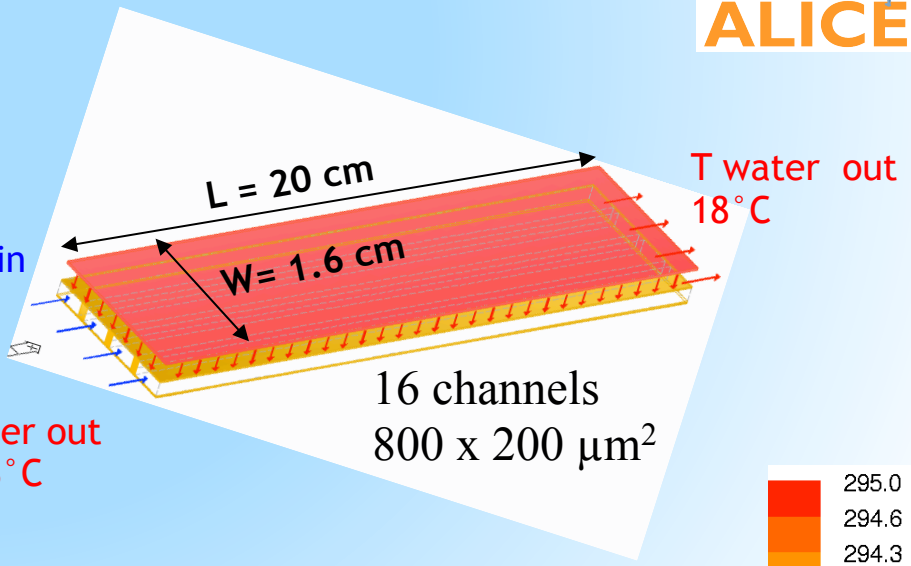






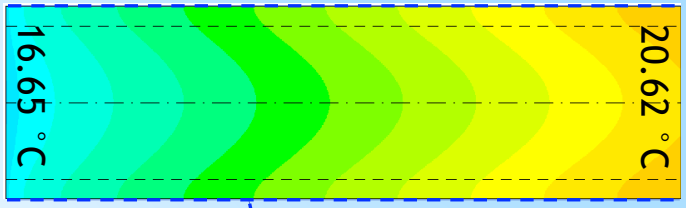
MicroChannel Simulation (Fluent 6.2)

- Assuming
  - $\Delta T_{max} = 3°C$
  - Leakless (underpressure) system



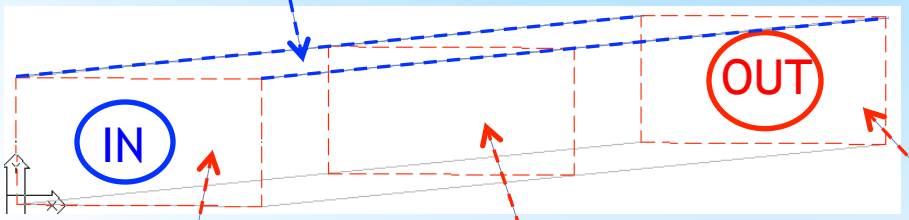
T water in
15°C

Top Layer

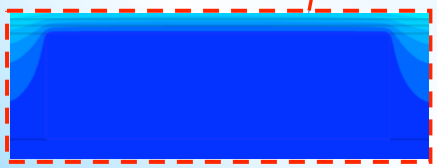


T water in
15°C

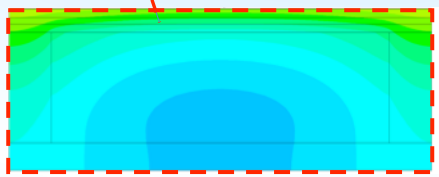
T water out
18°C



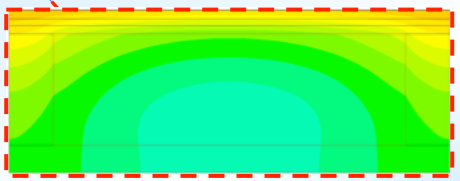
Axonometric view
of a single channel



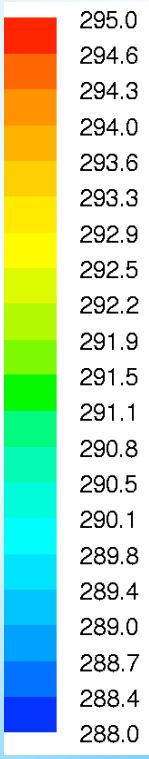
Inlet section



Middle section

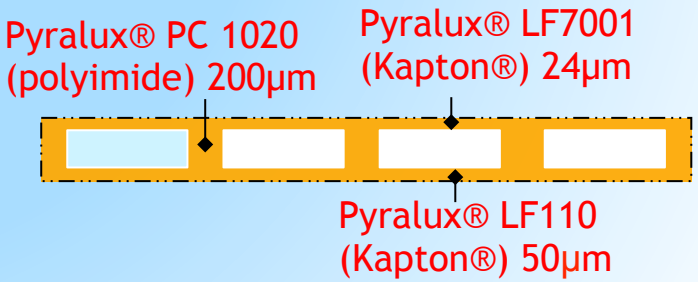


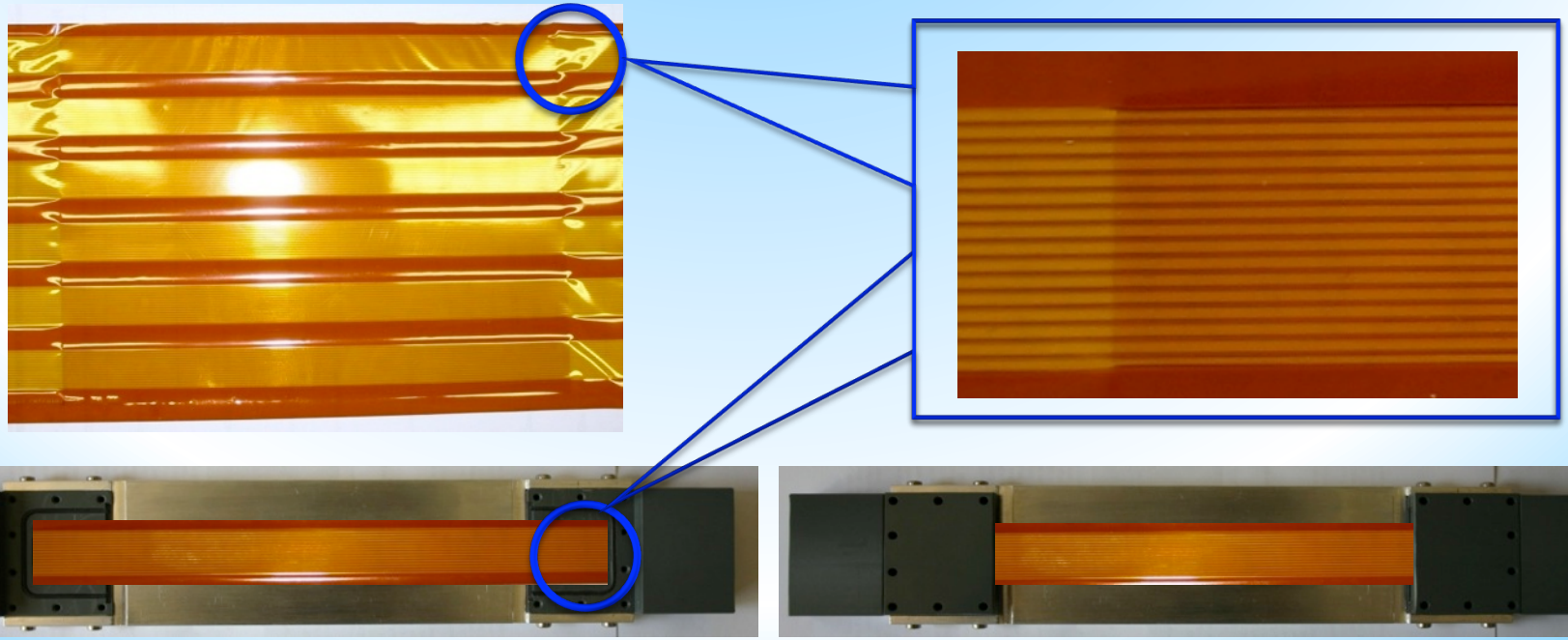
Outlet section



MicroChannel Production

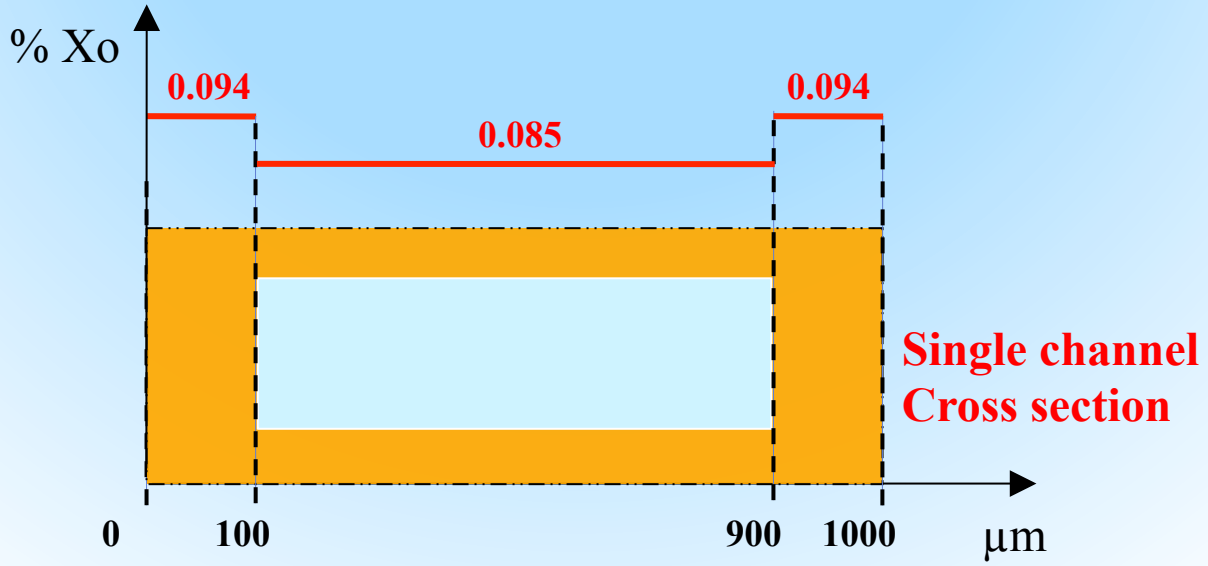
- **Main fabrication process steps (R. De Oliveira, CERN TM-MPE-EM)**
  - Sheet 50 µm of LF110
  - Lamination 200 µm photoimageable coverlay (4 layers of PC1020)
  - Creation of the grooves (800 x 200 µm^2) by photolithography process @ 180°C
  - Gluing by hot pressing the LF7001 24 µm lid
  - cured @ 180°C for 10h





MicroChannel Material Budget

Material	Radiation length [cm]
Kapton	28.6
H_2O	36.1



- Material budget of the ALICE Pixel cooling (Phynox tube + C4F10) ≈ O.8 % X_0

Conclusions

- The ITS upgrade aims to increase the ALICE sensitivity to heavy flavour by improving the impact parameter resolution
- Both Monolithic and Hybrid Pixels are being considered for the upgrade
- At present, for the innermost layers the hybrid option seems to be preferable compared to the monolithic for radiation hardness
- A very light (≤ 0.5 % X_0) pixel detector is necessary
- R&D activities ongoing:
  - thin active edge planar sensor
  - front-end chip thinning
  - polyimide microchannel cooling

Timeline

- The upgrade should target the Phase I (2017-18) shutdown
  - ✓ The scope of the upgrade Phase I should be well tailored to what can be reasonably prepared and tested within the next five years and installed in 15 months.
  - ✓ The full upgrade program might require a two step approach with a partial upgrade in Phase I and the completion in Phase II (2020 and beyond)
- Decisions on upgrade plans in terms of physics strategy, detector feasibility, funding availability, should be taken in 2011
  - ✓ Expression of Interest: ready
  - ✓ Preparation of a technical proposal till summer 2011
  - ✓ R&D for Phase I: 2010-2014
  - ✓ Production and pre-commissioning for Phase I: 2014-2016
  - ✓ Installation and commissioning for Phase I: 2017