SuperB IFR electronics: overview

SuperB IFR electronics: overview

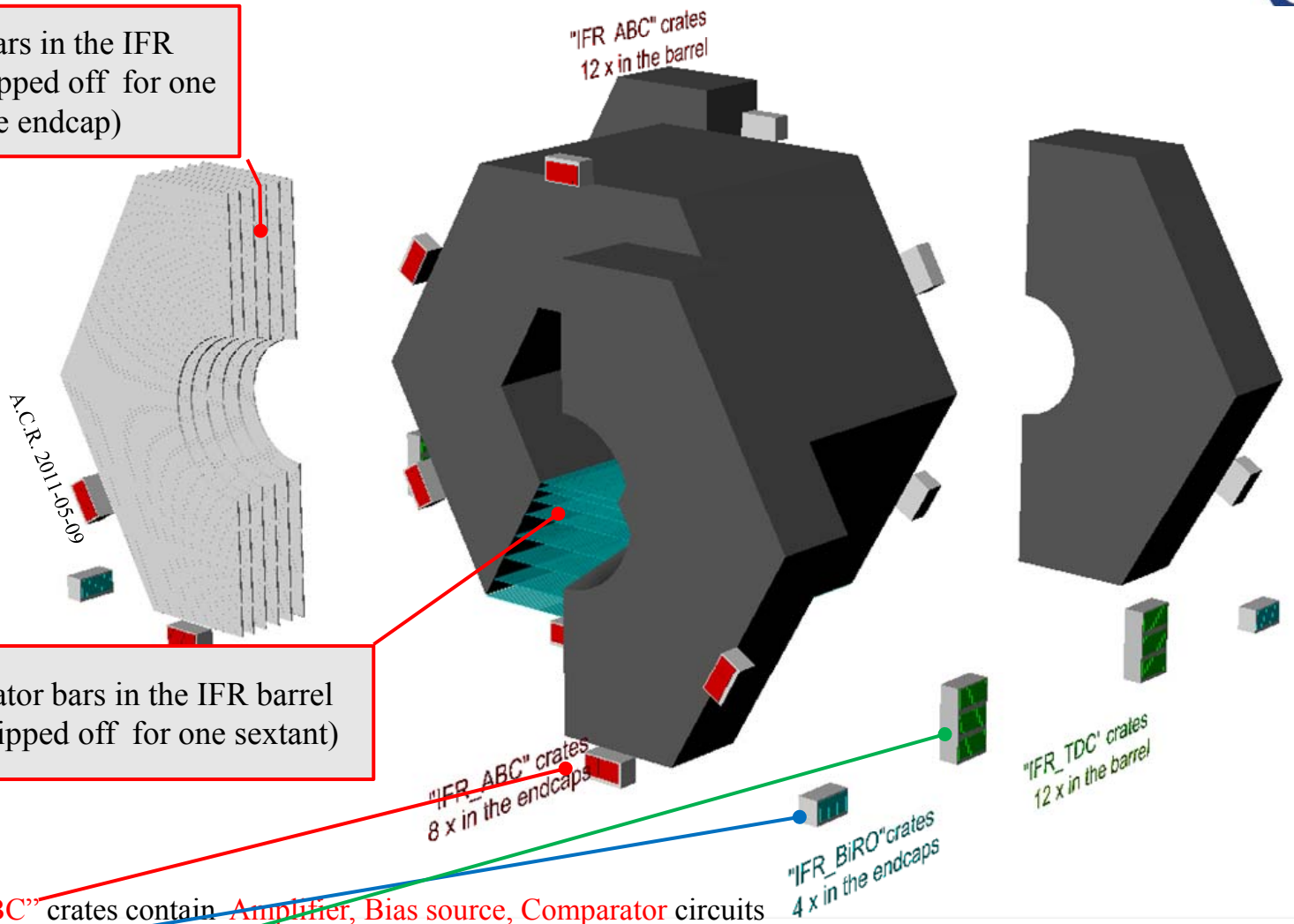
Outlook:

- Overview (for the new collaborators of the AGH University of Science and Technology in Krakow)
  - SiPM based IFR particle detectors
  - IFR small scale prototype as a proof of principle
  - the overall SuperB DAQ architecture
  - baseline design: IFR front end electronics
  - from baseline to final design: exploiting available SiPM readout ASICs
  - from baseline to final design : using FPGAs and design tecniques for radiation mitigation
- conclusions

- **APPENDIX A: schematic diagrams of some key parts of the "IFR_ABCD" board**
- **APPENDIX B: estimates of number of channels, hit rates, triggered data bandwidth**

SuperB IFR electronics: overview - SiPM based IFR particle detectors

Scintillator bars in the IFR endcap (iron stripped off for one half of the endcap)



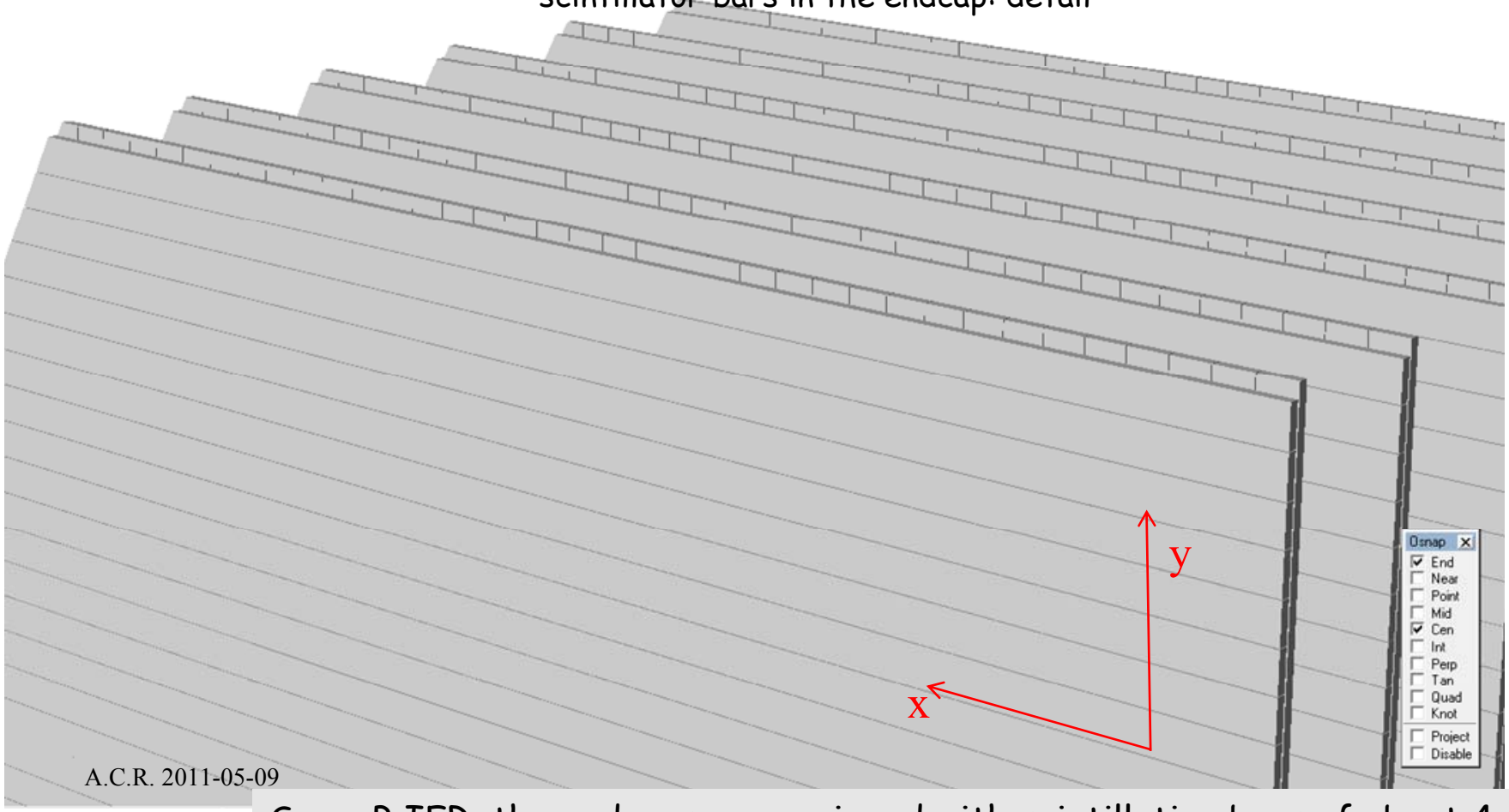
Scintillator bars in the IFR barrel (iron stripped off for one sextant)

Legenda:

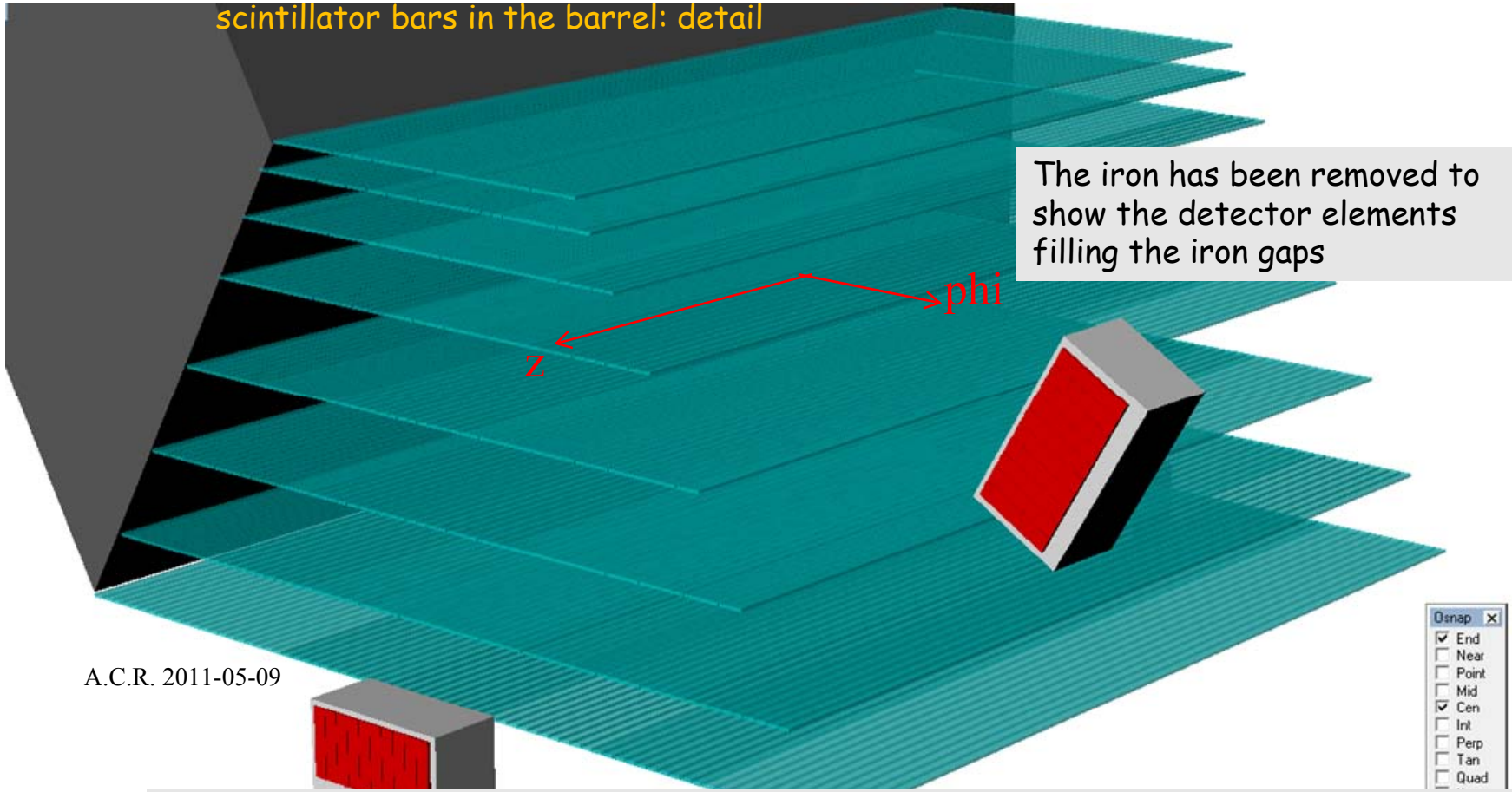
- "IFR_ABC" crates contain Amplifier, Bias source, Comparator circuits
- "IFR_BiRO" crates contain sampling circuits and buffer memories to Read Out the IFR_ABC cards in Binary mode
- "IFR_TDC" crates contain TDC circuits and buffer memories to readout the IFR_ABC cards in timing mode

In the baseline design the splitting of functions was meant to allow the digitizers and latency buffers to be positioned as far as possible away from the high radiation region of the detector and surroundings.

SuperB IFR electronics: overview - SiPM based IFR particle detectors
scintillator bars in the endcap: detail



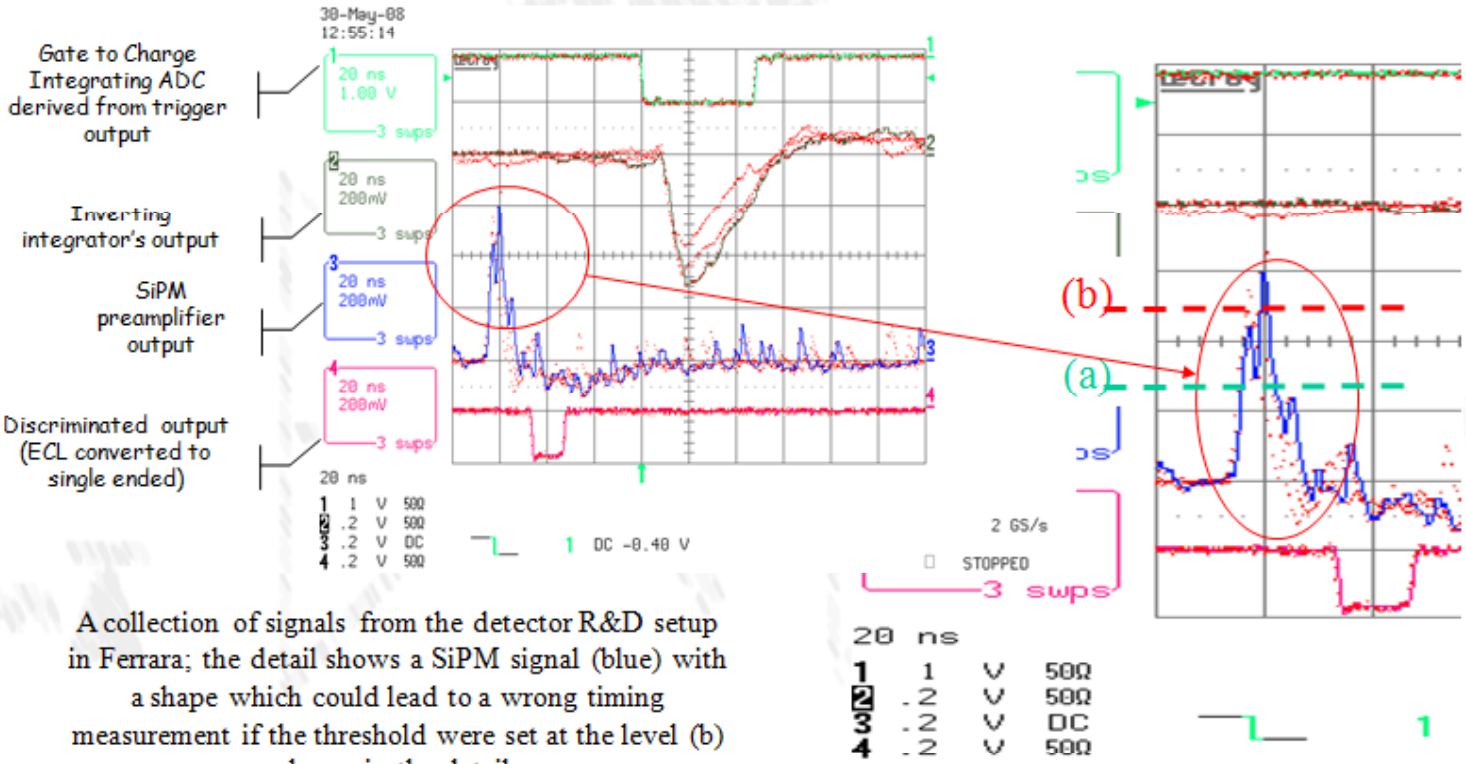
SuperB IFR: the endcaps are equipped with scintillating bars of about 4x1 cm^2 cross section which are assembled orthogonally and inserted in the iron gaps. Each bar is READ OUT BY SiPM AT ONLY ONE END.
The "hit" coordinates are found by simply recording the IDs of the two orthogonal bars producing a signal (the off line reconstruction will resolve ambiguities due to high multiplicity)



SuperB IFR (baseline design): in the barrel the scintillator bars are 4x2cm^2 in cross section and are only oriented in the Z direction. Each bar is READ OUT BY SiPM **AT BOTH ENDs**. The "hit" coordinates are found:
-in the PHI direction: by simply recording the ID of the scintillator bar producing a signal
-in the Z direction: by recording the times of arrival of the signals from the SiPM at each end of the detector bar. **The Z coordinate can then be determined off-line once the time zero of the event is known**

→ **...continues**

1) prototype of SiPM signal processing channel being used in detector R&D in Ferrara



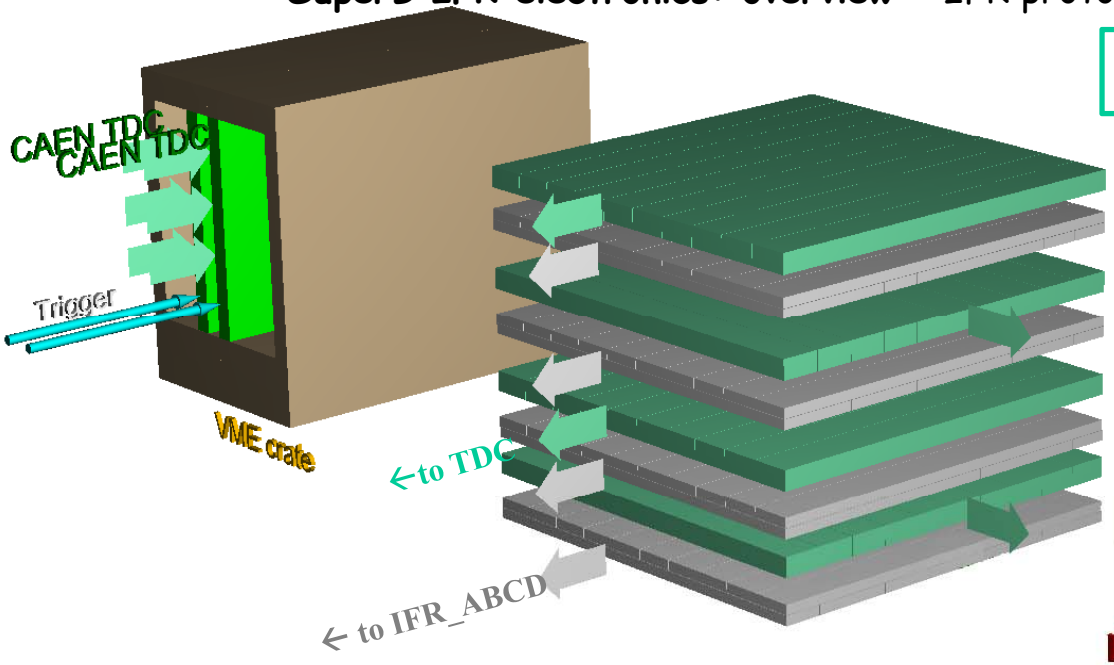
A collection of signals from the detector R&D setup in Ferrara; the detail shows a SiPM signal (blue) with a shape which could lead to a wrong timing measurement if the threshold were set at the level (b) shown in the detail.
The proper timing would be given by a threshold set at level (a).

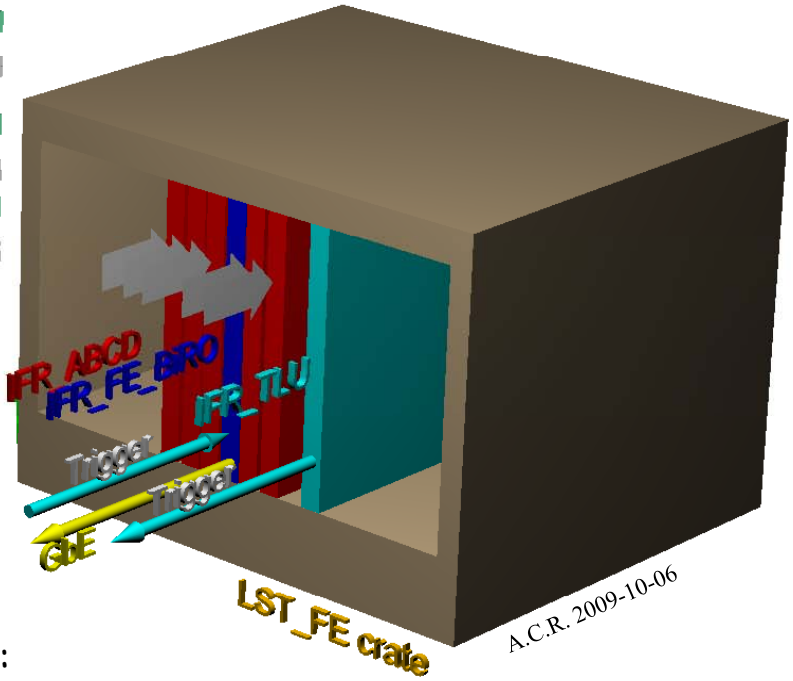
→ **...from previous slide**

due to the spread in the time of arrival of photons from a single "hit", setting a high threshold may not allow to obtain the true time of the event → two discriminators (LOW (a) plus HI (b) threshold) per channel → **two TDC records per event**

SuperB IFR electronics: overview – IFR prototype as a proof of principle

the concept....





SuperB IFR prototype:
- 4 layers of x-y scintillators, 1 cm thick, read in binary mode
- 4 layers of scintillators 2 cm thick, read in timing mode

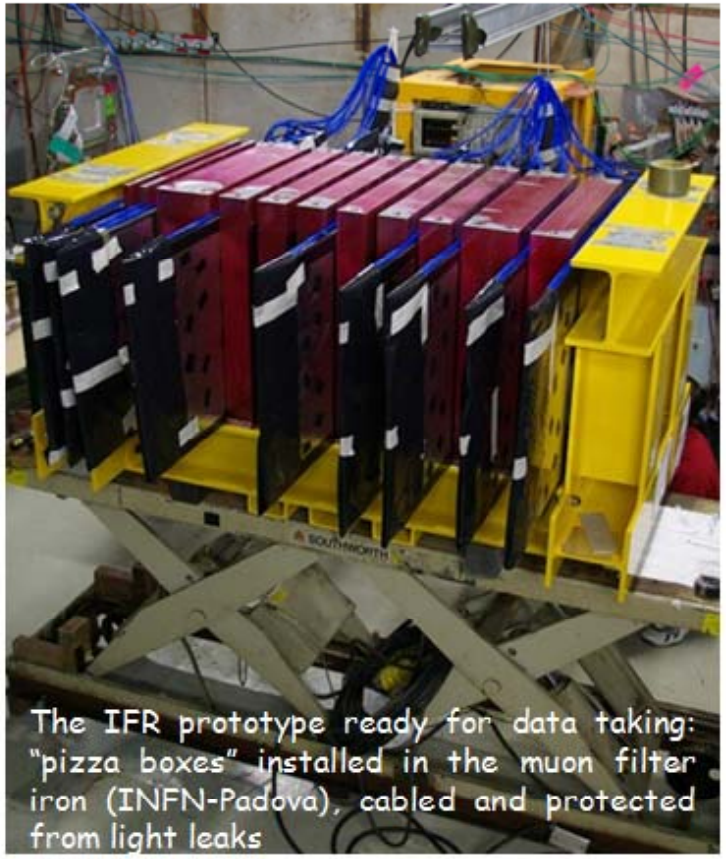
SuperB-IFR prototype readout electronics (baseline):
- "IFR_ABCD": sensor Amplification, Bias-conditioning, Comparators, Data processing:
it samples the level of the comparators outputs @ >= 80MHz and stores it, pending the trigger request
- "CAEN_TDC": a multi-hit TDC design based on CERN HP-TDC; hosted in a VME crate and read out via a VME CPU or via a VME-PCI bridge to the DAQ PC
- "IFR_FE_BiRO": collects data from IFR_ABCD cards upon trigger request and sends it to DAQ PC (via GbE)
- "IFR_TLU": a module (Trigger Logic Unit) to generate a fixed latency trigger based on primitives from the IFR prototype itself or from external sources

IFR_FE_BiRO + IFR_TLU are now a single module

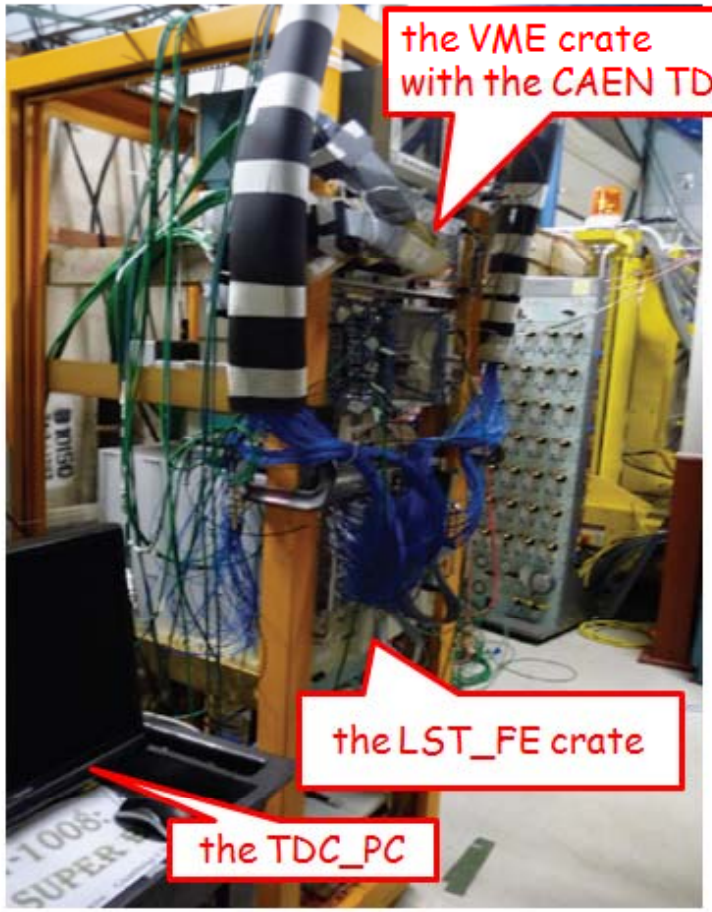
SuperB IFR electronics : Beam test of the IFR prototype electronics and DAQ system

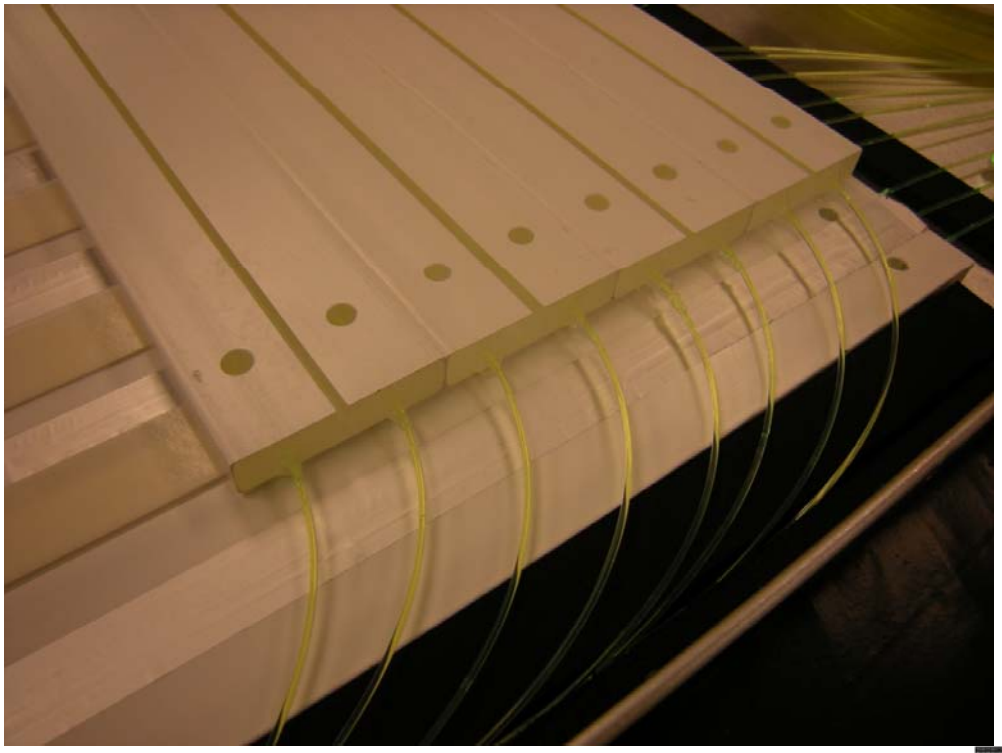
...and the real thing!

pictures from G. Cibinetto, "Some note on the beam test" presented at this meeting

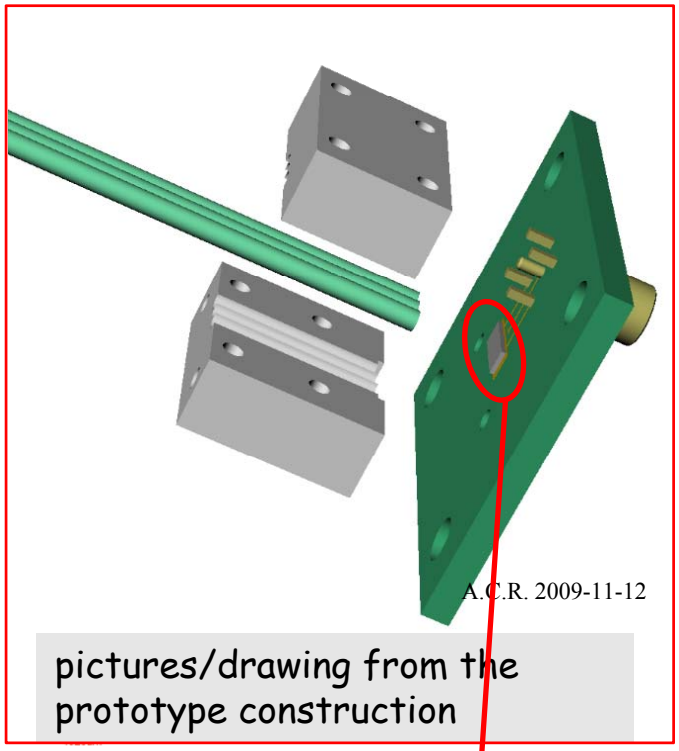


The IFR prototype ready for data taking: "pizza boxes" installed in the muon filter iron (INFN-Padova), cabled and protected from light leaks

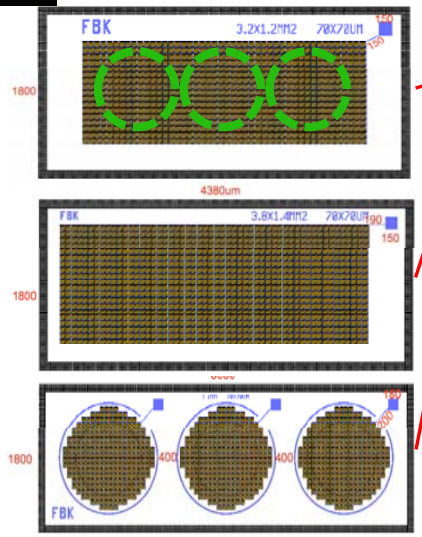




SuperB IFR : the scintillating bars are equipped with wavelength shifting fibers (3 for each bar in the prototype), which are then coupled to a SiPM device by means of precisely machined plastic supports.



pictures/drawing from the prototype construction



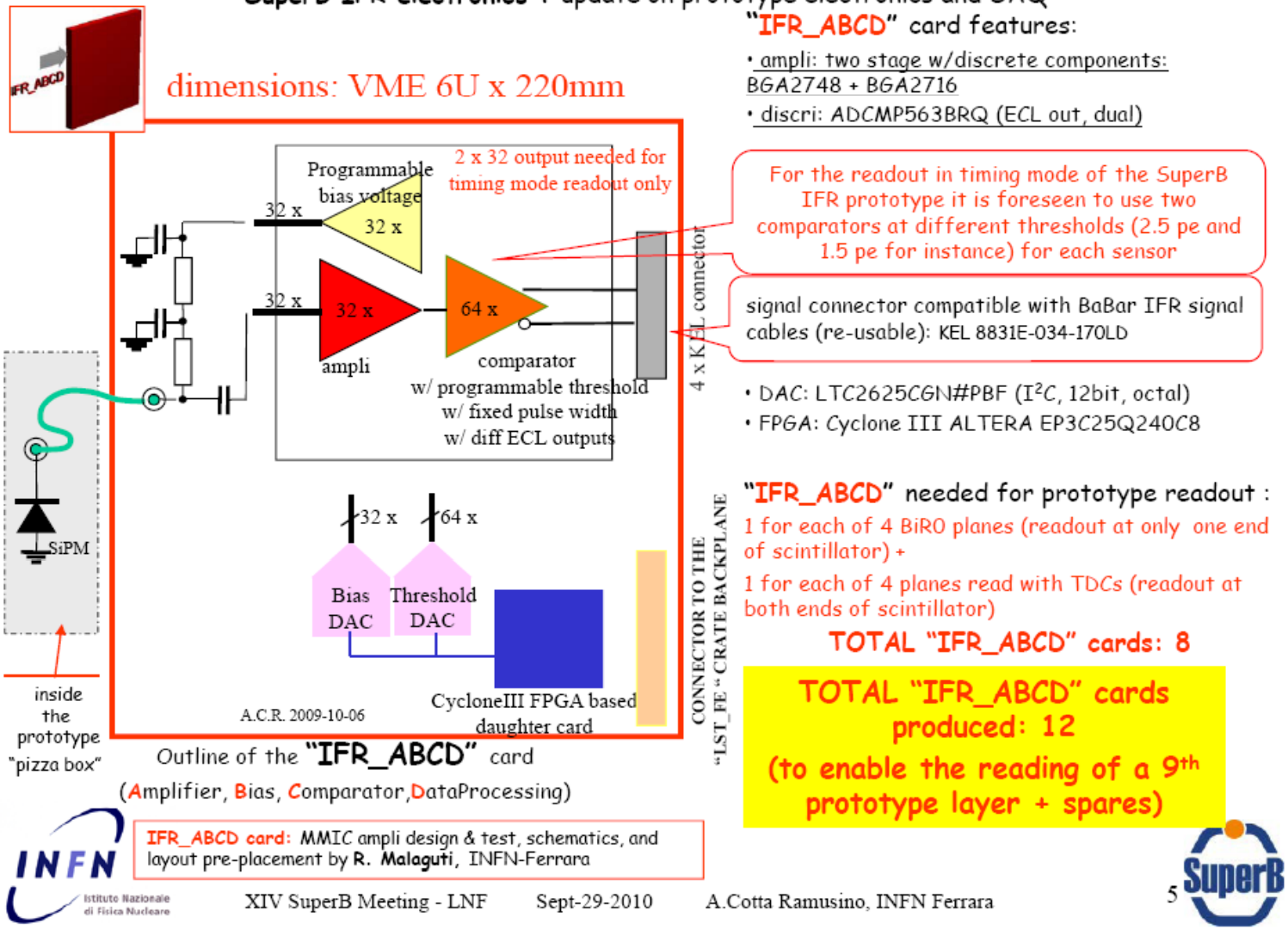
SiPM by FBK, Trento. 70x70um^2 cell size, n-on-p.

Bonding of the SiPM to the carrier PCB was performed at INFN Perugia thanks to G. Ambrosi, M. Ionica

SuperB IFR electronics: overview – IFR prototype as a proof of principle

The front end electronic card designed to read out the IFR small scale prototype has been based on discrete electronics (see also appendix A)

SuperB IFR electronics : update on prototype electronics and DAQ



"IFR_ABCD" card features:

- ampli: two stage w/discrete components: BGA2748 + BGA2716
- discri: ADCMP563BRQ (ECL out, dual)

For the readout in timing mode of the SuperB IFR prototype it is foreseen to use two comparators at different thresholds (2.5 pe and 1.5 pe for instance) for each sensor

signal connector compatible with BaBar IFR signal cables (re-usable): KEL 8831E-034-170LD

- DAC: LTC2625CGN#PBF (I^2C, 12bit, octal)
- FPGA: Cyclone III ALTERA EP3C25Q240C8

"IFR_ABCD" needed for prototype readout :

1 for each of 4 BiRO planes (readout at only one end of scintillator) +

1 for each of 4 planes read with TDCs (readout at both ends of scintillator)

TOTAL "IFR_ABCD" cards: 8

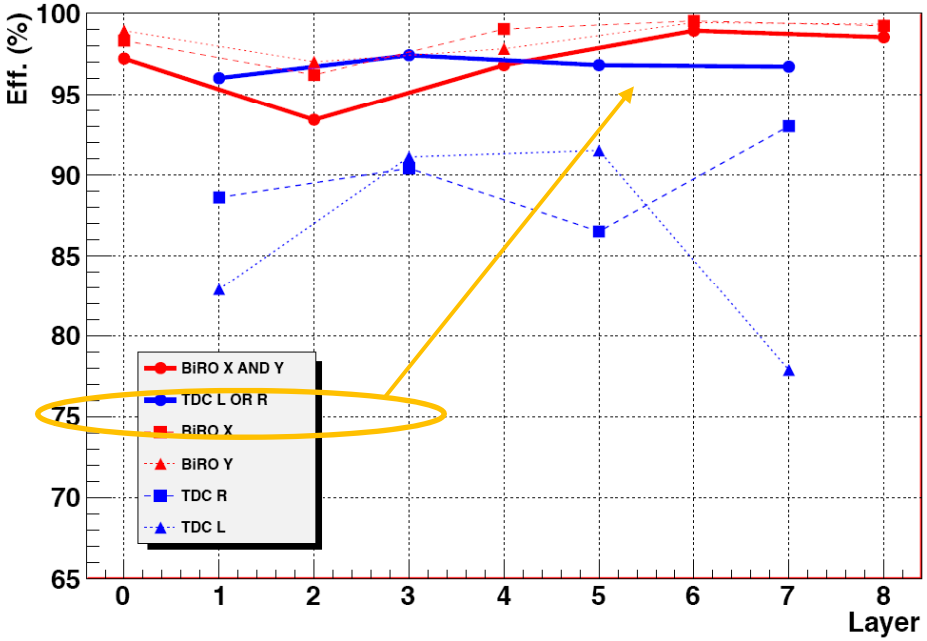
TOTAL "IFR_ABCD" cards produced: 12

(to enable the reading of a 9th prototype layer + spares)

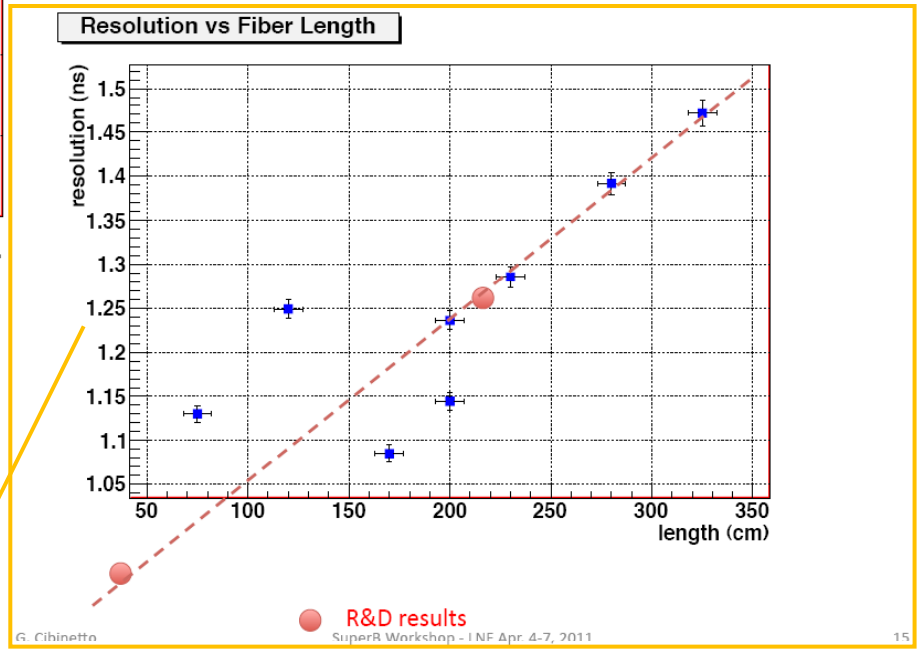
IFR_ABCD card: MMIC ampli design & test, schematics, and layout pre-placement by **R. Malaguti**, INFN-Ferrara

XIV SuperB Meeting - LNF Sept-29-2010 A.Cotta Ramusino, INFN Ferrara 5

from "Prototype data analysis" by G. Cibinetto, presented at the XVI SuperB workshop in LNF



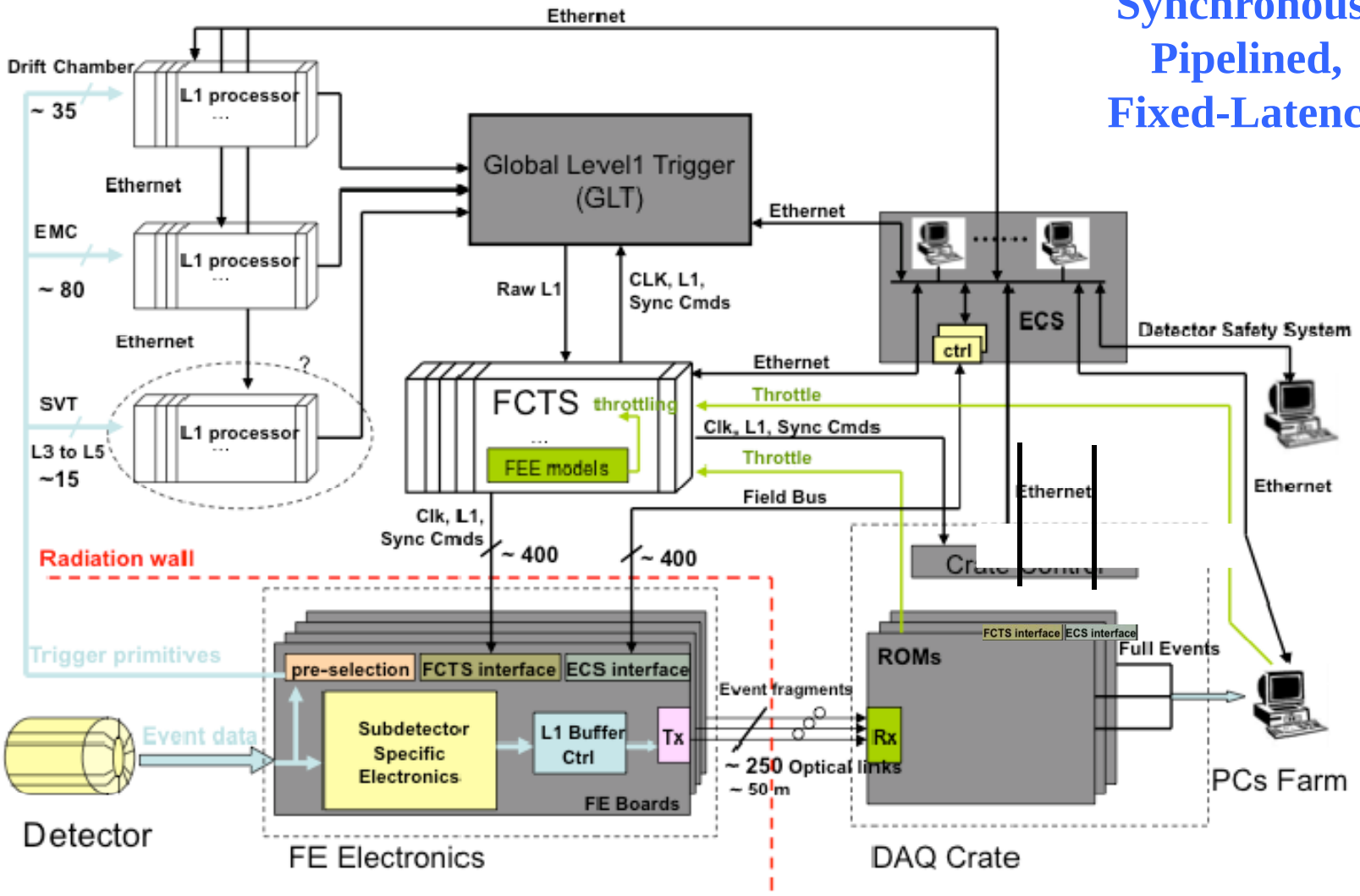
G. Cibinetto SuperB Workshop - LNF Apr. 4-7, 2011



Z position resolution ≈ 25cm

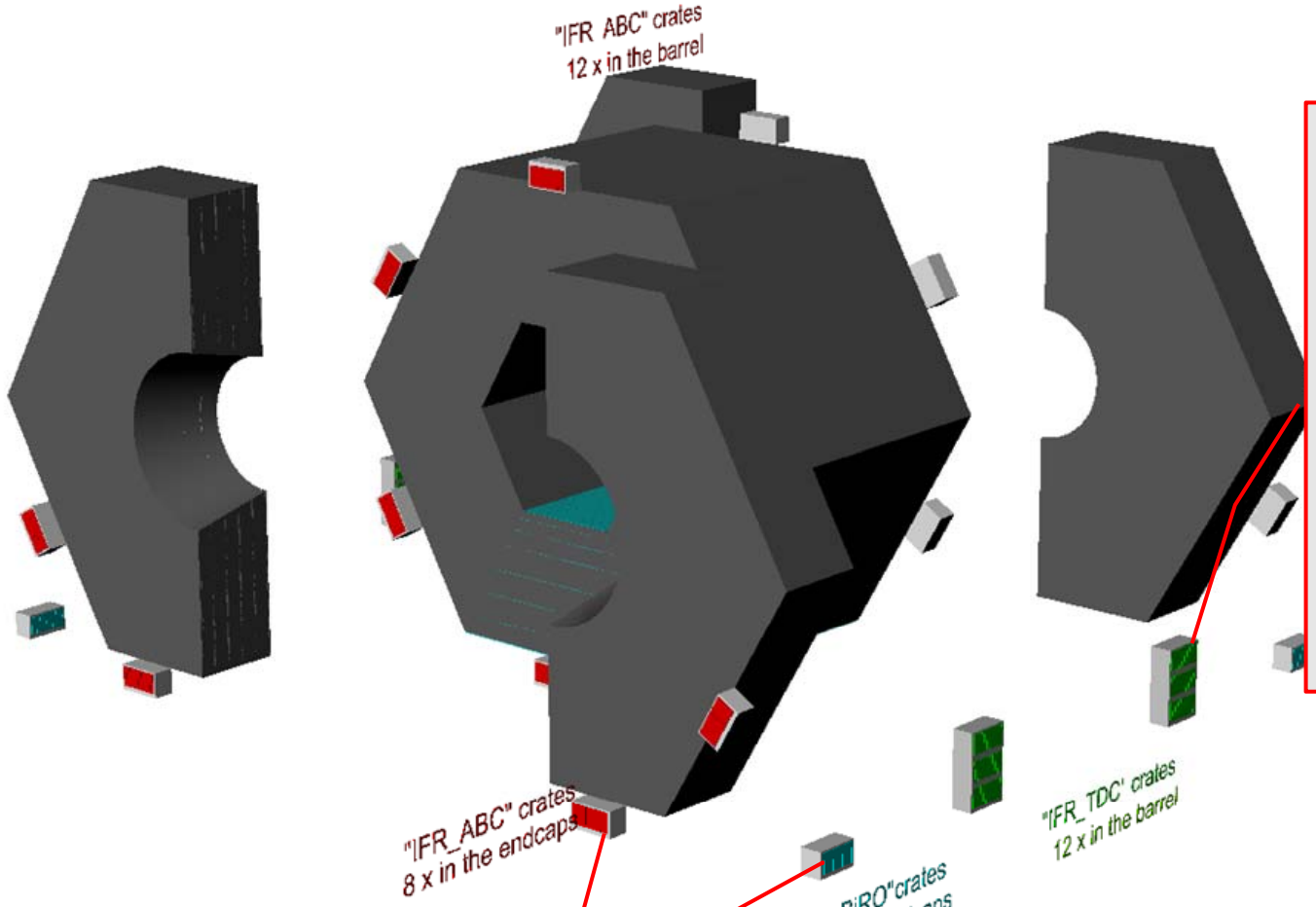
SuperB IFR electronics : overview - the overall SuperB DAQ architecture

Synchronous, Pipelined, Fixed-Latency



"**Electronics Trigger and DAQ - CERN meeting summary**", D.Breton (LAL), presented at the XVI SuperB workshop in LNF

SuperB IFR electronics : overview - baseline design: IFR front end electronics



The "**TDC**" cards contain:
- TDC digitizers (ACAM TDC GPX)
- memories, to buffer timing records for the trigger latency time
- trigger processing unit
- data link drivers

They readout the BARREL channels which produce **TIMING** information

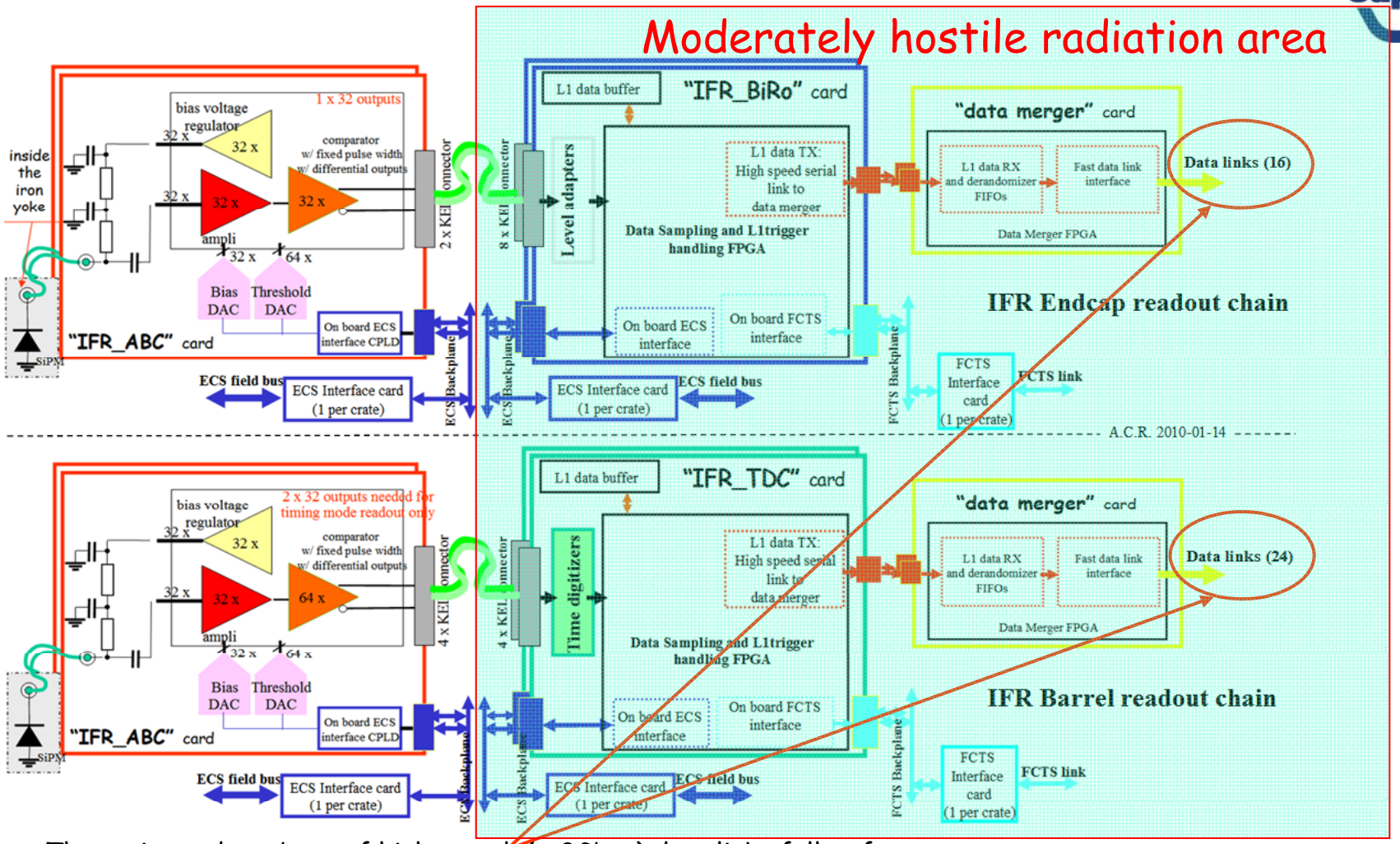
A.C.R. 2011-05-09

The "ABC" cards contain:
-Amplifier
-Bias circuit
-Comparators

The "Binary ReadOut" ("**BiRO**") cards contain:
- memories, to buffer samples of the comparator output for the trigger latency time
- trigger processing unit
- data link drivers

They readout the ENDCAP channels which produce a simple binary information ("hit" or "not hit")

SuperB IFR electronics : overview - baseline design: IFR front end electronics



The estimated numbers of high speed (≈2Gbps) data links follow from:
-the current SiPM dark count estimates at the operating conditions
-a trigger rate of 150kHz and a trigger extraction window of 150ns (determined by the trigger jitter)

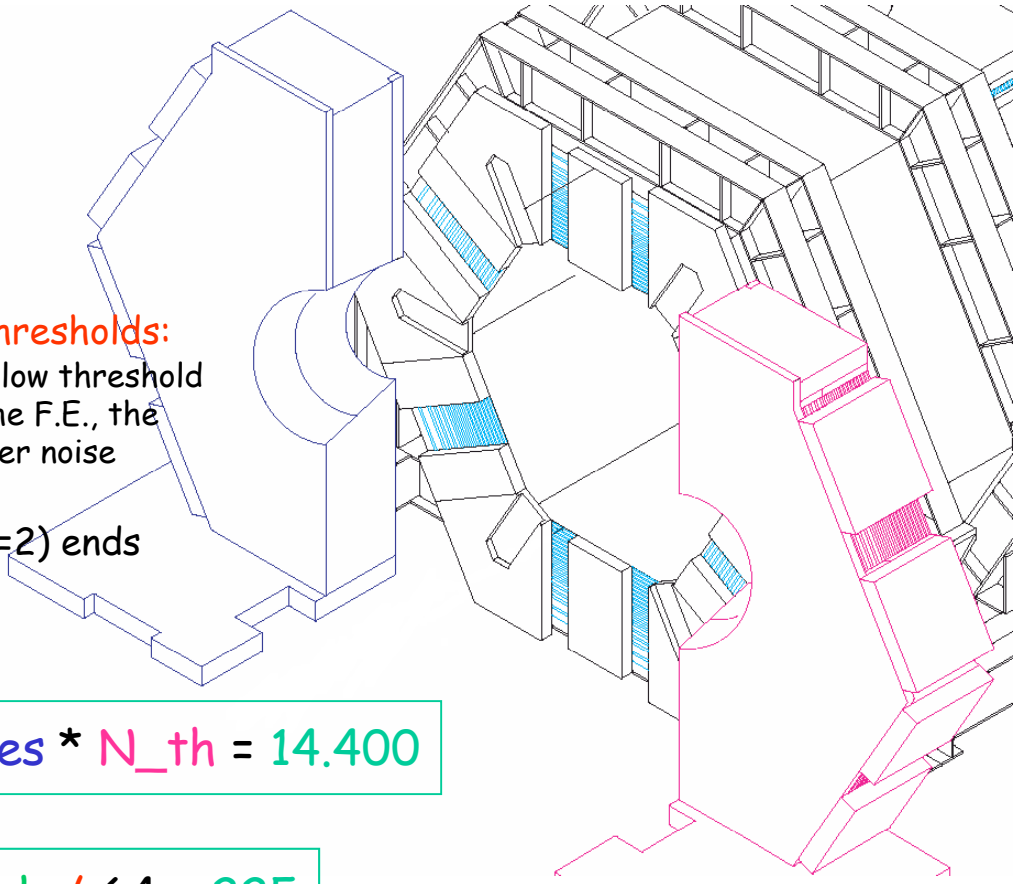
SuperB-IFR numerology:

• Barrel: N_Barrel = 3600 scintillator bars
(quoting G. Cibinetto)

Assuming:

• readout in TIMING mode with N_th (=2) thresholds:
both the high threshold (2.5 p.e. for instance) and the low threshold (1.5 p.e. for instance) crossing times are acquired by the F.E., the second threshold crossing validating the first for better noise rejection.

• each scintillator is readout from N_sides (=2) ends
-> total number of TDC channels: N_TDC_ch



W.Sands., Princeton Univ., 2003

N_TDC_ch = (N_Barrel) * N_sides * N_th = 14.400

N_TDC_board = N_TDC_ch / 64 = 225

Hopefully the tests on the prototype will show that it will be possible to keep:
N_th = 1
but in the meantime it is better to brace for the worst!

outline of the IFR DAQ electronics: data bandwidth estimates WITH BINARY READOUT FOR ENDCAP

SuperB-IFR numerology:

- EndCaps: N_EndCap = 2400 + 2400 scintillator bars

(quoting G. Cibinetto)

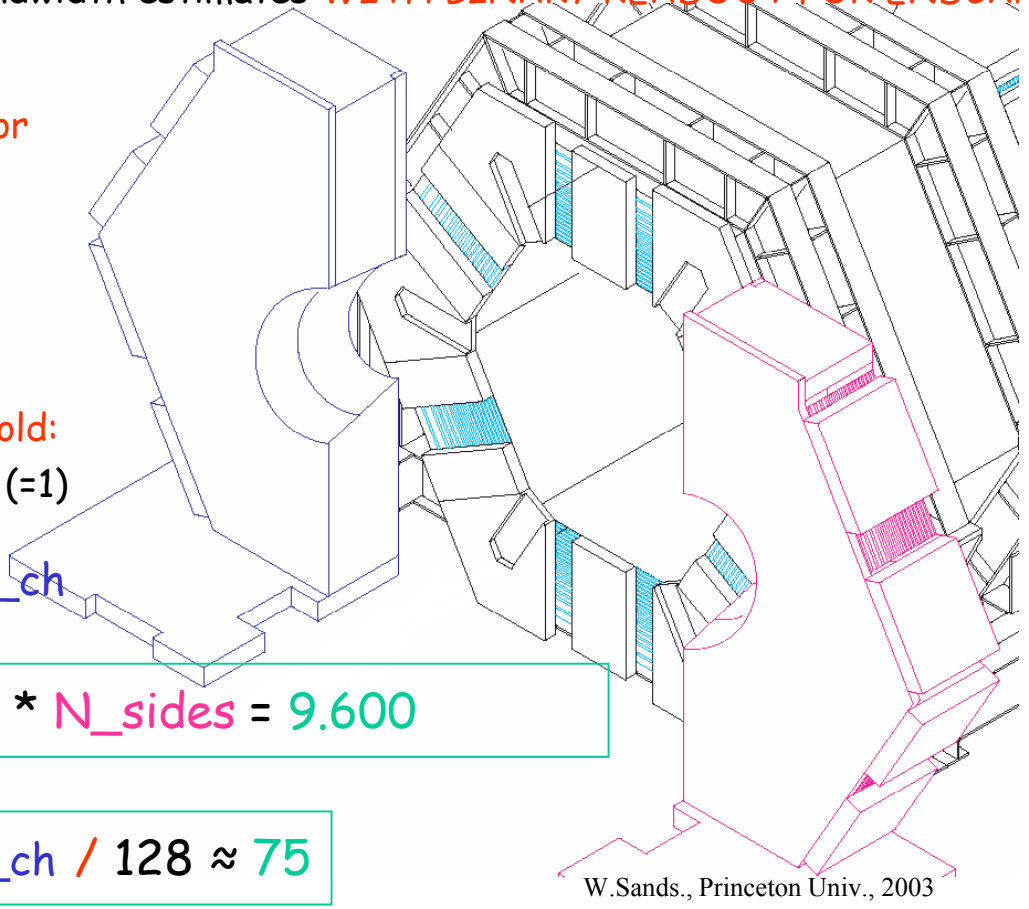
Assuming:

- the number of (thin) scintillators doubles (for X-Y readout; it's a coarse estimate)
- readout in BINARY mode with single threshold:
- each scintillator is readout from N_sides (=1) ends

-> total number of BiRO channels: N_BiRO_ch

$$N\_BiRO\_ch = (N\_EndCap) * 2 * N\_sides = 9.600$$

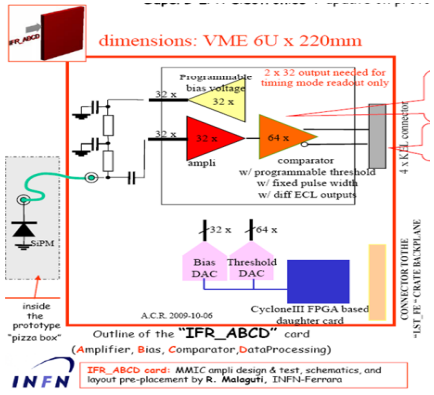
$$N\_BiRO\_Board = N\_BiRO\_ch / 128 \approx 75$$



W.Sands., Princeton Univ., 2003

For bars read out in "binary" mode N_sides has settled to: 1

SuperB IFR electronics : from baseline to final design: exploiting available SiPM readout ASICs



The "IFR_ABCD" has proven to be a flexible and reliable design, easy to adapt to "p-on-n" as well as "n-on-p" SiPM devices. Its on board microcontroller allows for stand –alone operation and its amplifier monitoring outputs make the "IFR_ABCD" a good SiPM characterization tool.

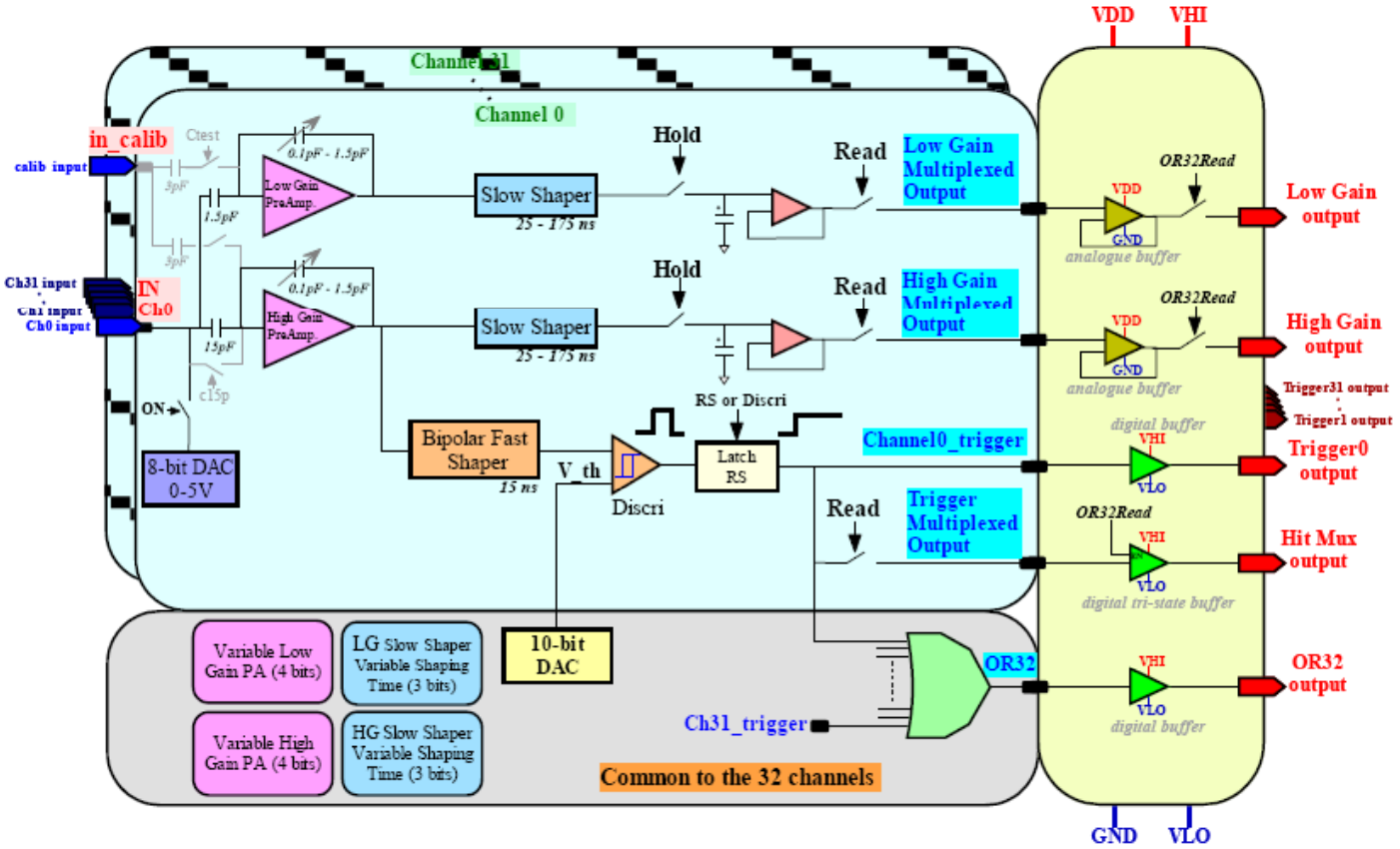
NEVERTHELESS WHEN PLANNING THE READOUT OF > 20.000 CHANNELS it is good to look for ASICs solutions, starting from existing ones. A good occasion was the:

Infact the present state of the art was very effectively described in:

"**Review of ASIC developments for SiPM signal readout**",
Wojtek Kucewicz, AGH- University of Science and Technology Krakow.

SuperB IFR electronics : from baseline to final design: exploiting available SiPM readout ASICs

One of the ASICs presented at the SiPM event was the "EASIROC" by the OMEGA group of LAL in Orsay.



It has an individual trigger output for each of 32 channels plus 32 individual bias setting DACs and a common threshold setting DAC.

!!! CAVEAT: the EASIROC was not designed to operate in a high radiation area

USER GUIDE Omega

EASIROC

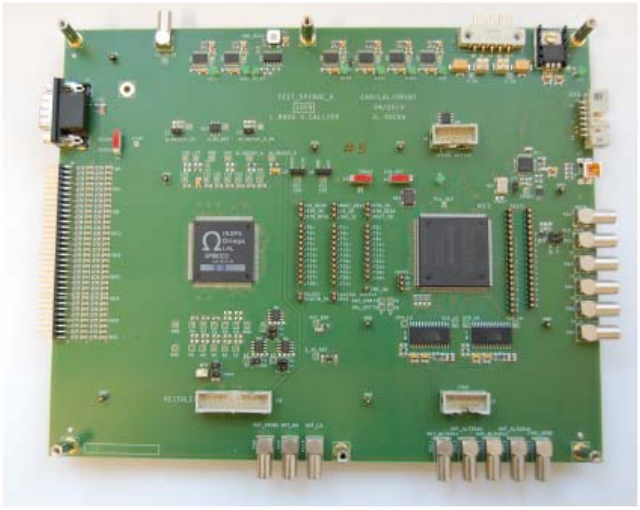
SOFTWARE & TEST BOARD USER GUIDE

Version: 11 April 2011

Abstract

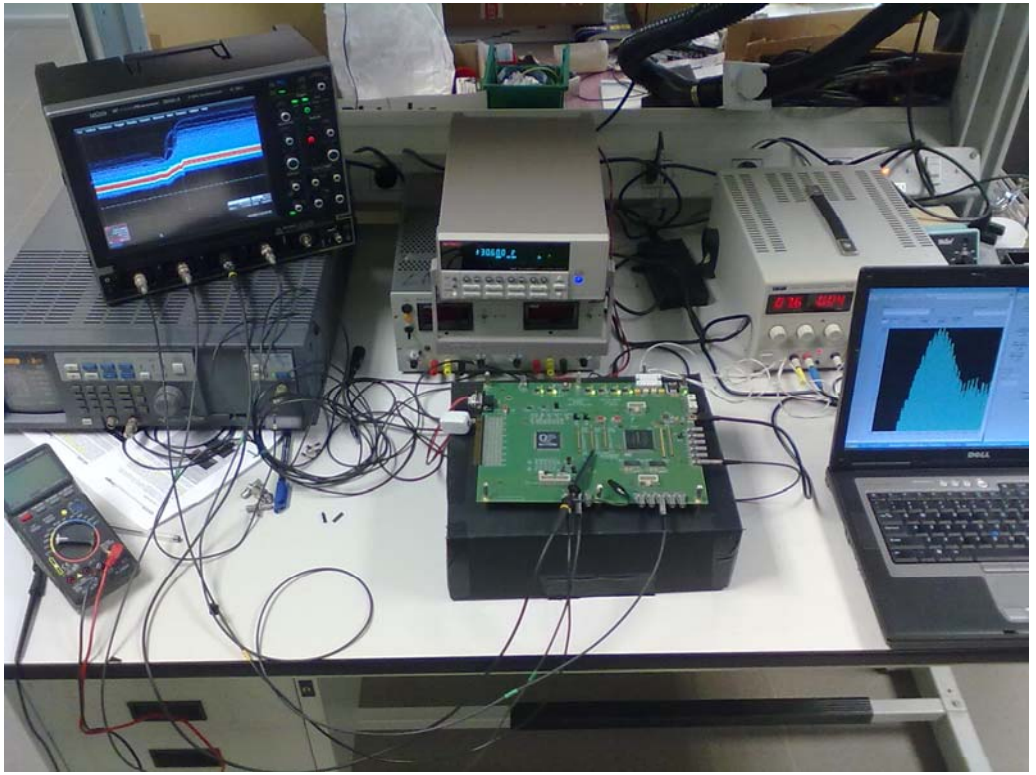
EASIROC (previously SPIROC0), standing for *Extended Analogue Silicon pm Integrated Read Out Chip*, is a 32-channel fully-analogue front end ASIC dedicated to the gain trimming and read-out of SiPM detectors.

This guide explains how to install & use the test board for EASIROC and how to operate with the associated software.

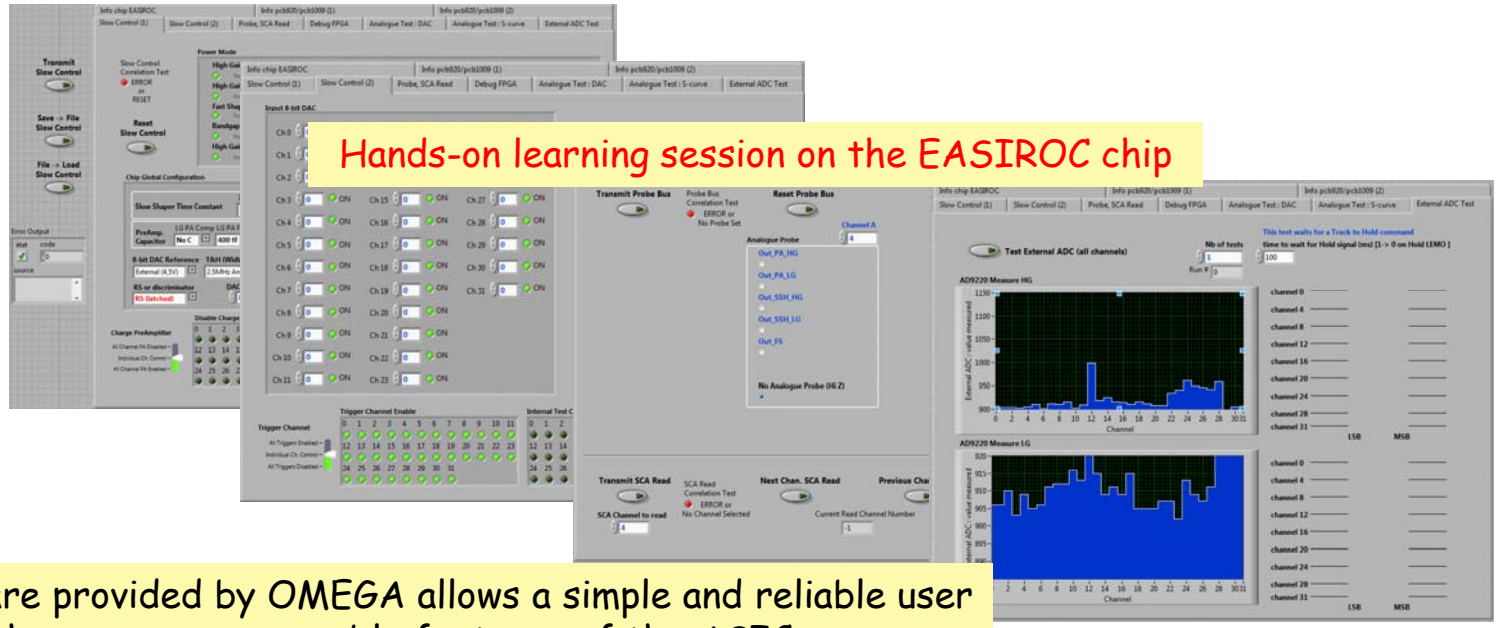


Orsay MicroElectronics Group Associated

Gisèle MARTIN-CHASSARD and Stephane CALLIER of OMEGA have provided us not only plenty of information but a complete hardware and software test system, which we have been using in Ferrara since a couple of weeks to learn "hands-on"



SuperB IFR electronics : from baseline to final design: exploiting available SiPM readout ASICs



Hands-on learning session on the EASIROC chip

The software provided by OMEGA allows a simple and reliable user control of the many programmable features of the ASIC.

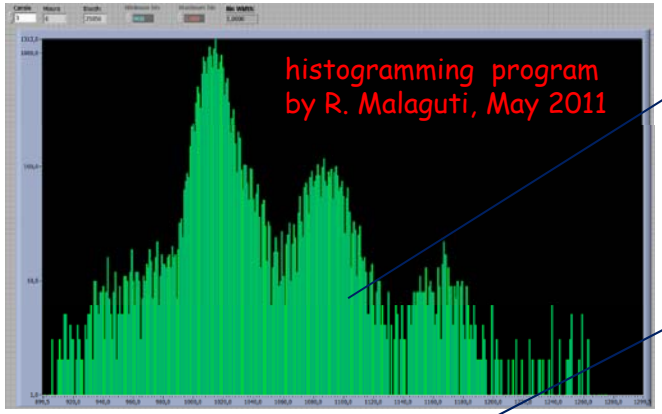
Step 1:
- Setup the EASIROC chip and look at signals

analog output monitored after the Sample and Hold
(with hold signal generated inside the on-board FPGA
after a slight modification by Roberto Malaguti, INFN-FE)

active low HOLD_n signal

Trigger output associated to the tested channel.
The jitter we measured with respect to the light pulse shone on the SiPM was too high for the EASIROC to be used for TDC timing mode readout **but the trigger outputs are perfectly good for Binary Reaadout mode of the SiPM of the IFR**

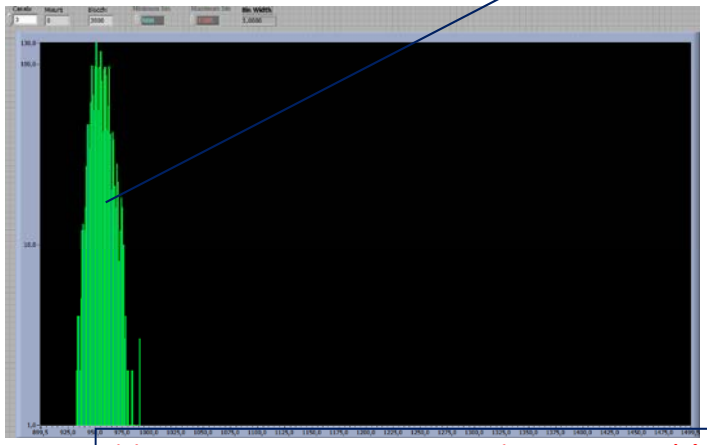
Step 2:
- use the 12bit ADCs of the test board to collect spectra of signals from the active device connected to the input

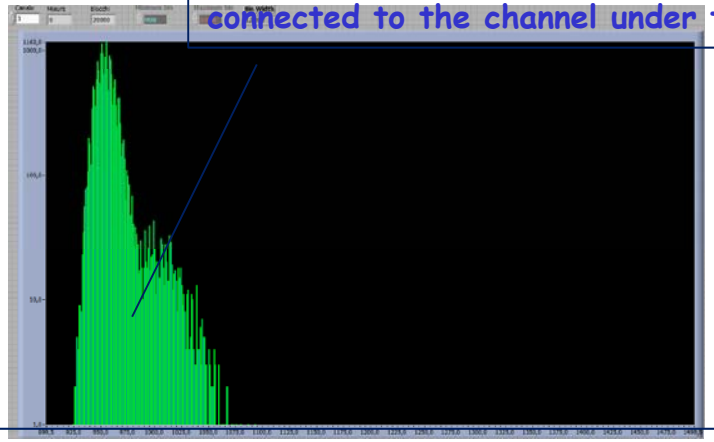


dark current amplitude histogram for an Hamamatsu 1x1mm^2 MPPC, biased at 69.84V, connected to the input under test

dark current amplitude histogram for an FBK 1.2x3.2mm^2 SiPM, biased at 30.90V, connected to the channel under test

amplitude histogram for dark current + LED pulser induced events, for an FBK 1.2x3.2mm^2 SiPM, biased at 30.90V, connected to the channel under test



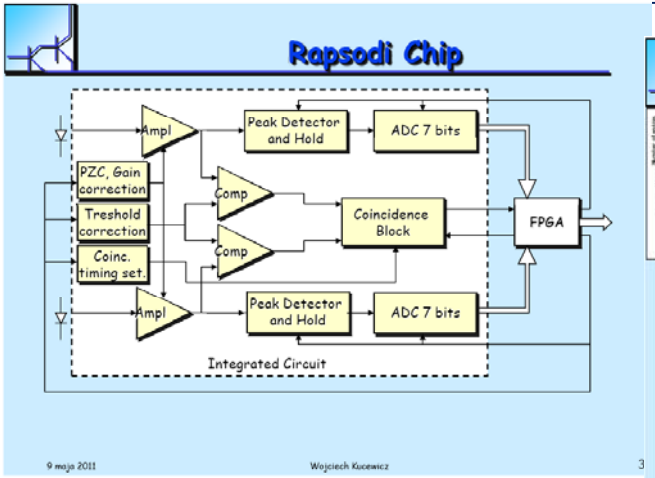


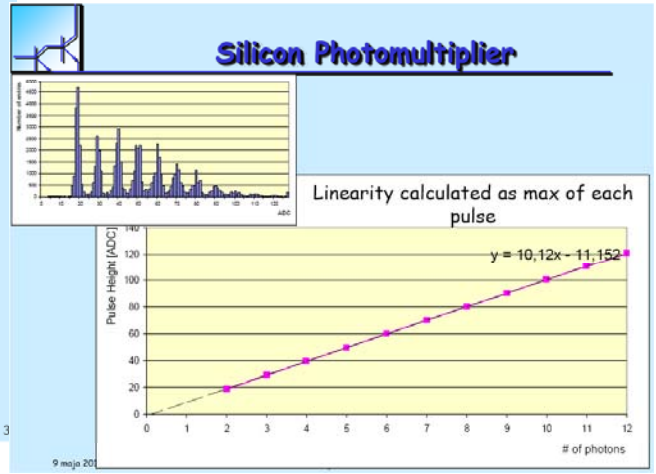
Note: our setup uses a 1m coax cable to connect the SiPM carrier PCB to the ORSAY test board. This and, possibly, the fact that the substrate of the SiPM (n-on-p device) is connected to the EASIROC input seems to introduce more noise in the SiPM case → MORE WORK NEEDED TO DECREASE INJECTED NOISE

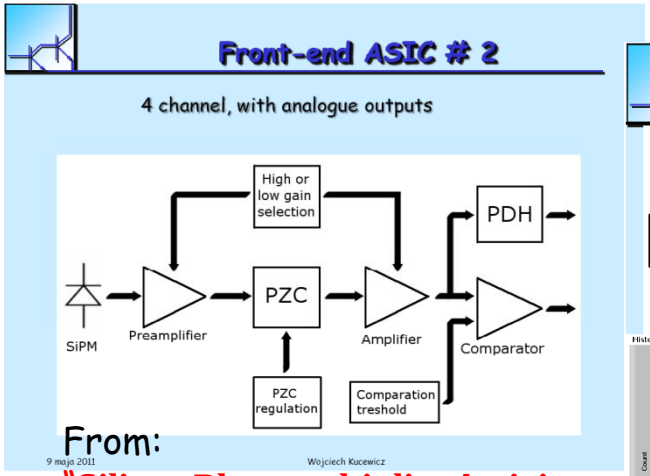
THE ORSAY TEST BOARD WOULD A NICE TOOL TO HAVE TO CHARACTERIZE ON A LARGE SCALE THE SiPM FOR THE CONSTRUCTION OF THE IFR!!

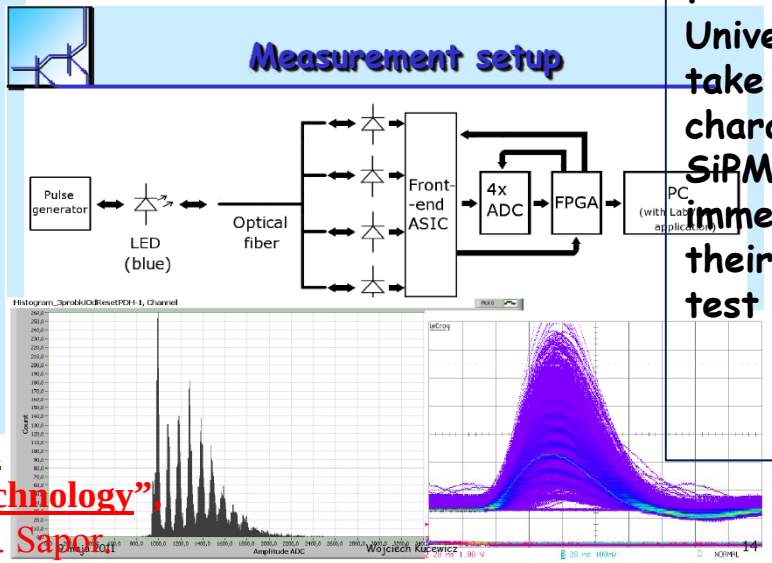
SuperB IFR electronics : from baseline to final design: exploiting available SiPM readout ASICs

One of the important assets brought by the AGH- University of Science and Technology in joining the SuperB collaboration is their experience in ASIC design as shown by the RAPSODY chip (and its successors):









Discussion items:

? Would AGH University consider feasible a redesign of their ASICs to address the requirements of the SuperB IFR detectors?

? Would AGH University, consider to take on the large scale characterization of the SiPM, taking full and immediate advantage of their current ASICs and test systems ?

From:

"Silicon Photomultiplier Activity at AGH-University of Science and Technology",
W. Kucewicz, J. Barszcz, S. Głąb, M. Sapor

While our prototype electronics (IFR_ABCD, IFR_BiRO, IFR_TDC) did not include any **radiation mitigation feature, these must be included, most likely, in the final design of the SuperB IFR readout system**.

A dedicated group of SuperB collaborators is characterizing the data links (for trigger, data and detector control) to/from the sub-detectors specific electronics system and will provide a radiation-proven design to the rest of the collaboration.

Each sub-detector group is instead responsible for integrating radiation mitigation features in its sub-detector specific readout; this might involve the use of flash based FPGAs on the hardware side and the use of proper design techniques on the firmware side(TRM, hamming coding for FSM ..) eventually assisted by currently available CAE tools.

We intend to explore solutions based on Actel proASICs as the target FPGA for the IFR readout system and Mentor Graphics HDL tools specifically design to automatize the

? Would AGH University consider to share with us the effort needed to prototype and characterize under radiation the critical blocks of the IFR data acquisitions ?

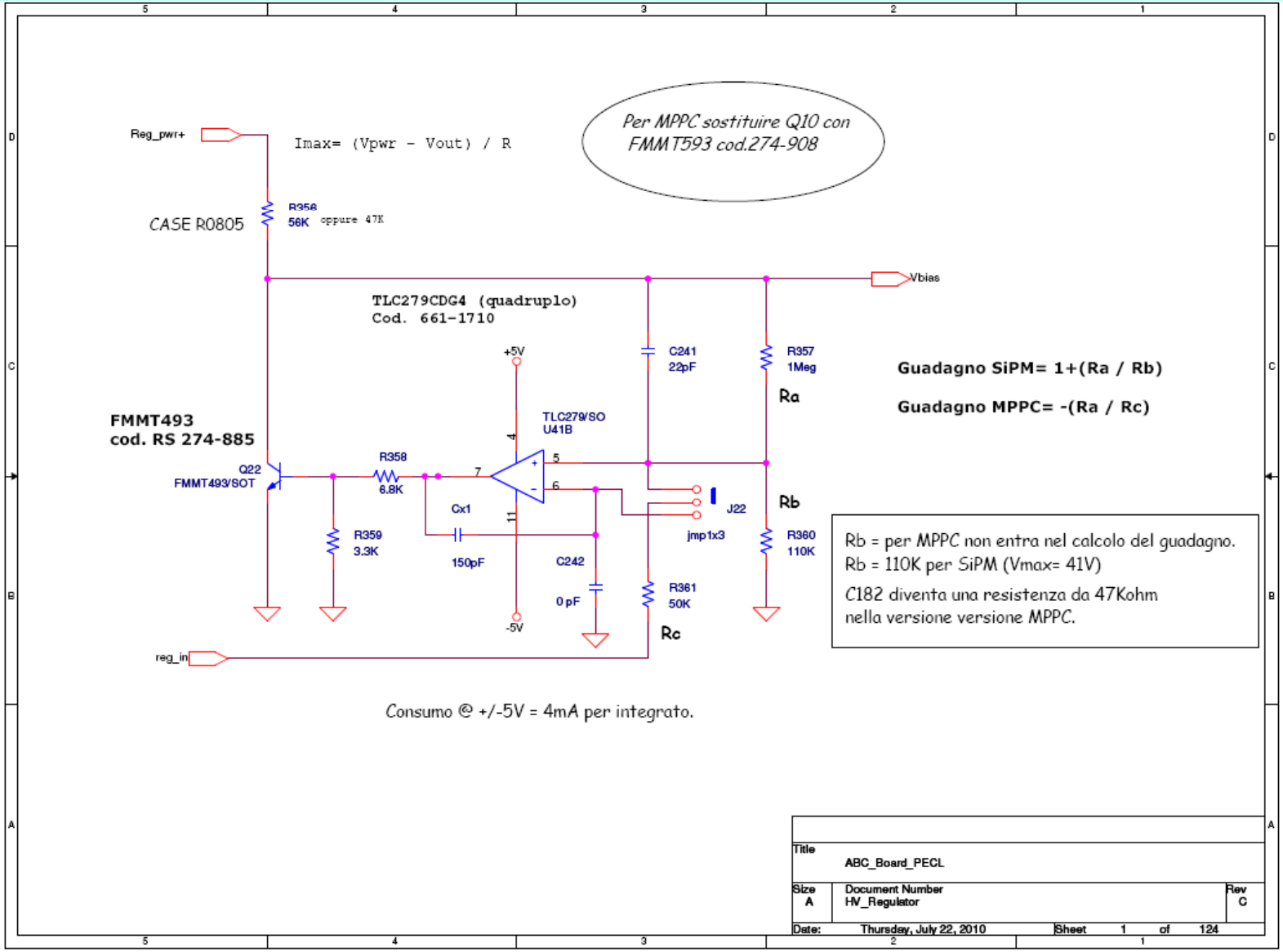
Conclusions:

While the prototype electronics which was designed so far allowed us to build a working small scale prototype, when preparing for the final system we should aim for a front end design based on suitable ASICs.

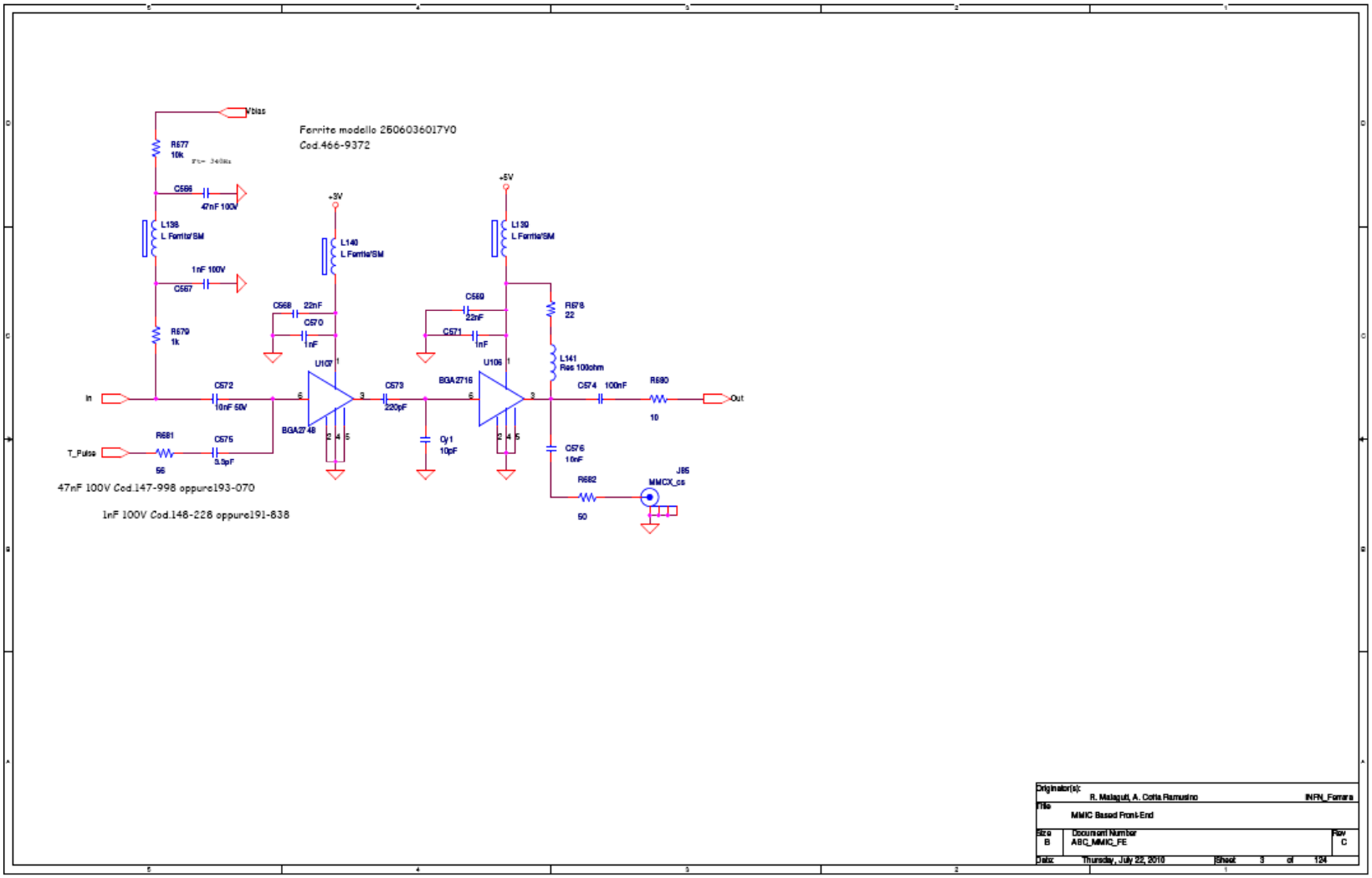
Also, while waiting for final estimates on the radiation rates in and around the detector, we should be prepared to estimate the costs and the performance toll of designing the front end electronics and latency buffers using radiation mitigation techniques.

In both tasks as well as in the large scale characterization of the SiPM devices needed for the construction of the IFR, the AGH University of Science and Technology in Krakow would be a very welcome partner.

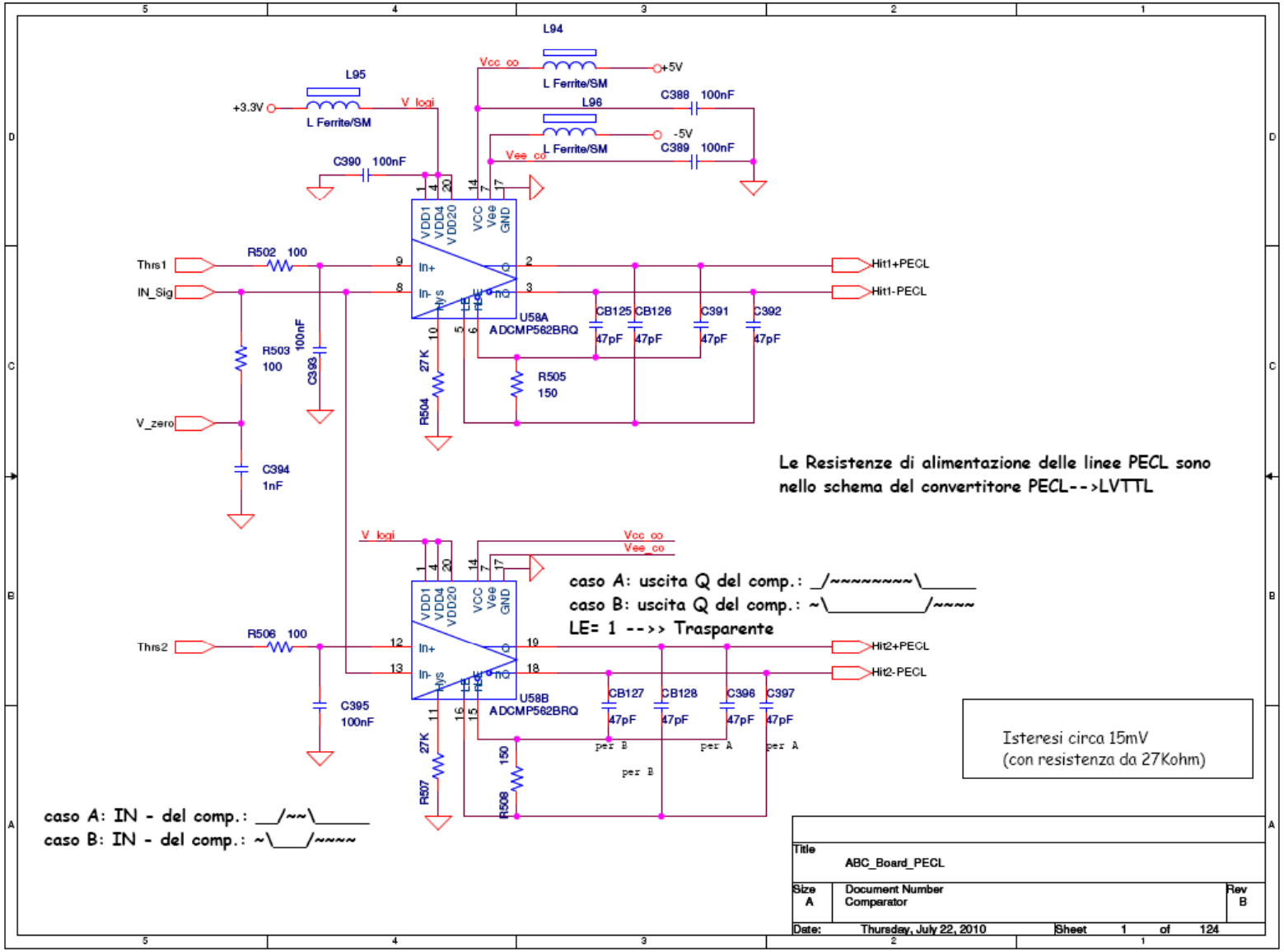
SuperB IFR electronics : APPENDIX A: schematic diagrams of some key parts of the "IFR_ABCD" board: individual SiPM bias



SuperB IFR electronics : APPENDIX A: schematic diagrams of some key parts of the "IFR_ABCD" board: individual amplifier channel with input MMCX connector and analog monitor output (also on MMCX connector)



SuperB IFR electronics : APPENDIX A: schematic diagrams of some key parts of the "IFR_ABCD" board: dual comparator channel with pulse shaping (T_width ≈ 20ns)



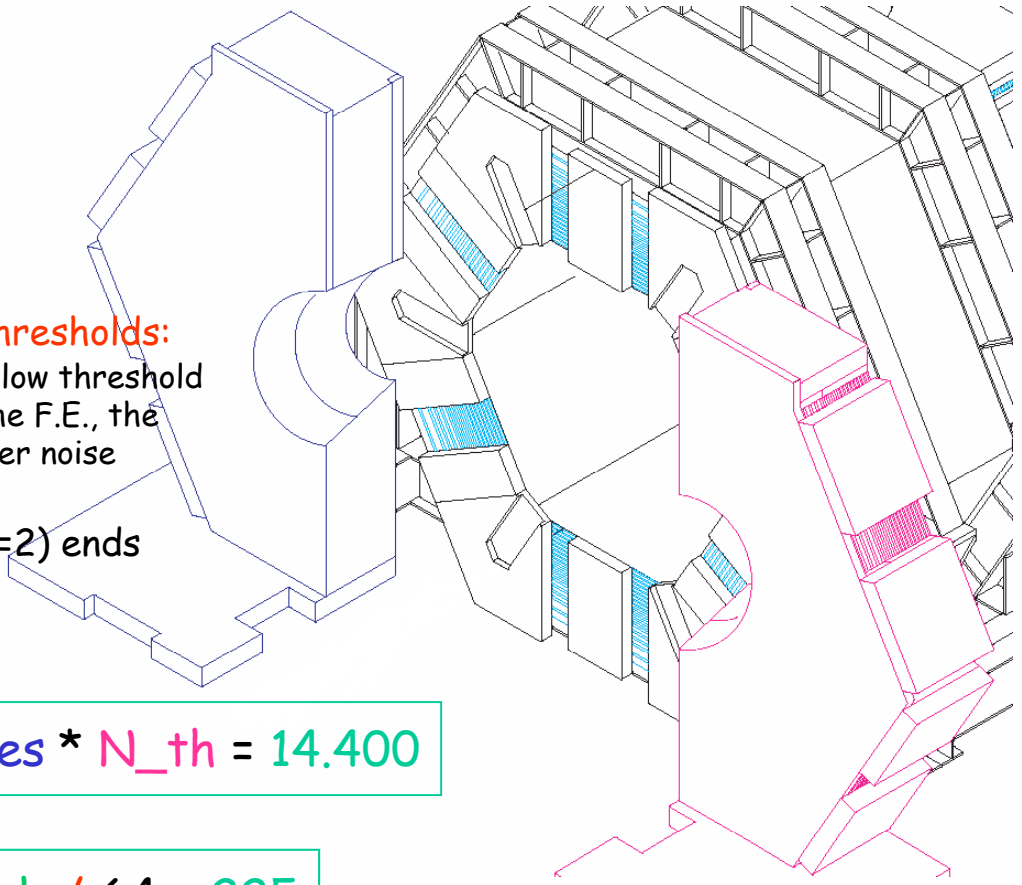
SuperB-IFR numerology:

• Barrel: N_Barrel = 3600 scintillator bars
(quoting G. Cibinetto)

Assuming:

• readout in TIMING mode with N_th (=2) thresholds:
both the high threshold (2.5 p.e. for instance) and the low threshold (1.5 p.e. for instance) crossing times are acquired by the F.E., the second threshold crossing validating the first for better noise rejection.

• each scintillator is readout from N_sides (=2) ends
-> total number of TDC channels: N_TDC_ch



W.Sands., Princeton Univ., 2003

$$N\_TDC\_ch = (N\_Barrel) * N\_sides * N\_th = 14.400$$

$$N\_TDC\_board = N\_TDC\_ch / 64 = 225$$

Hopefully the tests on the prototype will show that it will be possible to keep:
N_th = 1
but in the meantime it is better to brace for the worst!

SuperB IFR electronics : APPENDIX B: estimates of number of channels, hit rates, triggered data bandwidth

outline of the IFR DAQ electronics: data bandwidth estimates WITH TIMING READOUT FOR BARREL
SuperB-IFR numerology:

"Physics" rate : **500kHz**/channel, <u>in the hottest region</u>, arising from:

- particle rate : O(100Hz) / cm^2 (including background)
- dimensions of a detector element : < 400cm x 4cm (thickness 20mm)

(quoting R.Calabrese, W.Baldini, G.Cibinetto)

"Dark count" rate : **for a 1mm^2 SiPM by FBK:**

(quoting R.Malaguti, L.Milano test results in Ferrara)

@ 0.5pe threshold

- @ 25°C, 34.4V: ≈ 360kHz
- @ 5°C, 33.8V: ≈ 128kHz

@ 2.5pe threshold

- @ 25°C, 35V: ≈ 20kHz
- @ 5°C, 34V: ≈ 6.3kHz

!!! The "dark count" rate scales with the sensor's area and we don't know yet which would be the final area of the sensor of choice (a 4mm^2 is also being considered)

!!! We need to have, on each processing channel, one comparator with a low threshold (0.5pe? 1.5pe? Only prototype test will tell) → it's TDC input will see the highest rate.

Let's consider a "Hit" rate of:

Hit_rate = physics_rate + dark count_rate ≤ 1MHz per TDC input !!!

it is compatible with the TDC-GPX maximum sustained input rate

SuperB IFR electronics : APPENDIX B: estimates of number of channels, hit rates, triggered data bandwidth

outline of the IFR DAQ electronics: data bandwidth estimates WITH TIMING READOUT FOR BARREL

if we do L1 trigger matching on board

--- BARREL

- assuming a 150ns trigger window

- assuming that trigger matching is performed at the front end cards

- assuming a "hit rate per scintillating element" of 1MHz per channel in the barrel (500Khz of "physics" + 500KHz of dark count rate because of the low threshold needed to improve timing precision)

- assuming that an event from an "IFR_TDC" board is built like outlined below:

  - Header = Board ID + Frame ID (allows to reconstruct ABSOLUTE timing for hit records) : 12 Byte
  - Channel ID + hit timing information RELATIVE to beginning of frame : 4 Byte per Hit
  - Trailer = L1_Trigger_Data + WordCount + error code: 12 Byte

- assuming that on each TDC half of the channels has a 1MHz input rate and half has a 500KHz input rate →

The TDC event size and data rates can be estimated as follows:

<"IFR_TDC" event size> = 12 + [(0.15us * 1MHz) hit * 32 + (0.15us * 0.5MHz) hit * 32] * 4 + 12 ≈ 12 + 8 * 4 + 12 ≈ **0.06kB**

and thus the "**trigger matched**" data rate produced by each "IFR_TDC" is:

<"IFR_TDC" data rate> = 150KHz * 0.06kB ≈ **9MB/s**

SuperB IFR electronics : APPENDIX B: estimates of number of channels, hit rates, triggered data bandwidth

outline of the IFR DAQ electronics: data bandwidth estimates WITH TIMING READOUT FOR BARREL

if we do L1 trigger matching on board

BARREL summary

- **Number of "IFR_TDC"s = 225**

- Numbers per "IFR_TDC" board:
  <"IFR_TDC" event size> = 0.06kB
  <"IFR_TDC" data rate> = 9MB/s
- Average event size for the whole Barrel read in timing mode:
  <Event size Barrel> = 0.06kB * 225 ≈ 13.5kB
- Total data rate produced by the Barrel:
  <Event data rate Barrel> = 9MB/s * 225 ≈ 2,025MB/s
- Tentative calculation of the number of links required (assuming the "concentration" of 10 "IFR_TDC" output links into 1 link at 2Gbps):
  Number_of_data_links_barrel = 225 / 10 ≈ 24
  (i.e. 2 links per digitizer crate)

outline of the IFR DAQ electronics: data bandwidth estimates WITH BINARY READOUT FOR ENDCAP

SuperB-IFR numerology:

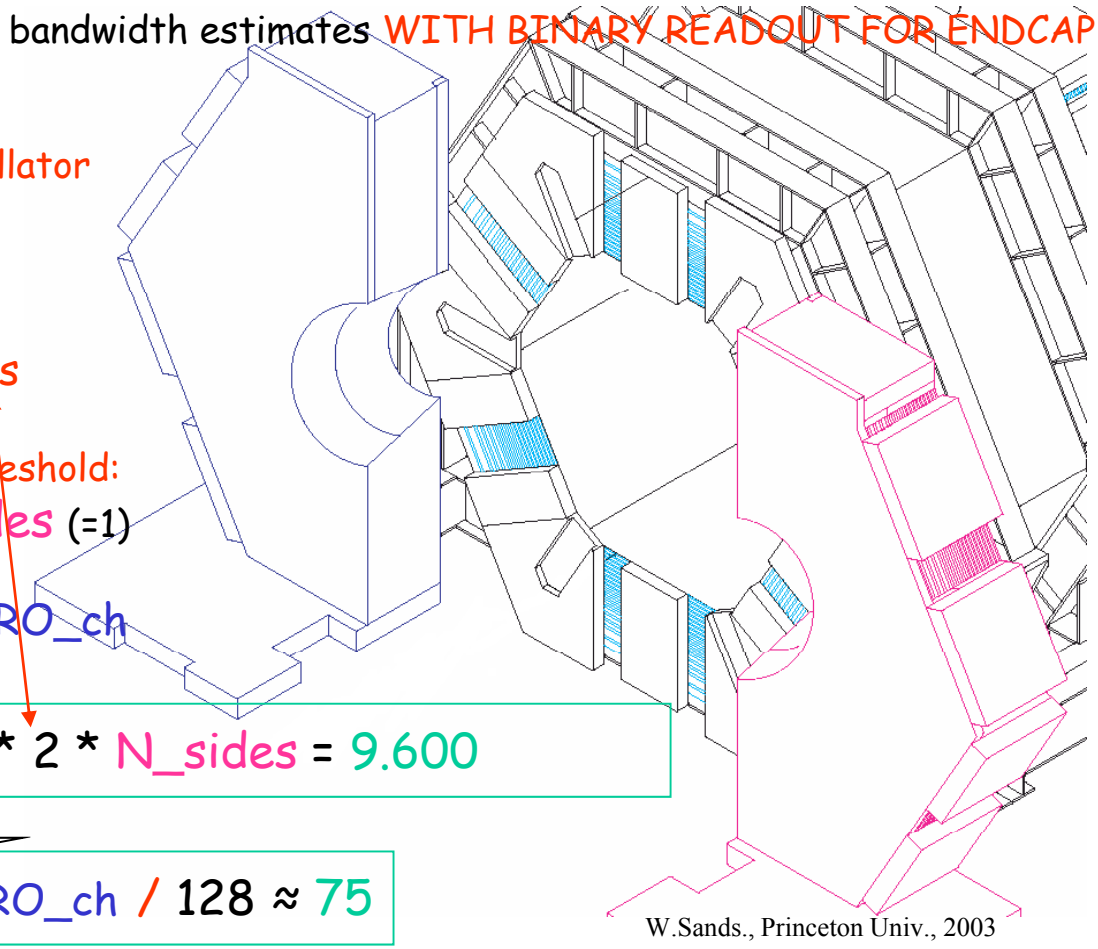
- EndCaps: N_EndCap = 2400 + 2400 scintillator bars

(quoting G. Cibinetto)

Assuming:

- the number of (thin) scintillators doubles (for X-Y readout; it's a coarse estimate)
- readout in BINARY mode with single threshold:
- each scintillator is readout from N_sides (=1) ends

-> total number of BiRO channels: N_BiRO_ch



W.Sands., Princeton Univ., 2003

$$N\_BiRO\_ch = (N\_EndCap) * 2 * N\_sides = 9.600$$

$$N\_BiRO\_Board = N\_BiRO\_ch / 128 \approx 75$$

For bars read out in "binary" mode N_sides has settled to: 1

outline of the IFR DAQ electronics: data bandwidth estimates WITH BINARY READOUT FOR ENDCAP
SuperB-IFR numerology:

"Physics" rate : **500kHz**/channel, in the hottest region, arising from:

- particle rate : O(100Hz) / cm^2 (including background)
- dimensions of a detector element : < 400cm x 4cm (thickness 20mm)

(quoting R.Calabrese, W.Baldini, G.Cibinetto)

"Dark count" rate : **for a 1mm^2 SiPM by FBK:**

(quoting R.Malaguti, L.Milano test results in Ferrara)

@ 0.5pe threshold

- @ 25°C, 34.4V: ≈ 360kHz
- @ 5°C, 33.8V: ≈ 128kHz

@ 2.5pe threshold

- @ 25°C, 35V: ≈ 20kHz
- @ 5°C, 34V: ≈ 6.3kHz

!!! The "dark count" rate scales with the sensor's area and we don't know yet which would be the final area of the sensor of choice (a 4mm^2 is also being considered)

!!! We need to have, on each processing channel, just one comparator with a 2.5pe threshold
→ The dark count rate @ 2.5pe threshold is just a fraction of the physics rate

Let's consider a "Hit" rate of:
Hit_rate = physics_rate + dark count_rate ≈ 600kHz per BiRO input

SuperB IFR electronics : APPENDIX B: estimates of number of channels, hit rates, triggered data bandwidth

outline of the IFR DAQ electronics: data bandwidth estimates WITH BINARY READOUT FOR ENDCAP

if we do L1 trigger matching on board

- **assuming a 150ns trigger window**
- **assuming that trigger matching is performed at the front end cards**
- assuming a "hit rate per scintillating element" of 600kHz per channel in the endcaps (500Khz of "physics" + 100KHz of dark count rate because in the endcap we can set a higher threshold w.r.t the barrel)
- assuming that an event from an "IFR_BiRO" board is built like outlined below:
  - Header = Board ID + Frame ID (allows to reconstruct ABSOLUTE timing for hit records) : 12 Byte
  - 8 samples within the trigger window for all 128 inputs → 8 * (128/8) = 128 Byte
  - Trailer = L1_Trigger_Data + WordCount + error code: 12 Byte

The "IFR_BiRO" event size and data rates can be estimated as follows:

<"IFR_BiRO" event size> = 12 + 128 + 12 ≈ **0.152kB**

and thus the "**trigger matched**" data rate produced by each "IFR_BiRO" is:

<"IFR_BiRO" data rate> = 150KHz * 0.152kB ≈ **22.8MB/s**

SuperB IFR electronics : APPENDIX B: estimates of number of channels, hit rates, triggered data bandwidth

outline of the IFR DAQ electronics: data bandwidth estimates WITH BINARY READOUT FOR ENDCAP

if we do L1 trigger matching on board

ENDCAP summary

- **Number of "IFR_BiRO"s = 75**

- Numbers per "IFR_BiRO" board:
  <"IFR_BiRO" event size> = 0.152kB
  <"IFR_BiRO" data rate> = 22.8MB/s
- Average event size for the whole Endcap read in binary mode:
  <Event size Endcap> = 0.152kB * 75 ≈ 11.4kB
- Total data rate produced by the Endcap:
  <Event data rate Endcap> = 22.8MB/s * 75 ≈ 1,710MB/s
- Tentative calculation of the number of links required (assuming the "concentration" of 5 "IFR_BiRO" output links into 1 link at 2Gbps):
  Number_of_data_links_endcap = 75 / 5 ≈ 16
  (i.e. 4 links per digitizer crate)