Status of SVT front-end electronics

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on behalf of INFN and University of Milan

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- DAQ reading chain for L0-L5
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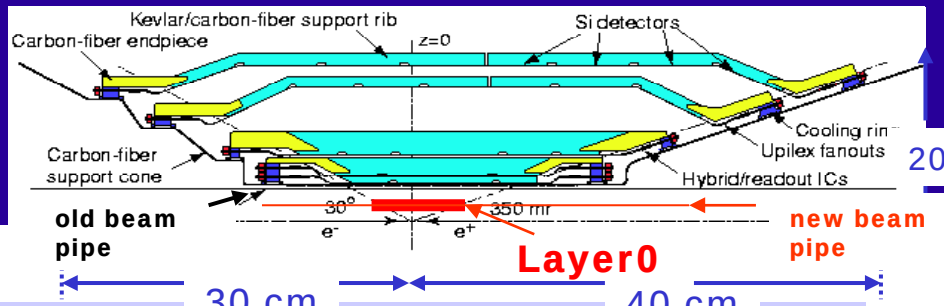
SVT System (1 of 2)



SVT Baseline for TDR

- Striplets in Layer0 @ R~1.5 cm → Triggered FE chips
- 5 layers of silicon strip modules (extended coverage w.r.t BaBar) → Triggered or data push FE chips

Upgrade Layer0 to thin pixel for full luminosity run

- more robust against background occupancy

Several progress on the baseline design in the last few months:

- Definition of the requirements for readout chips for striplets and strip:
  - Need to develop 2 new chips since existent chips do not match all the requirements : analog info, very high rates in inner Layers (0-3) & short shaping time, long shaping in Layers 4-5 to reduce noise for long modules.
  - Started to evaluate if readout architecture developed for pixel can be used for strips: no evident showstop up to now
  - First estimate of noise vs shaping time in each layer done: optimization still needed.

SVT System (2 of 2)

- Detailed study of striplets performance in high background (occupancy >= 10%) just started with Fastsim.
- Updated background simulation: Rates in strip layers 1-5 increased by a factor 3 after a bug was discovered, more checks ongoing. Layer0 was not affected.
- Clearer definition of requirements for Layer0 pixels

Physics:

- Resolution of 10-15 um in both coordinates
- Total material budget <= 1% X0
- Radius ~1.3-1.5 cm

Background (x5 safety included)

- Rate ~100-300 MHz/cm2 depends stronlgy on radius and sensor thickness
  - Timestamp of 1 us → 5-10 Gbit/s per module
- TID ~ 15Mrad/yr
- Equivalent neutron fluence: 2.5 10^{13} n/cm2/yr
  - Standard CMOS MAPS marginal

- Several options still open and under development → decision on technology in 2013
- Hybrid pixels: more mature and rad hard but with higher material budget
- CMOS MAPS: newer technology potentially very thin, readout speed and rad hardness challenging for application in Layer0.

Parameter Space

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Gangling/Occupancy/Simulations

Several unknowns: exact background rate; hit multiplicities

Trigger

frequency: 150 kHz (1.5 S.F)

jitter: 100 ns (the goal is to go down to 30 ns)

latency: 10 us (1.7 SF; LVL1 design is 6 us)

DAQ window: 100ns + 2 Time stamps

or 300 ns

Time stamping: 33 MHz (T(BCO)=30 ns)

Chip readout clock: 66 MHz (T(RDclk)=15 ns)

Hit rates from the last simulations

Assumptions:

Strip dead time equal to 2.4 peaking time

Strip rates as given by Riccardo Cenci (13/5/11):

New Values	(Old values)
L0: 2060 kHz/strip	
L1: 687 kHz/strip	(268 kHz/strip)
L2: 422 kHz/strip	(179 kHz/strip)
L3: 325 kHz/strip	(52.5 kHz/strip (?))
L4: 47 kHz/strip	(21.9 kHz/strip)
L5: 28 kHz/strip	(18.7 kHz/strip)

Efficiency vs peaking time

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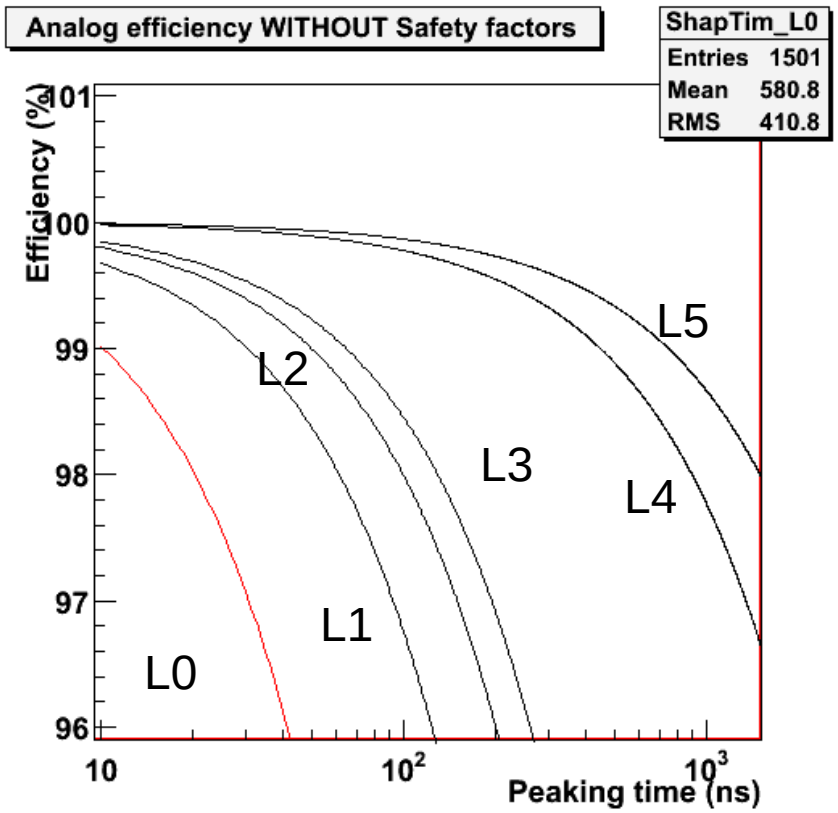
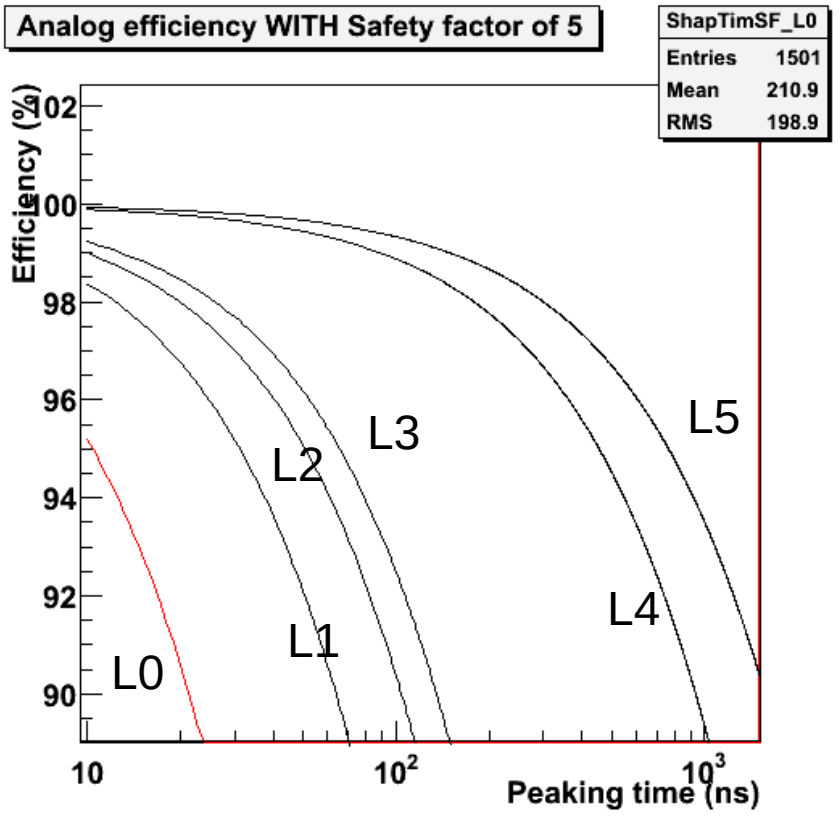
No safety factor



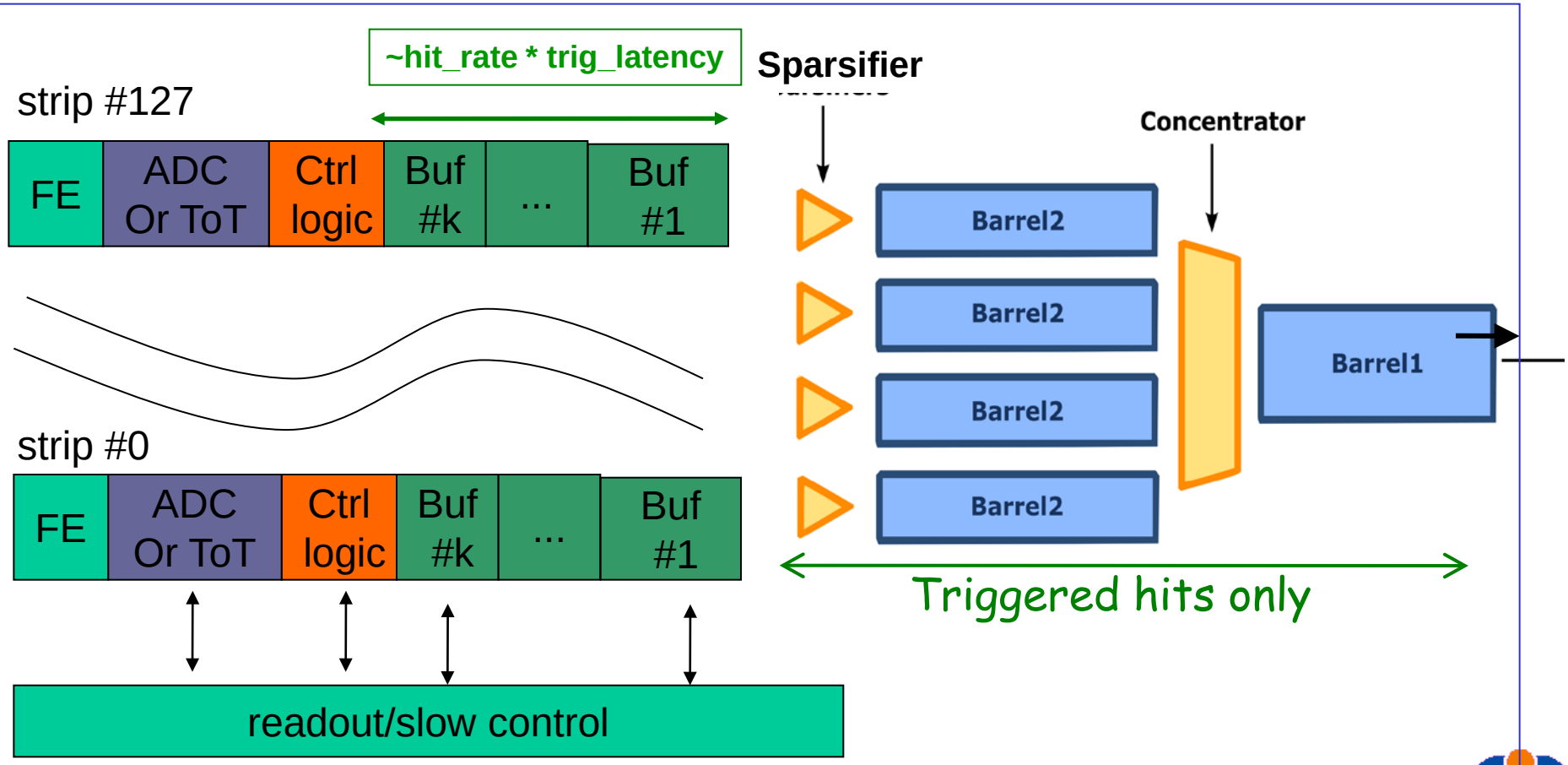
97.6% eff →Tp(L1)=74 ns

Safety factor of 5



97.6% eff →Tp(L1)=15 ns

Readout chip for strips



How many buffers?
How many barrels?

Asynchronous logic assumed

L1 simulation: 687 kHz/strip

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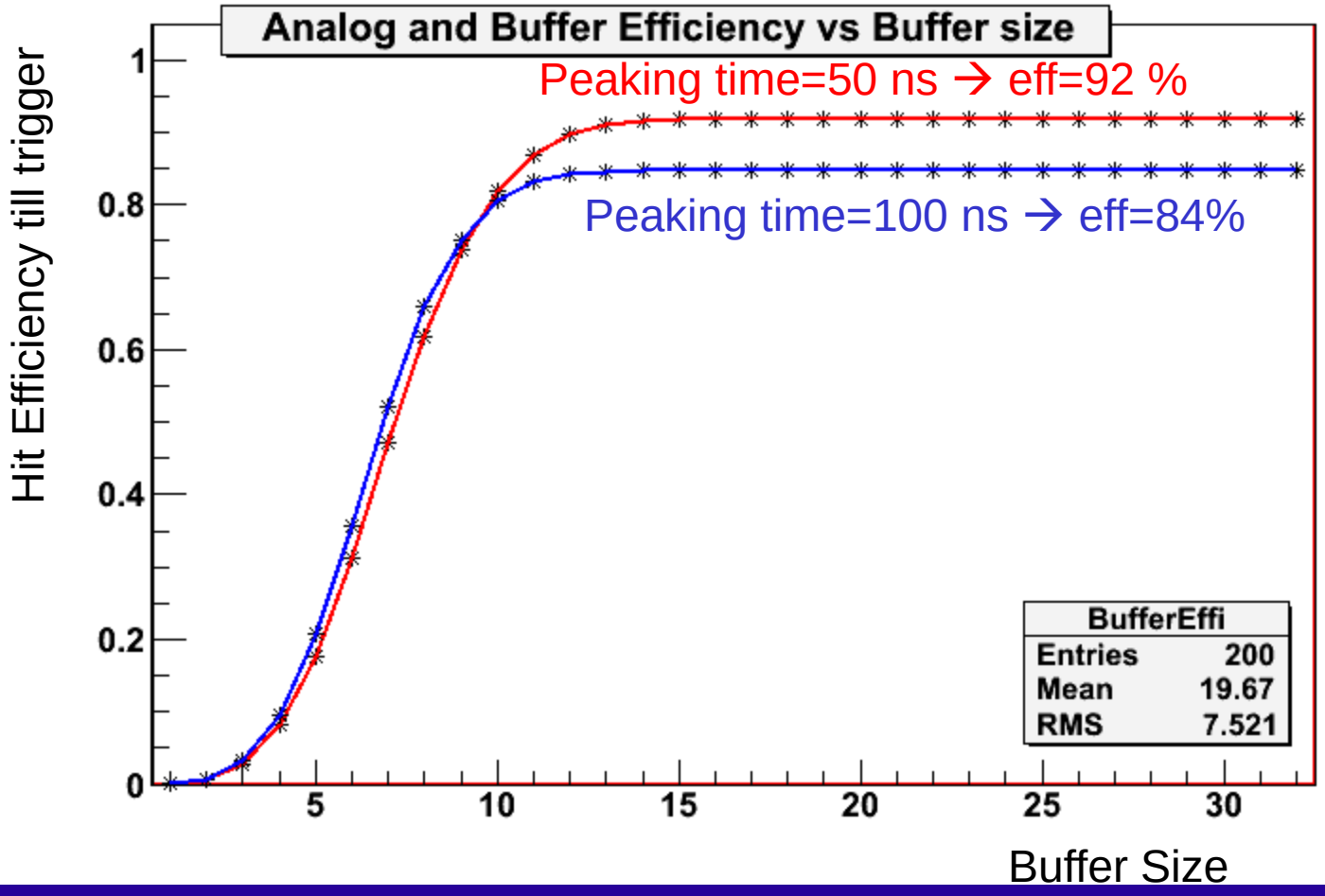
Analog efficiency and limited buffer lenghts

Single strip simulation



L4: 47 kHz/strip but longer deadtimes

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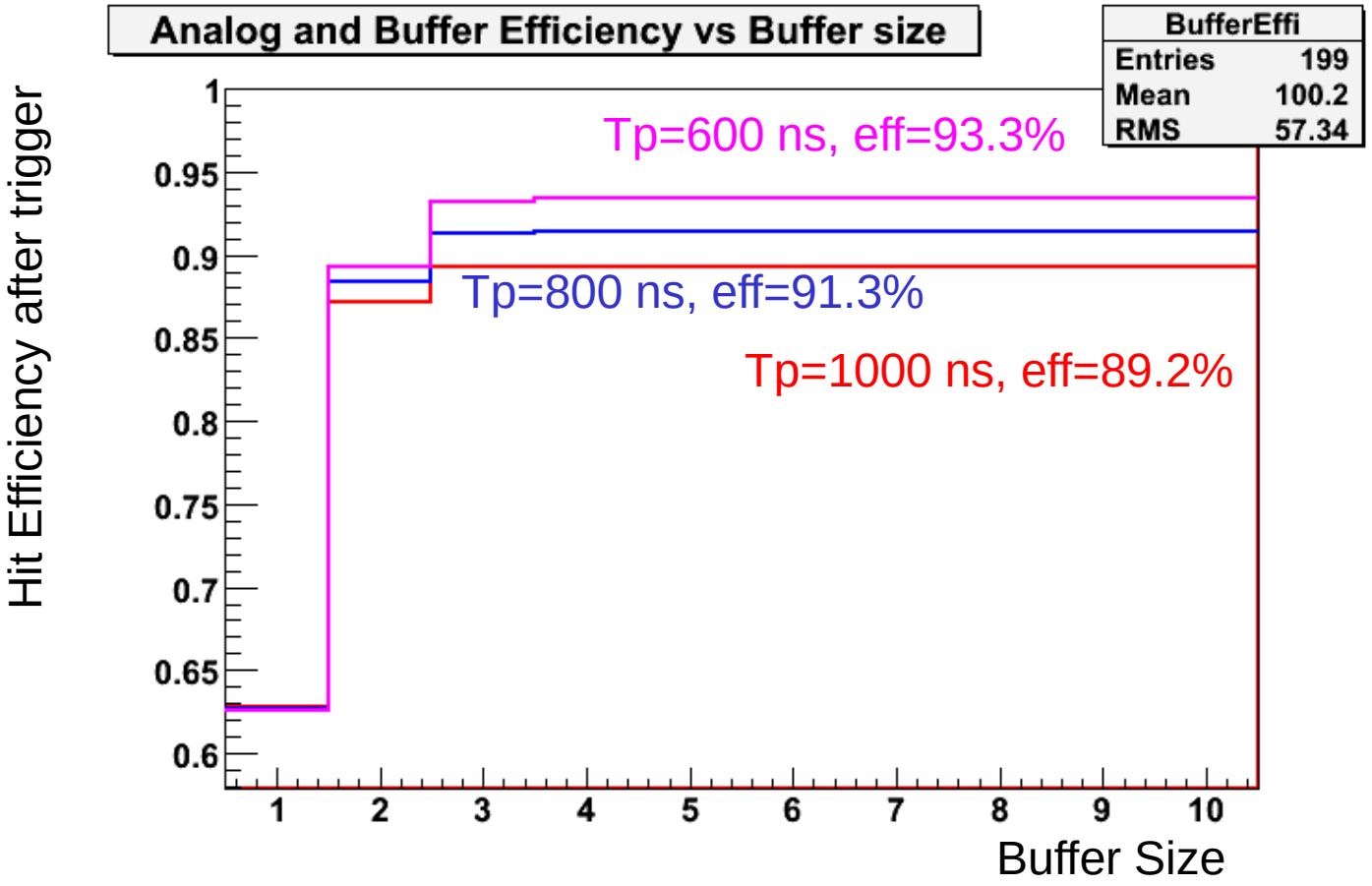


For outer layers (smaller hit rate) the buffer size is not a problem: 5 buffers/strip are enough. The dominant parameter is the analog dead time.

Efficiencies vs rate and dead times

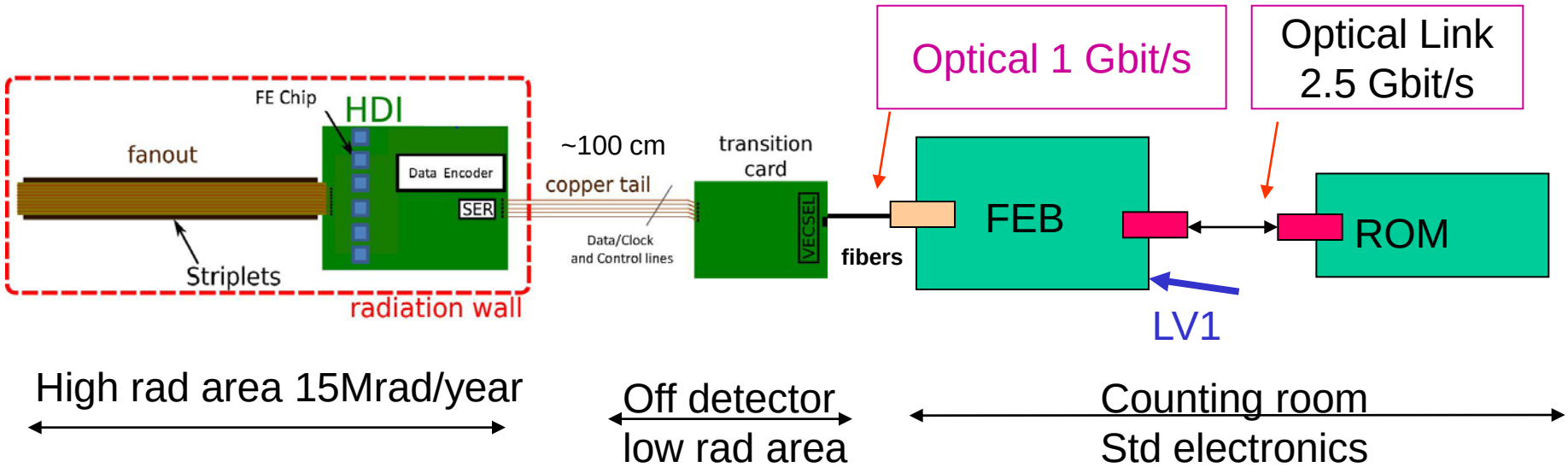
Layer	C_D [pF]	t_p [ns]	ENC from R_S [e rms]	ENC [e rms]	Hit rate/strip [kHz]	MMC Efficiency
0	11.2	25	220	680	2060	(0.732)
1	26.7	50	650	1190	687	0.917
		100	460	930		0.841
2	31.2	50	830	1400	422	0.948
3	45.8	50	1480	2130	325	0.960
4	52.6	1000	340	820	47	0.893
5	67.5	1000	500	1010	28	0.934

Conditions: 20 buffers, 150 kHz trigger rate, 300 ns time window for all layers.

DAQ reading chain for L0-L5

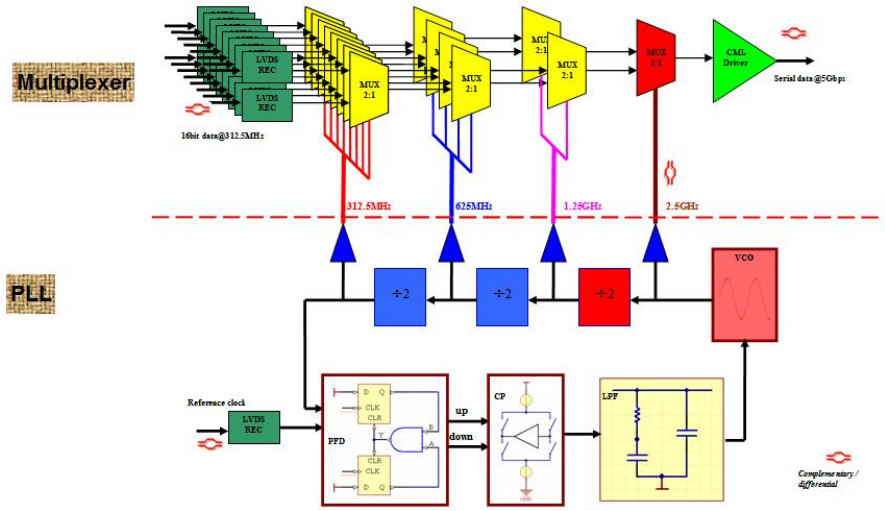
DAQ chain independent on the chosen FE options

HDI +Transition card+FEB+ROM



HDI and transition card design is ongoing
Data Encoder IC .... Specs are under discussion
Rad-hard serializer to be finalized
→ looking into a low power/low speed version
Copper tail: lenght vs data transfer are under study
FEB + ROM as before

Low Speed / Low Power Serializer



The block schematic of the SMU LOC1 shows that the typical power of the chip (~ 500 mW at 5 Gbps) has a substantial contribution coming from the PLL circuit.

A “Tunable” Serializer (data rate from 2.5 to 5 Gbps) can be obtained by changing the PLL.

The goal is to reduce the power to ~ 250 mW at 2. 5 Gbps

Simulation results indicate that (courtesy of SMU) :

	LOCs1 (mW)	low power design
CML Driver	96	50%
PLL	173	80%
Others	187	30%

The final design/prototyping phase of this Low Speed /Low Power IC did not start, yet.

SMU has received expression of interest by other experiment for such a development

SMU is looking into opening a collaboration on such IC (technology is 0.25 um Silicon on Sapphire)

Data/Clock and Control Cables (1 of 2)

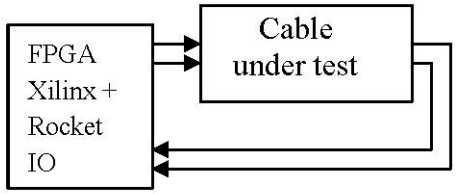
Kapton tail is probably not a solution for SuperB

- data speed is much higher than before
- differential/coaxial lines are not usually designed in flat circuits

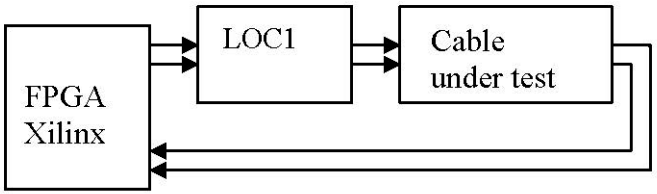
Some small and flexible cables have been selected and tests are on-going

Some preliminary results are shown

- the reference lenght has been chosen ~ 1m (not to push on driving capability of devices)
- the test has been performed using
  - Xilinx FPGA + Rocket IO as a reference
  - Xilinx FPGA + LOC1 serializer as a comparison

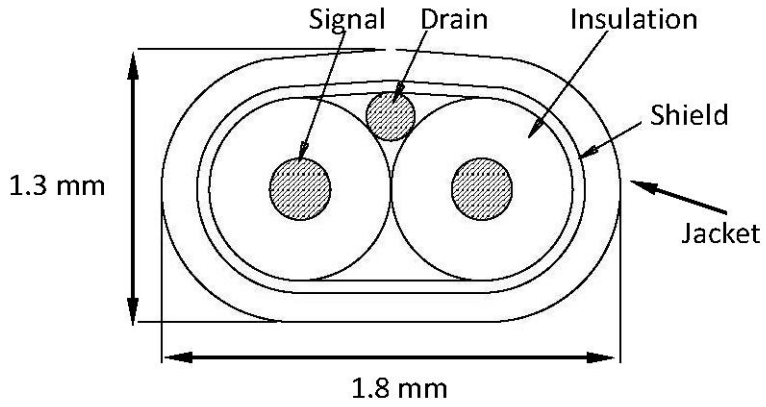


Configuration 1



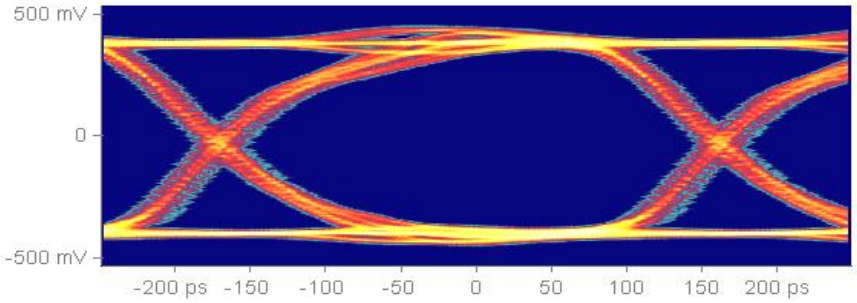
Configuration 2

Data/Clock and Control Cables (2 of 2)

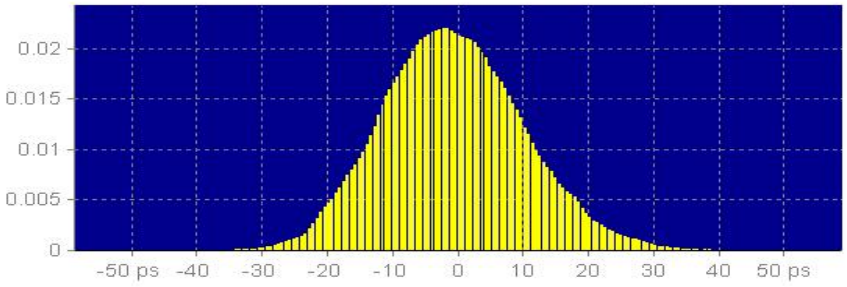


Signal: 30 AWG, Solid Copper Clad Aluminum
Differential Impedance ~ 100 Ohms +/- 5%
Capacitance: 16 pF / ft
Propagation Delay: < 2 ns/ft

The preliminary measurements show that LOC1 can drive such a cable without substantial degradation even without pre/post emphasis

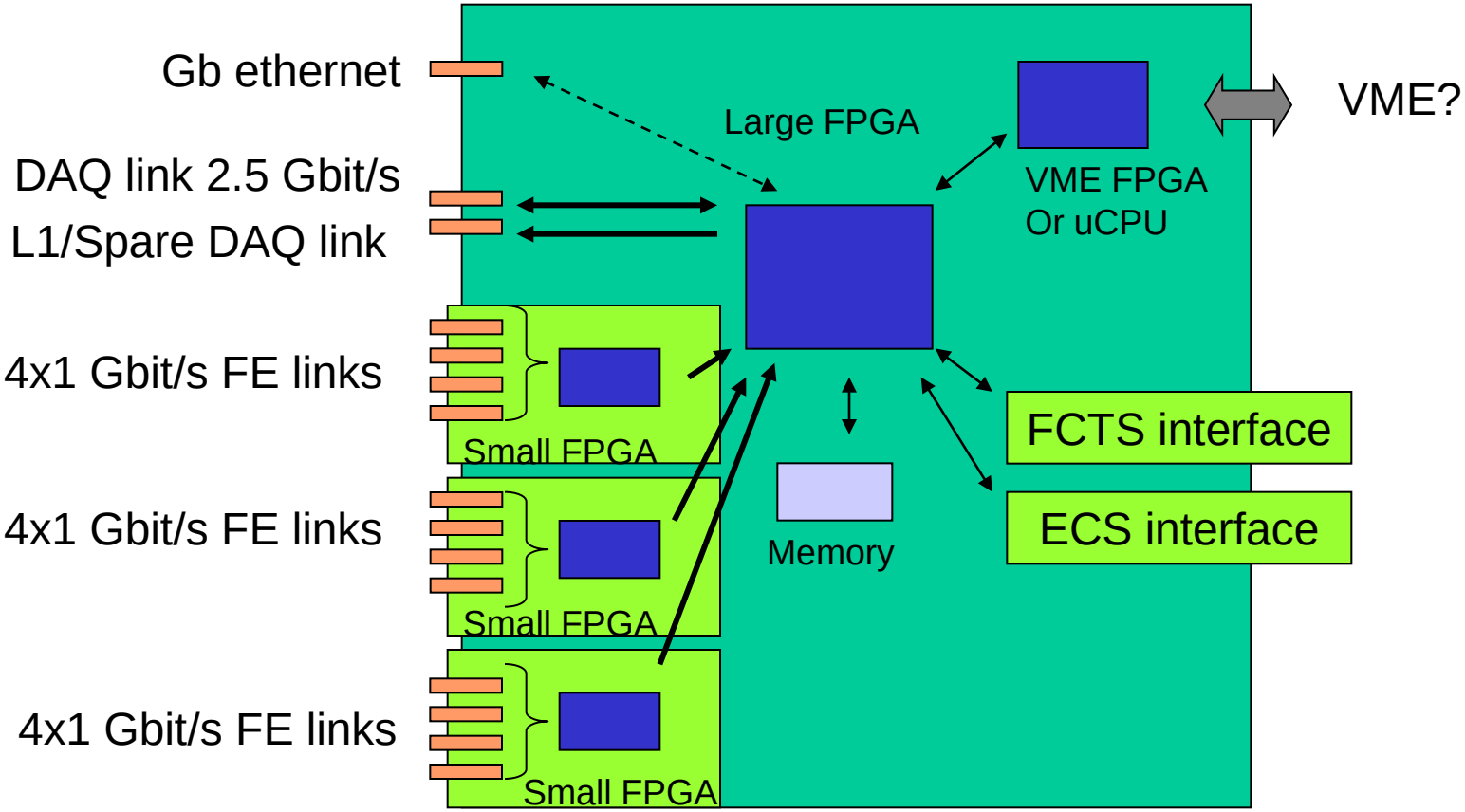


Eye diagram



BER probability density function

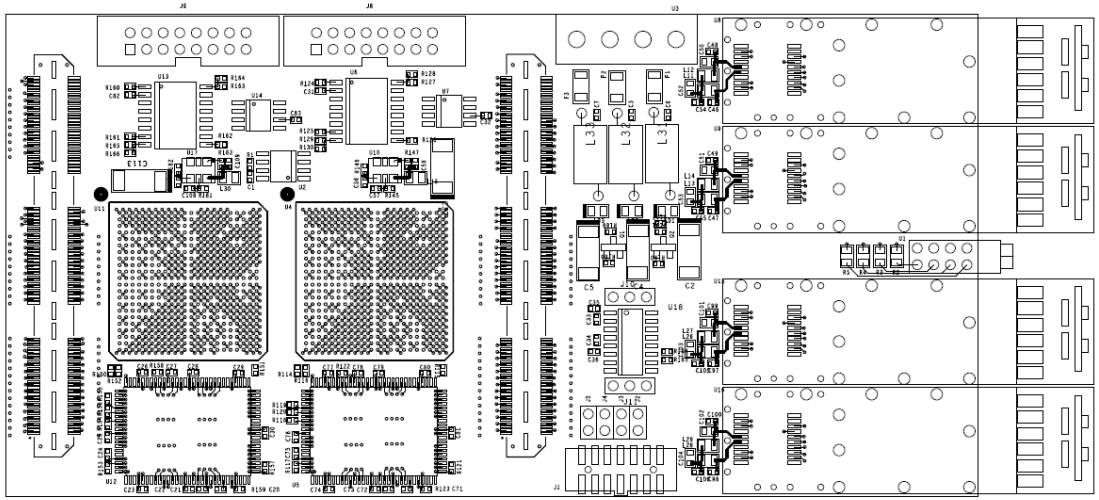
SuperB-FEB Board schematics



FCTS, ECS protocols to be decided experiment-wide
Large FPGA for data shipping and monitoring
VME FPGA or uCPU might be included in the large FPGA.

Optical link mezzanine card for EDRO

Developed as a part of ATLAS/FTK project



4 optical links at 1 Gbit/s; FPGA Xilinx, 40/100 MHz clk (programmable)

PCB realized; now mounting components on first prototype

Usable as link test mezzanine in SuperB (fall 2011)

Data Chain …. locations

HDI	Located near the detector
Transition cards	Located approximately ~ 1 m from the HDI in a “not too hostile” environment. →We will try to maximize such a distance → Receivers and electrical to optical transition will be located on this card. It is an advantage to go further away form the detector.
DAQ	Located after the so called "radiation wall“ .... For L1-L5 layers are needed ~ 120 optical links, equivalent to ~ 20 boards (each board will have up to 12 optical links) L0 layer ..... Still to be addressed

Conclusions

First core of a Mini Monte Carlo for the Strip readout chip is available, containing

- Hit and trigger generation
- Analog inefficiency, buffers and barrels
- Several improvements can be foreseen: input hit multiplicities and correlations, etc

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Good indications that for L1 the pixel readout architecture can be reused fruifully

Two parameters were found to be (very) critical:

- T(BCO) vs T(RD)
- Analog dead time

Analysis on other layers foreseen

Data chain is progressing by defining all the elements of the chain ....


SuperB

Strip chip: how many barrels ?

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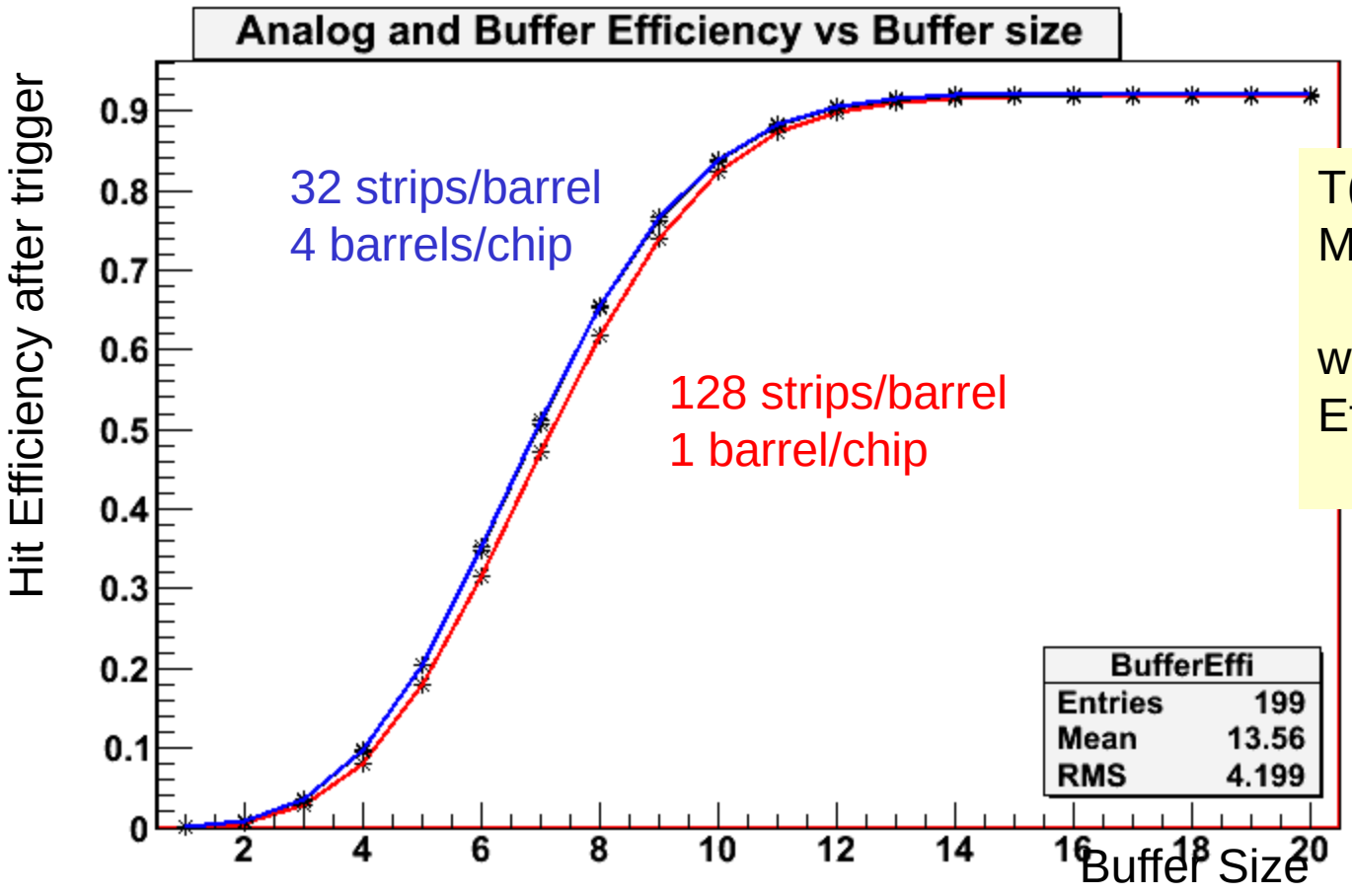
Peaking time=50 ns



T(BCO)>2T(RD)
Mandatory!

when T(BCO)=T(RD)
Efficiencies at zero

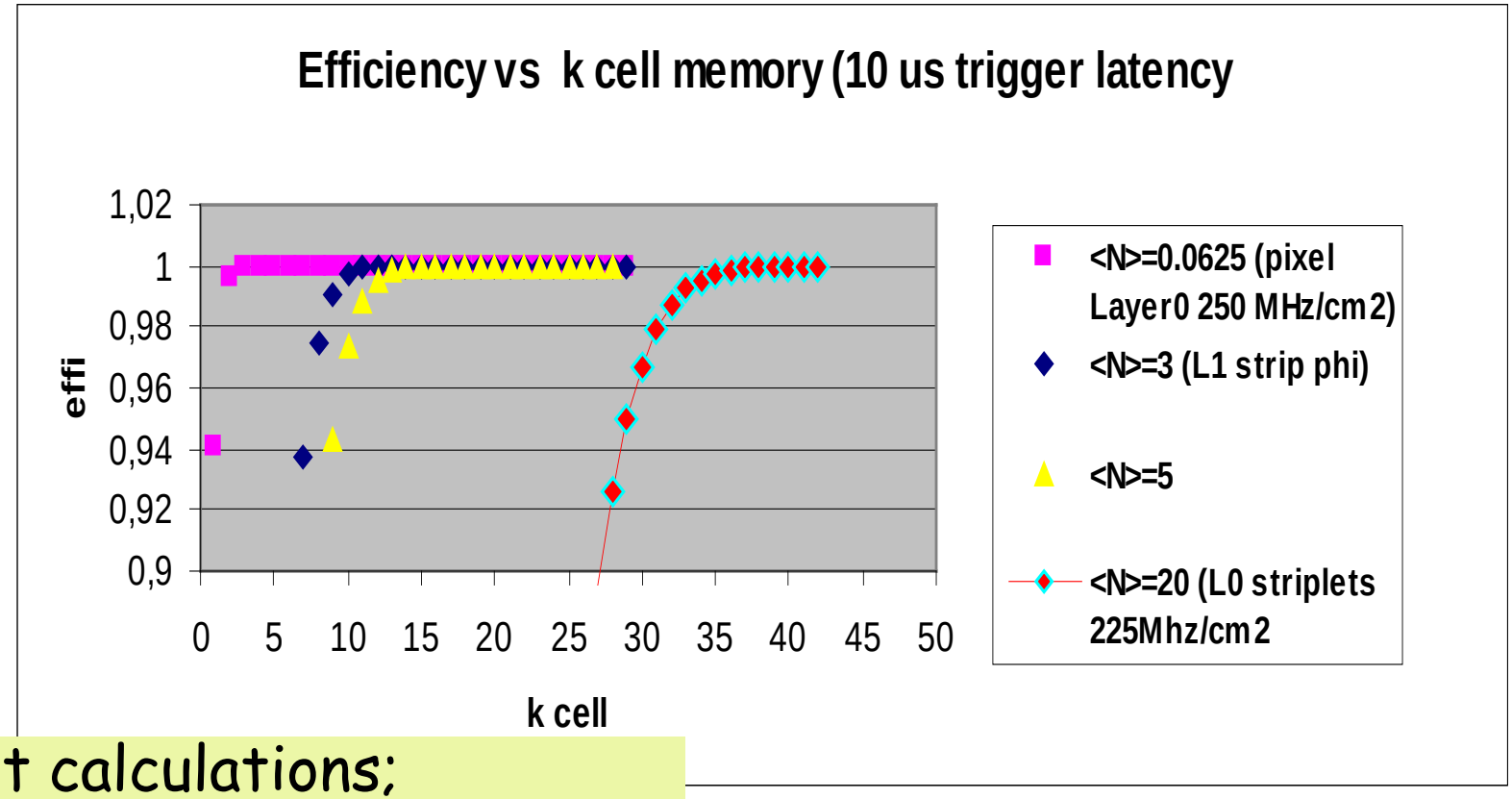
150 kHz trig rate
300 ns DAQ
time window

One or few barrels seem enough!

Number of buffers required for L0 striplets/L1 strip (preliminary)

Assume L0 @ 225 MHz/cm2, L1@5 MHz/cm2

L0 = 2 MHz/strip, L1=270 KHz/strip



Just calculations;
Mini-MC simulation needed

F. Morsani/G. Rizzo