DCH FEE

28 chs DCH prototype FEE instrumentation update

&

some remarks on the use of SRAM based FPGA in DCH DAQ chain

G. Felici

Outline

- DCH prototype front-end and HV distribution
  - Requirements
  - 28 channels DCH prototype front-end & HV distribution boards assembling
  - Preamplifier board features
- Readout chain implementation - Some consideration on programmable devices
  - VirtexQ & Actel ProAsic comparison
  - Implementation of 1 ns resolution TDC on a ProAsic3E device
- Cluster Counting update
  - Cluster Counting scenarios – pros & cons
  - Derivative circuit – Simulation result examples
- DCH front-end power requirement & location
- Conclusions

DCH prototype front-end & HV distribution

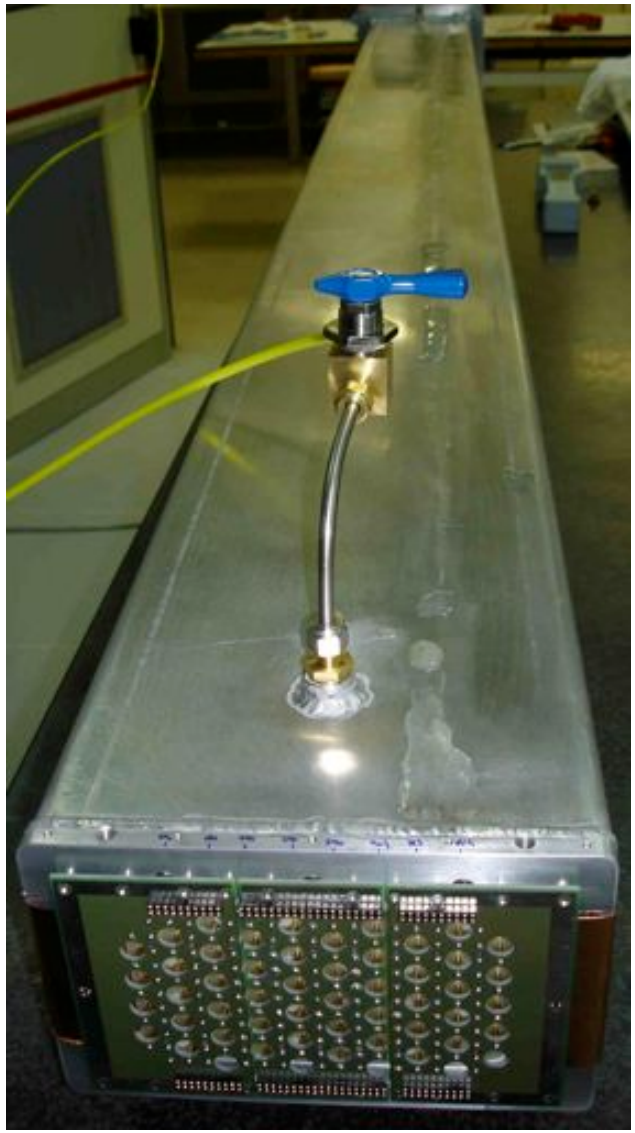
28 chs DCH prototype FEE

Signal amplification requirements

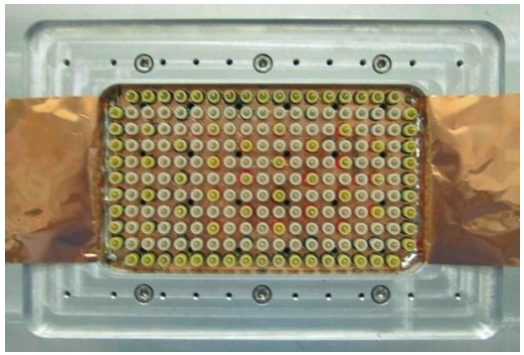
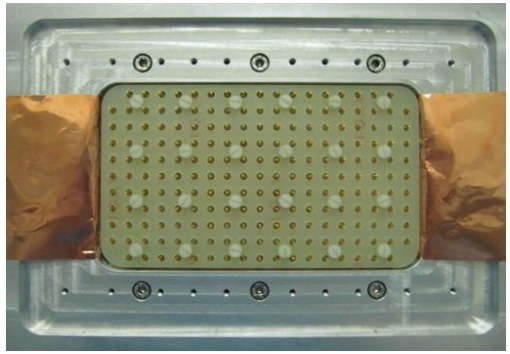
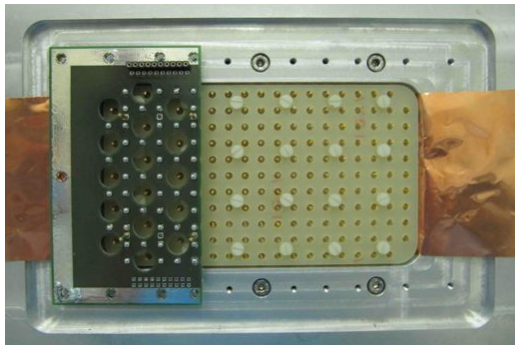
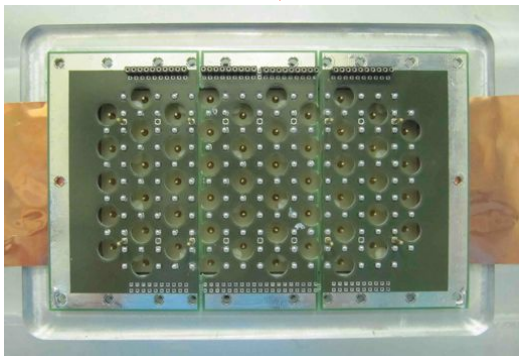
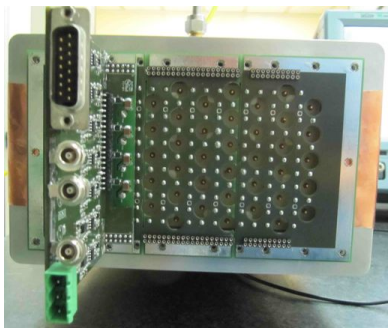
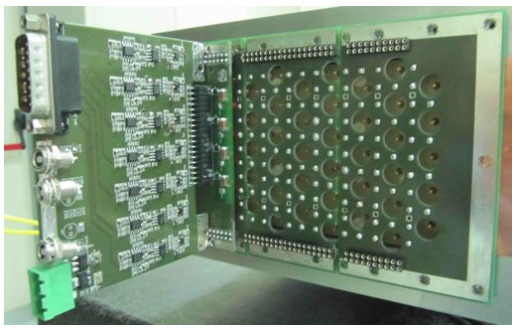
- BW ≥ 250 MHz
- Amplification ≥ 5 mV/fC
- Noise < 2000 erms

On Detector FEE boards

1. Feedthrough lock board (2 boards required)
2. Field wires GND boards (2 boards required)
3. HV distribution board (1 board required)
4. Signal extraction (decoupling & protection) board (1 board required)
5. Preamplifier board (1 board required)

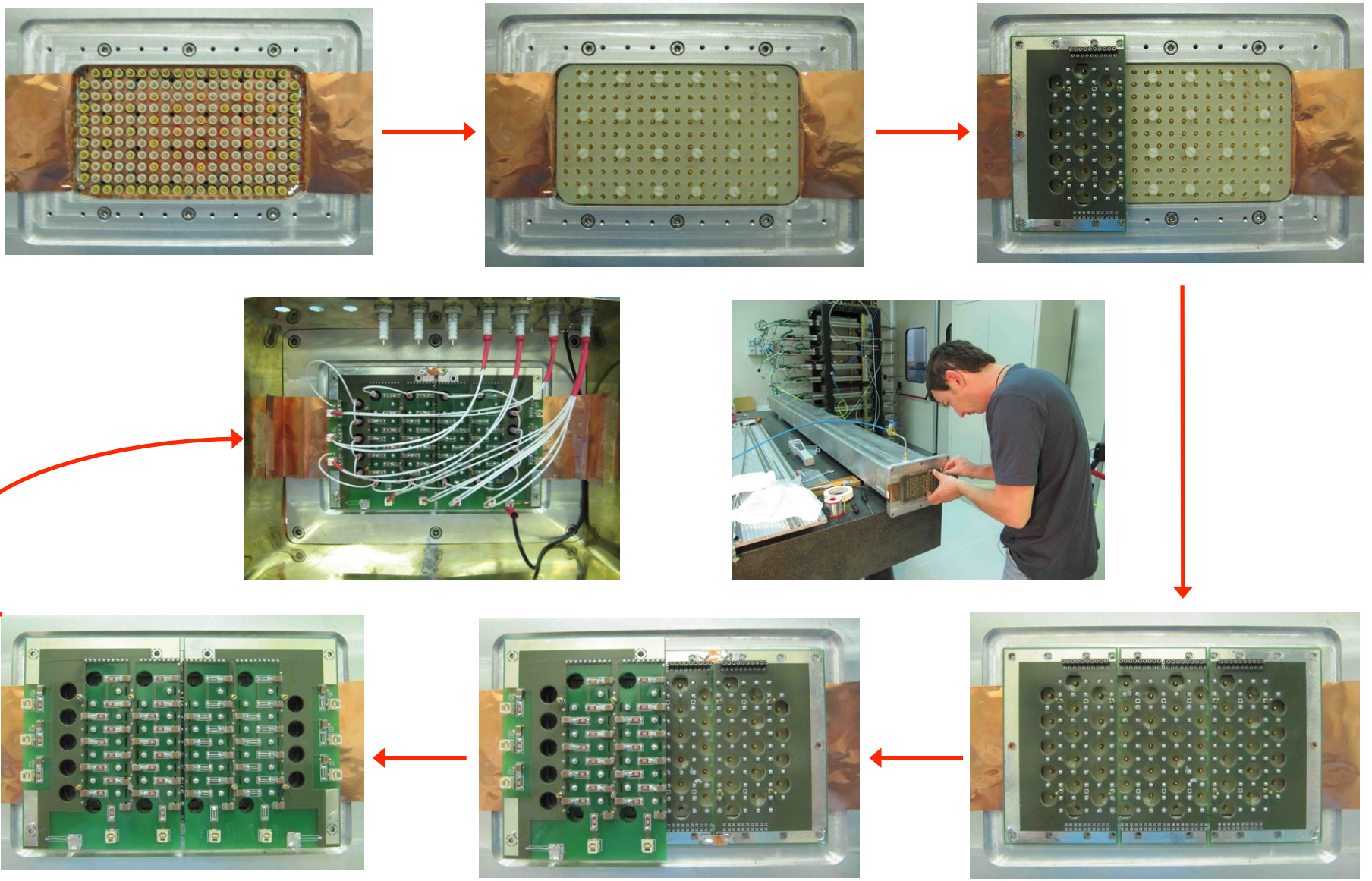


28 chs DCH prototype - FEE side

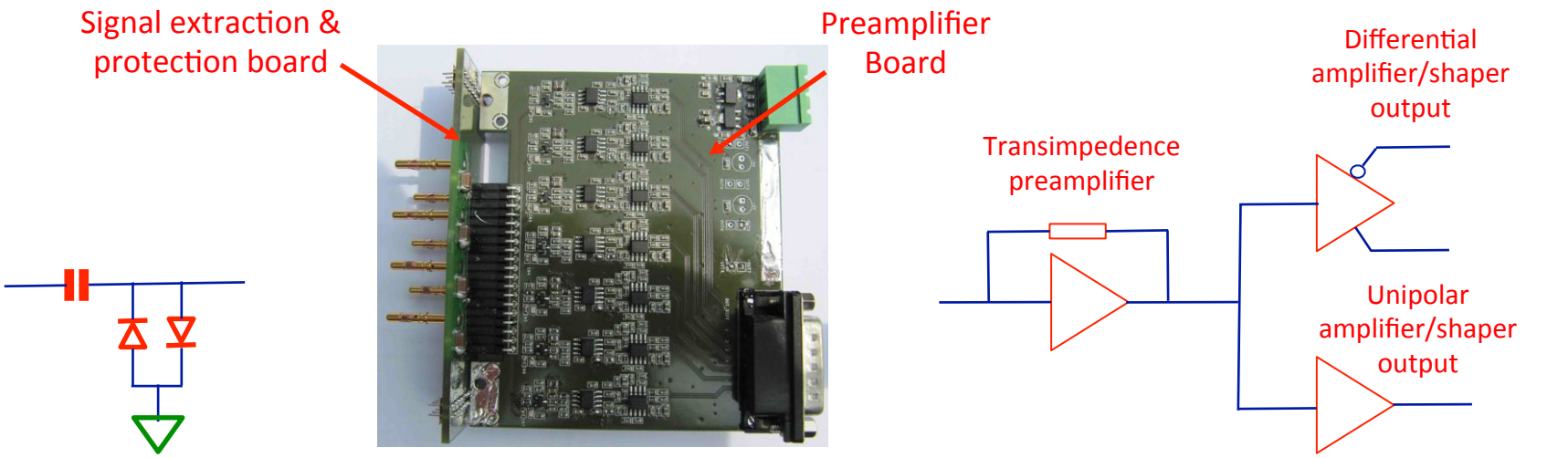







- Front-End side FC design is in progress
- Test will start as soon as FC will be available (≈ 2 week)

28 chs DCH prototype HV side

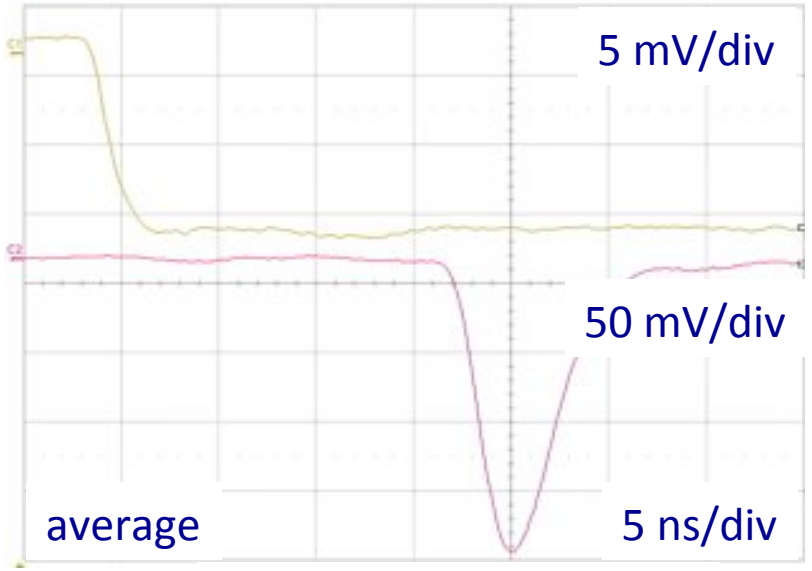


28 chs DCH preamplifier board main features



Preamplifier main features

- Number of channels : 7
- Zin ≈ 60 Ω
- Gain ≈ 8.8 mV/fC
- Noise ≈ 2500 erms @ 250 MHz BW
- Rise time ≈ 2.4 ns
- Unipolar & Differential outputs (50 Ω – 110 Ω)
- Test input
- Supply Voltage : + 7V (310 mA) - 7V (190 mA)
- Power Dissipation : 490 mW/ch



1.8 pF injecting capacitance

Readout chain implementation

Some remarks on programmable devices

SRAM & FLASH based FPGA devices (I)

- DCH readout chain is supposed make large use of programmable devices
  - Up to now DCH standard readout chain simulation has been implemented using SRAM based devices (Virtex5 FPGA)

- SRAM based devices are very flexible and powerful but unfortunately they are sensitive to single-event transients (SETs), and SEUs (FPGA user-programmed functionality relay on data stored in device configuration latches) .

- A radiation hardened family (virtexQ) is available, but costs are prohibitive for large production.

- Scrubbing (configuration and block-RAM) techniques allow to mitigate radiation effects and could be used in DCH readout chain but background radiation level should be foreseen with a good accuracy and complexity of design increase.

- Alternative solution using FLASH based devices (ACTEL ProAsic devices) could be used.
  - These devices are less susceptible to “firm errors”, while “soft errors” can be corrected by means of standard mitigation techniques (triple modular redundancy).
  - Unfortunately features of these devices (in terms of clock frequency and resources) are not comparable with Virtex5 or 6 devices, then a study to verify the possibility of implementing a 1ns resolution TDC based on 4xOversampling technique has been started.

Xilinx Aerospace Products

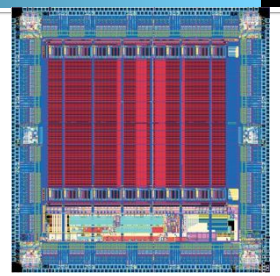
- Virtex-4 QPro V-grade
  - Total-dose tolerance at least 250 krad
  - SEL Immunity up to LET > 100 MeV/mg-cm²
  - Characterization report (SEU, SEL, SEFI): http://parts.jpl.nasa.gov/docs/NEPP07/NEPP07FPGAv4Static.pdf
- Expensive ☹, but reprogrammable ☺

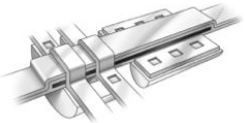
2/6/2009 R2E Radiation School: SEU effects in FPGA

Csaba Soos
PH-ESE-BE

SEU effects in FPGA How to deal with them?

Actel ProASIC3 FPGA





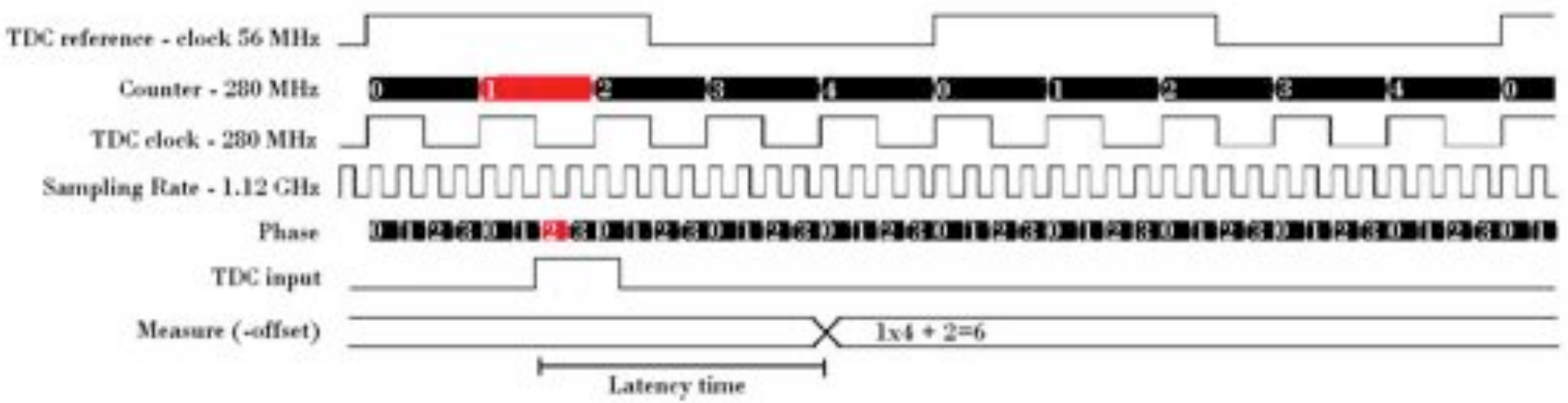
- Flash-memory based configuration
- 0.13 micron process
- SEL free[1]
- SEU immune configuration[1]
- Heavy Ion cross-sections (saturation)
  - 2E-7 cm²/flip-flop
  - 4E-8 cm²/SRAM bit
- Total-dose
  - Up 15 krad (some issues above)
- Not expensive ☺ and reprogrammable ☺

Note 1: Tested at LET = 96 MeV/mg-cm²

2/6/2009 R2E Radiation School: SEU effects in FPGA 36

Radiation-Tolerant ProASIC3 FPGAs Radiation Effects: http://www.actel.com/documents/RT3P_Rad_Rpt.pdf

Implementation of 1ns resolution TDC on a ProASIC3E device



- Simulations show it is possible to implement a 4xOversampling – 1ns time resolution TDC

- Caveat
  - No radiation mitigation technique can be applied to PLLs and (probably) to the high frequency section of 4xOversampling TDC
  - FPGA internal resources could be not enough to manage data conversion & feature extraction for an acceptable number of channels.
  - At the moment no Ser-Des are available

lorenzo.iafolla@lnf.infn.it

Cluster counting

Cluster counting scenarios: Pros & Cons

Concerning CC we have identified 3 possible scenarios:

1. FADC@1GHz + local features extraction (i.e. arrival time of individual clusters)
2. FADC@1GHz + data links and remote features extraction
3. Analog derivative method + local feature extraction

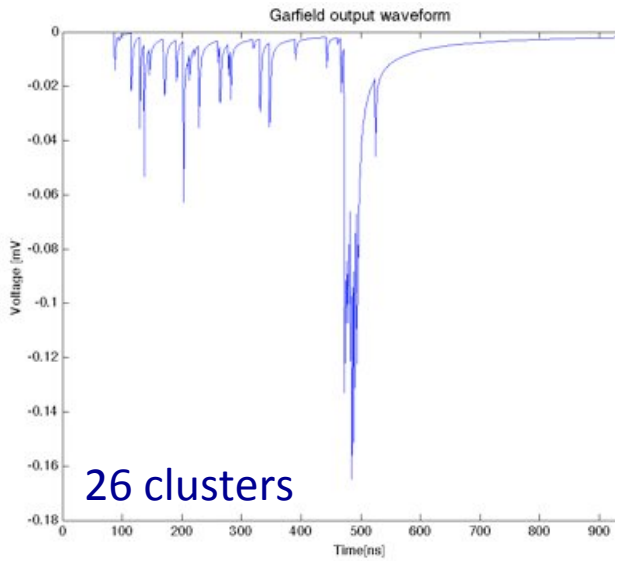
Pros:

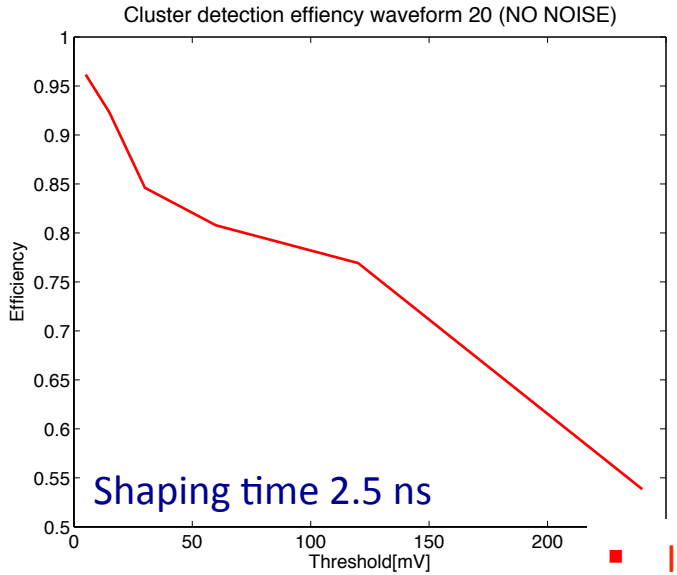
- Scenario 1 & 2 allow a better control of signal noise then allowing a better clusters detection
- Scenario 3 can be easily integrated in the standard RO chain also using Flash based FPGA

Cons:

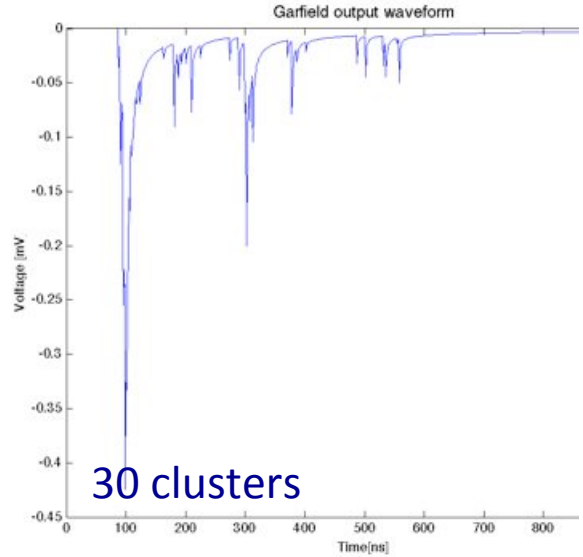
- Scenario 1 requires the development of fast algorithms implemented in firmware and high performance devices (i.e. Virtex 7 or similar) to process data, while scenario 2 requires a huge BW to transfer acquired data (= 1.2×10^{12} bits/s). Both scenarios require powerful (SRAM based) FPGA to manage data the huge amount of data. Unfortunately (relatively) low cost devices are sensitive to radiation background.
- Analog derivative based measurement is strongly dependent on signal S/N ratio

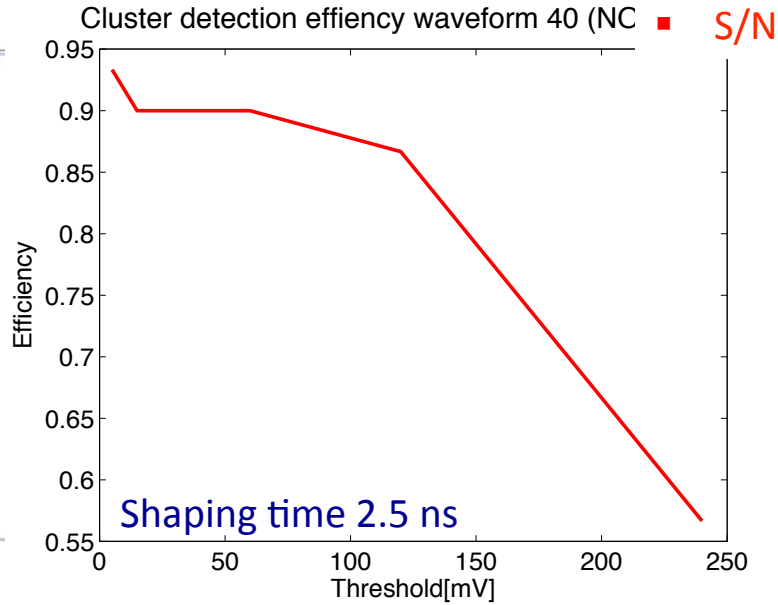
Analog derivative method applied to Garfield data – a couple of samples without npise



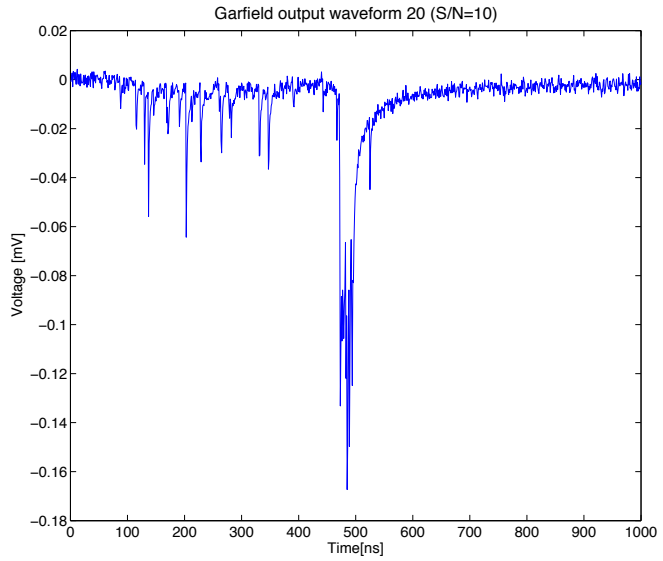


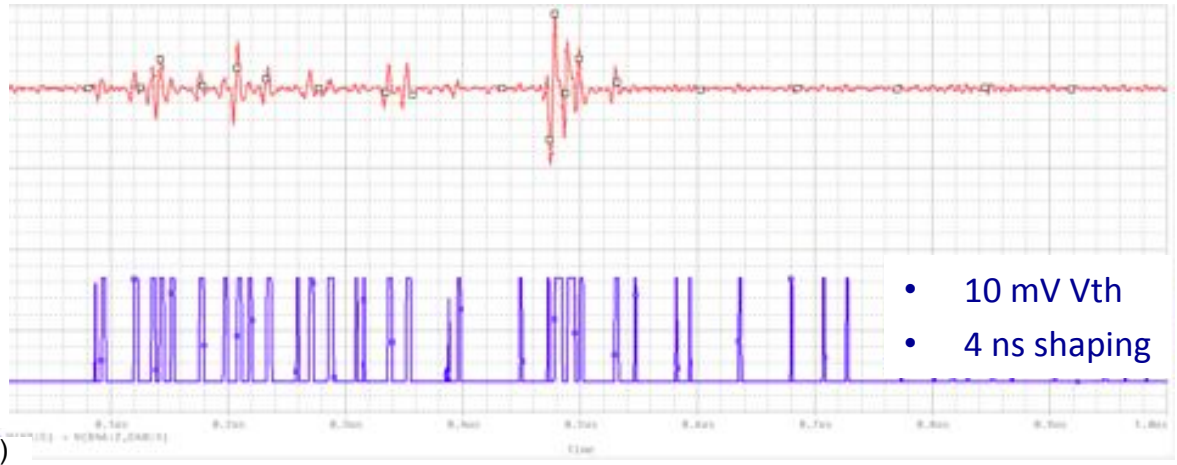
- Impact parameter = 2.5 mm
- S/N = ∞



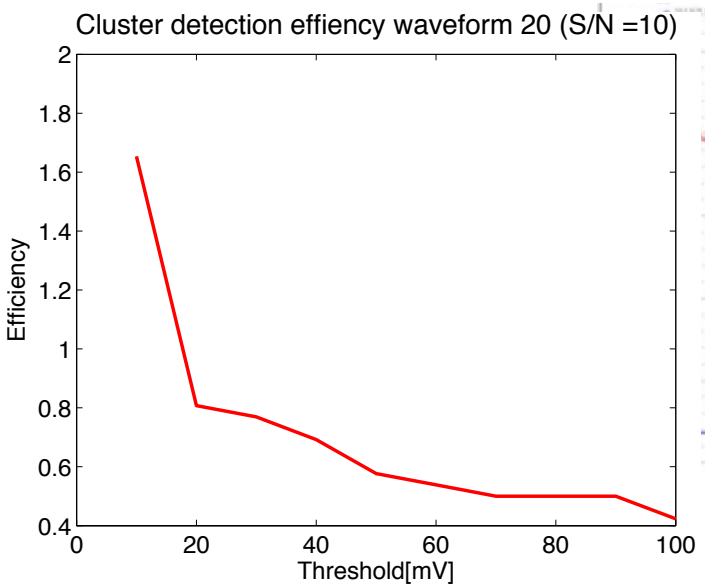


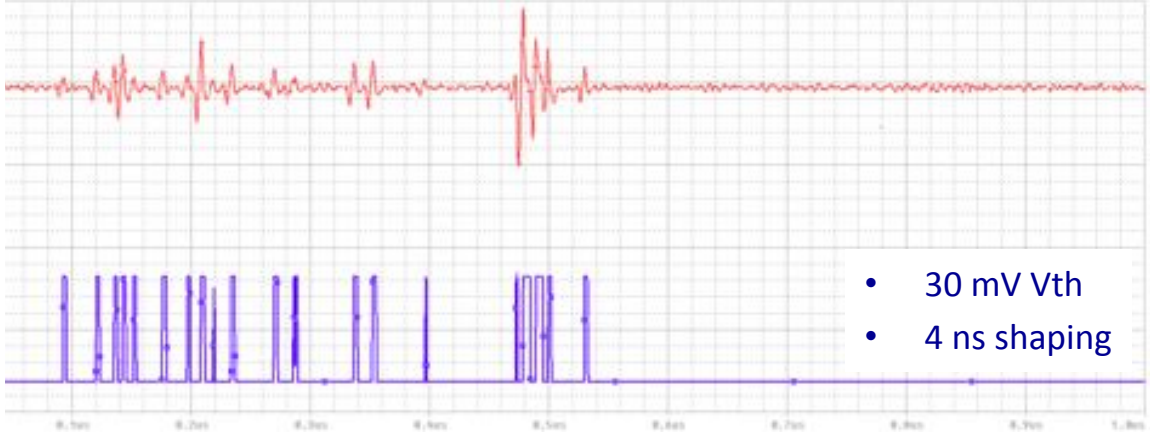
Analog derivative method applied to Garfield data – a couple of samples WITH noise (I)





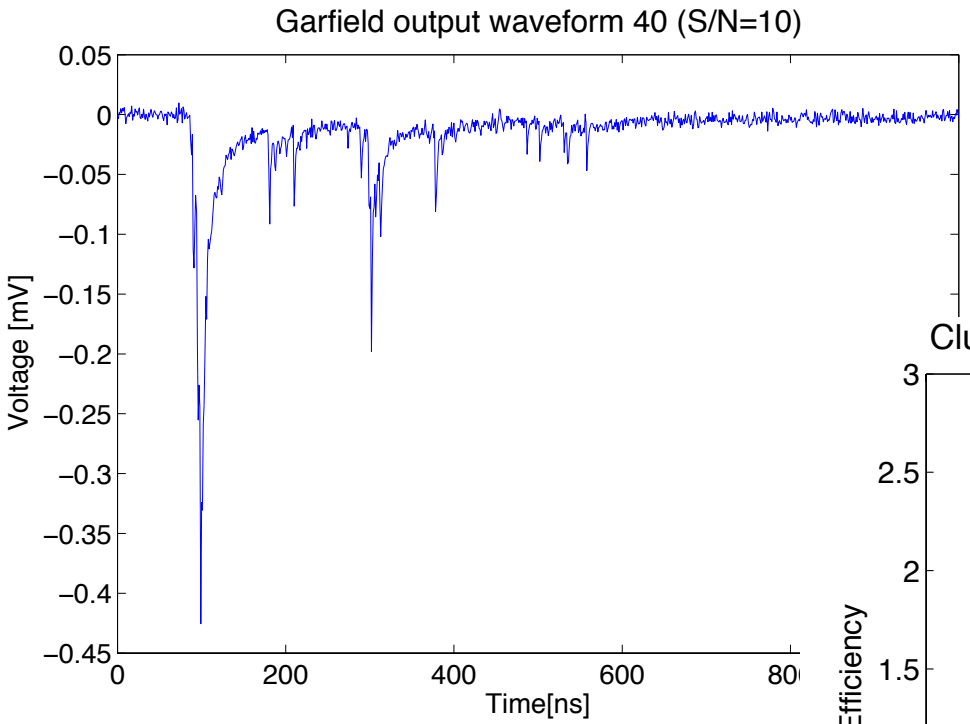
- 10 mV Vth
- 4 ns shaping

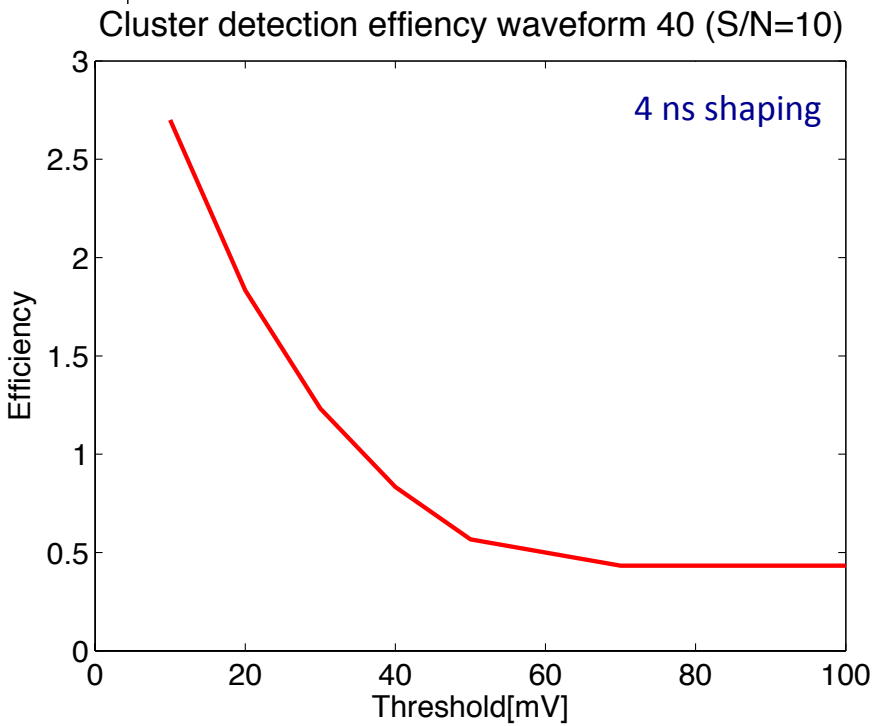




- 30 mV Vth
- 4 ns shaping

Analog derivative method applied to Garfield data – a couple of samples WITH noise (II)





DCH front-end power requirement & location

DCH front-end power requirement estimate

Background

- Drift Chamber FE design has not be finalized (CC option)
- HV distribution and VEFB boards should be assembled on the DCH end-plates
- Off-detector electronics should be located just outside the detector (minimize cable length)
- HV/LV power supply should be located not too far from detector unless we choose (expensive) devices developed for hostile area

BABAR experience

- Front-End Assemblies : 1300 W
- Data I/O Modules : 100 W
- Trigger I/O Modules : 260 W

NB : BABAR good results in PD due to development of ASIC devices

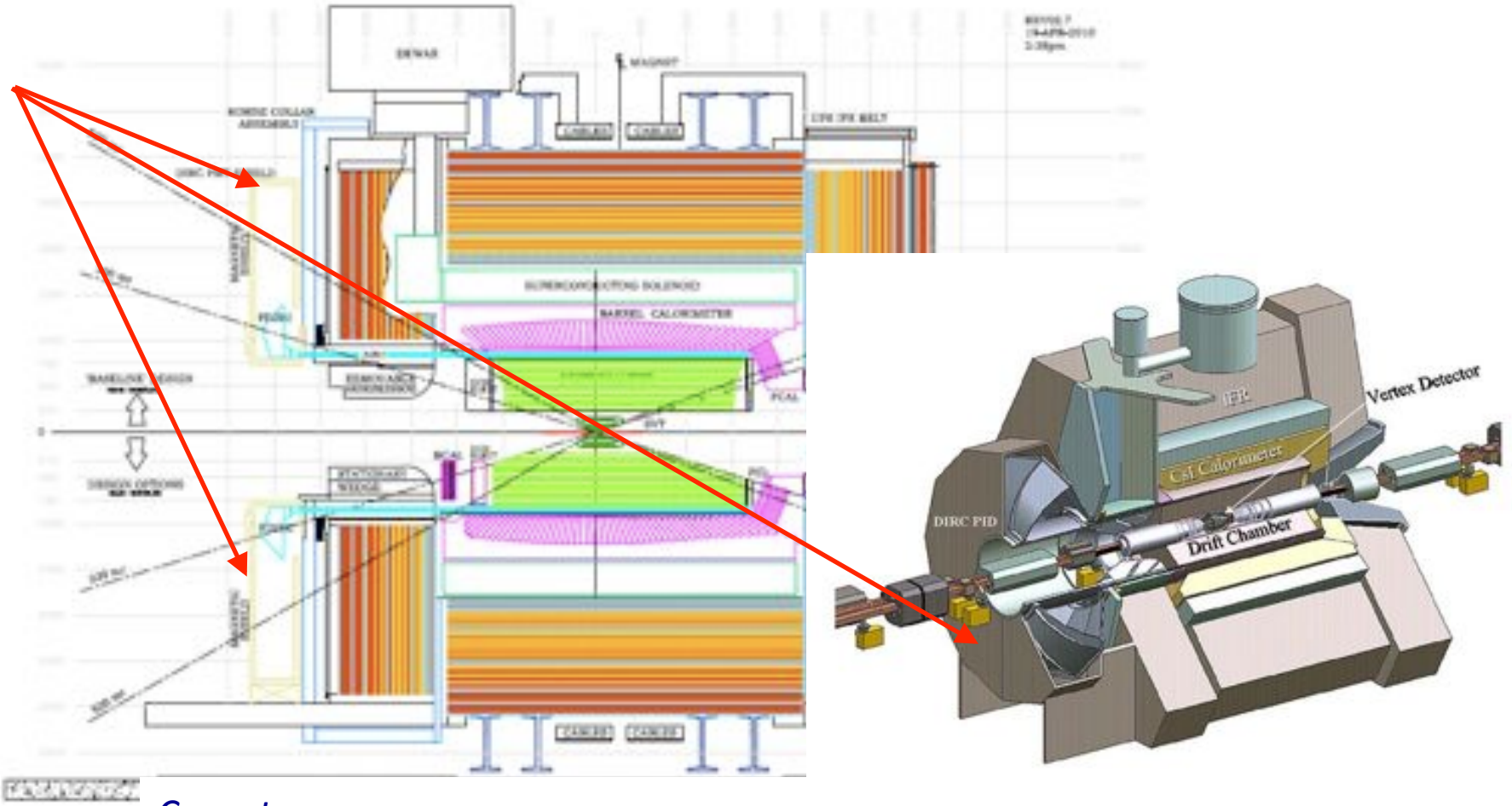
SuperB power requirement estimate

- VFEB ≈ 40 mW/ch → 400 W
- Off-Detector power requirement
  - Conventional RO chain ≈ 400 mW/ch → 4kW
  - CC RO chain : hard to tell .. probably both on-detector and off-detector FE will require dedicated circuits to avoid prohibitive system PD (to give an example a dual channel 1 GHz ADC from National consumes about 1.6 W @ 1.8 V while a Virtex5 device typically requires 1.7 mA/MHz (it was 3.74 mA/MHz for Virtex4)

DCH front-end power requirement location

Location

- On-detector : DCH end-plates (support structure required)
- Off-detector : as close as possible to the detector to avoid long cables (SOB ???)



Caveat

- SOB are tied to the flux return iron then they move when opening the detector

Conclusions

- In the past two months the LNF front-end activity has been mainly devoted to instrumentation of the new 28 channels chamber prototype.
- Several boards have been developed including a seven channels preamplifier board for Cluster Counting measurements whose main features are a gain of ≈ 9 mV/fC and a noise of ≈ 2500 erms @ 250 MHz BW.
- At the mean time a study to verify the feasibility of using FLASH based FPGA to implement the standard readout system (NO CC) is going on. In particular we are trying to implement with that device a 1 ns resolution TDC that is the most demanding part of the system (TDC has already been successfully implemented using a Xilinx Virtex5 device).
- Concerning CC we have identified 3 possible scenarios:

  1. FADC@1GHz + local feature extraction (i.e. single cluster arrival time)
  2. FADC@1GHz + buffers and remote feature extraction
  3. Analog derivative method + local feature extraction

  Scenario 1 or 2 allow a better control of the S/N ratio but feasibility must be verified with respect to background radiation and power dissipation
- An (very preliminary) estimation of power dissipation has been also shown