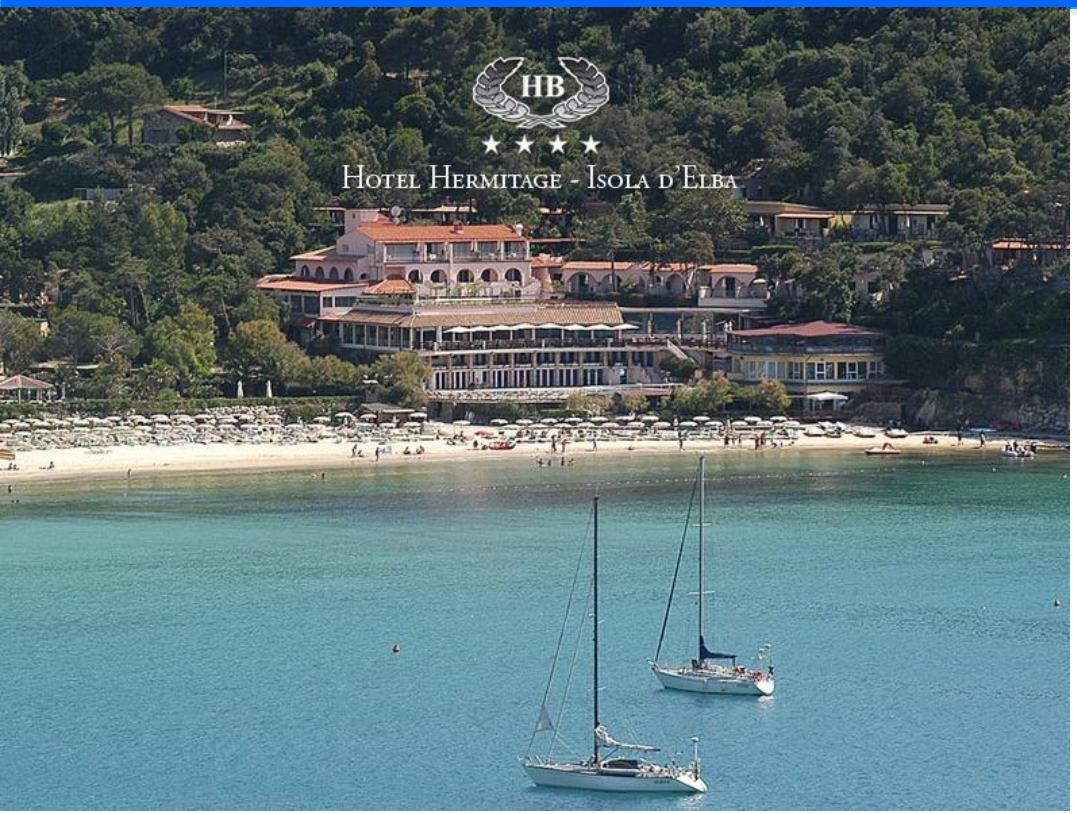
SuperB Detector Status-Elba-2011



- Overview
- System by System Updates and R&D
- Workshop Goals and Structure.

Blair Ratcliff
SLAC

Overview

- Detector design well advanced
  - Based on BaBar “prototype”
  - CDR (2007) http://web.infn.it/superb/images/stories/upload_file/superb-cdr.pdf
  - Detector Progress Report(2010): http://arxiv.org/abs/1007.4241
- Remaining Generic Detector Options to be decided following Detector Geometry Task Force reports and DGWG studies
- Proto-Detector Organization is in place. Needs to be enhanced/modified as collaboration develops.
- R&D ongoing across detector systems allow final designs to proceed.
- Aiming for TDR in about one year

Getting to the TDR

- The Technical Design Report is an essential step to a reviewable design, getting agency funding, and fabricating the detector.
- Conflicting requirements
  - Essential to reach a validated detector technical design taking machine constraints, backgrounds, overall system technical designs, and funding limitations into account.
  - Essential to enlarge the collaboration, define institutional responsibilites, and find resources for designing and building the detector
  - Essential that collaboration members, institutions and countries take ownership of the design and fabrication
  - Essential to move forward rapidly to finalizing the design and writing the TDR
- Timeline has to be adjudicated to meet all these requirements

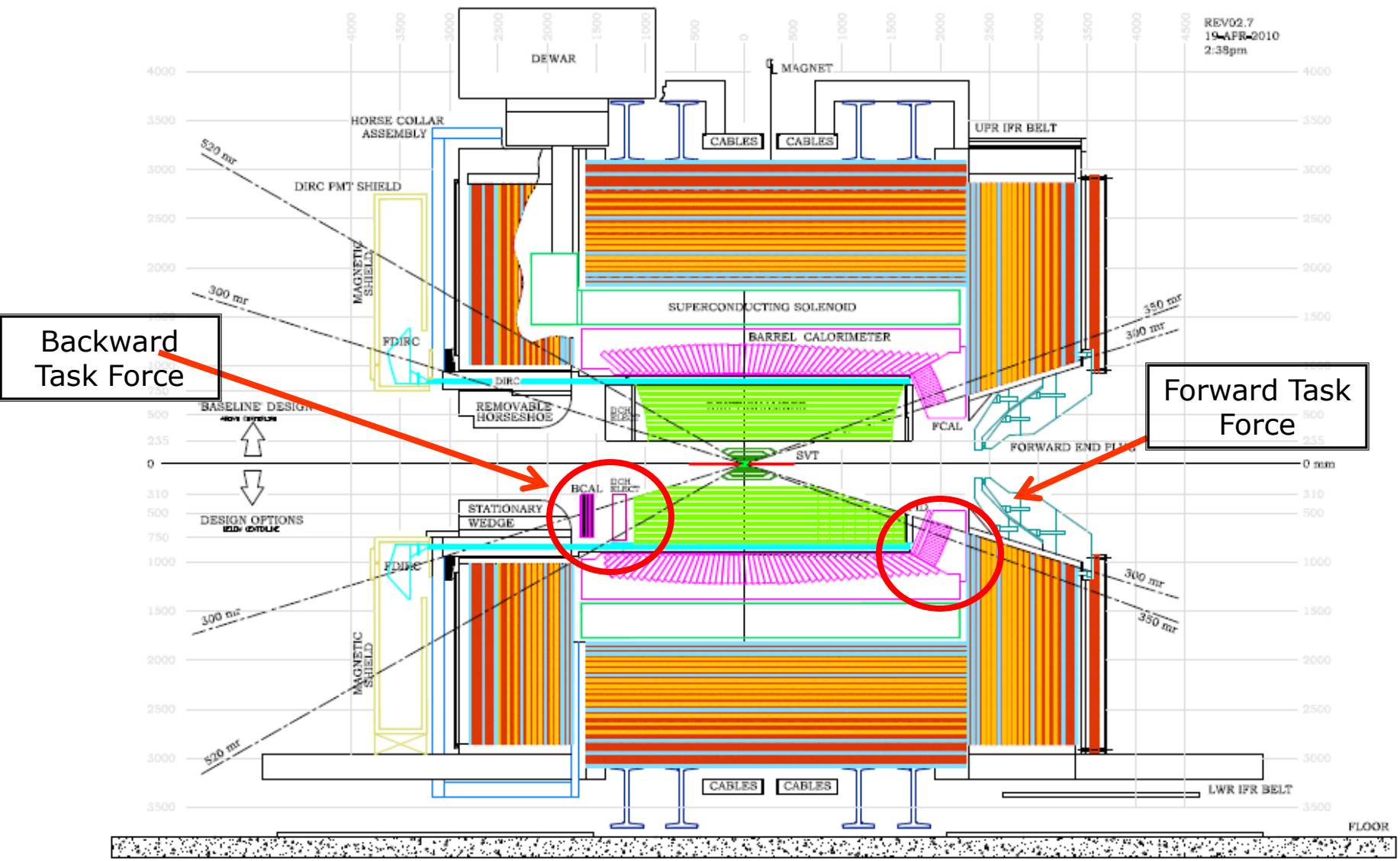
Detector Proto-Tech Board/Parallel Session Conveners

Detector Coordinators – B.Ratcliff, F. Forti
Technical Coordinator – W.Wisniewski

- SVT – G. Rizzo
- DCH – G. Finocchiaro, M.Roney
- PID – N.Arnaud, J.Vavra
- EMC – F.Porter, C.Cecchi
- IFR – R.Calabrese
- Magnet – W.Wisniewski
- Electronics, Trigger, DAQ – D. Breton, U. Marconi
- Online/DAQ – S.Luitz
- Offline SW
  - Simulation coordinator – D.Brown
  - Fast simulation – M. Rama
  - Full Simulation/Computing – F. Bianchi
- Background simulation – M.Boscolo, E.Paoloni
- Rad monitor –
- Lumi monitor –
- Polarimeter -
- Machine Detector Interface –
- Mechanical Integration Team F. Rafelli, W. Wisniewski, System Reps
- Central Electronics Team -
- +DGWG – A. Stocchi, M. Rama
- +Geometry Selection Task Forces- H. Jawahery, W. Wisniewski

Primary Detector Open Issues

SuperB Detector (with options))



Open Detector Design Issues

System	Baseline	Issues (technical OR manpower; R&D)
MDI	Initial IR designed	Magnetic elements and radiation masks. Design of tungsten shields. Background simulations: global map, detector occupancy
SVT	6-layer silicon	Technology for Layer 0: striplets or pixels. Thin pixels R&D. Readout chip for strips. Mechanical design.
DCH	Stereo-axial He-based	Dimensions (inner radius, length). Background rates. Mechanical structure. Cluster counting option R&D.
EMC	Barrel: CsI(Tl) Forw: LYSO	Electronics and trigger. Mechanical structure Forward EMC technology: LYSO / LYSO+CsI(Tl); Pure CsI. Backward EMC: cost/benefit analysis
PID	DIRC w/ FBLOCK	FBLOCK design. Photon detection. Mechanical structure Forward PID: cost/benefit analysis. Different technologies.
IFR	Scintillator+ fibers	8 vs 9 layers, and optimized configuration. SiPM radiation damage and location. Extra 10cm iron. Mechanical design and yoke reuse.
ETD	Synchronous const. latency	Fast link rad hardness. L1Trigger (jitter and rate). ROM design. Link to computing for HLT. Headroom.

Forward/Backward Task Forces

Plan for Task Force reports to the collaboration at this meeting with further discussion in Tech Board.

Forward Geometry Selection Task Force

- Hassan Jawahery, Chair
- Matteo Rama
- Brian Meadows
- Pasquale Lubrano
- Chris Hearty

Backward Geometry Selection Task Force

- Bill Wisniewski, Chair
- Achille Stocchi
- Steve Robertson
- Gianluigi Cibnetto
- Dave Aston

Brief System Reports

- **Advertisement for System Parallel Sessions.**
- **Status of Ongoing Detector Subsystem R&D**

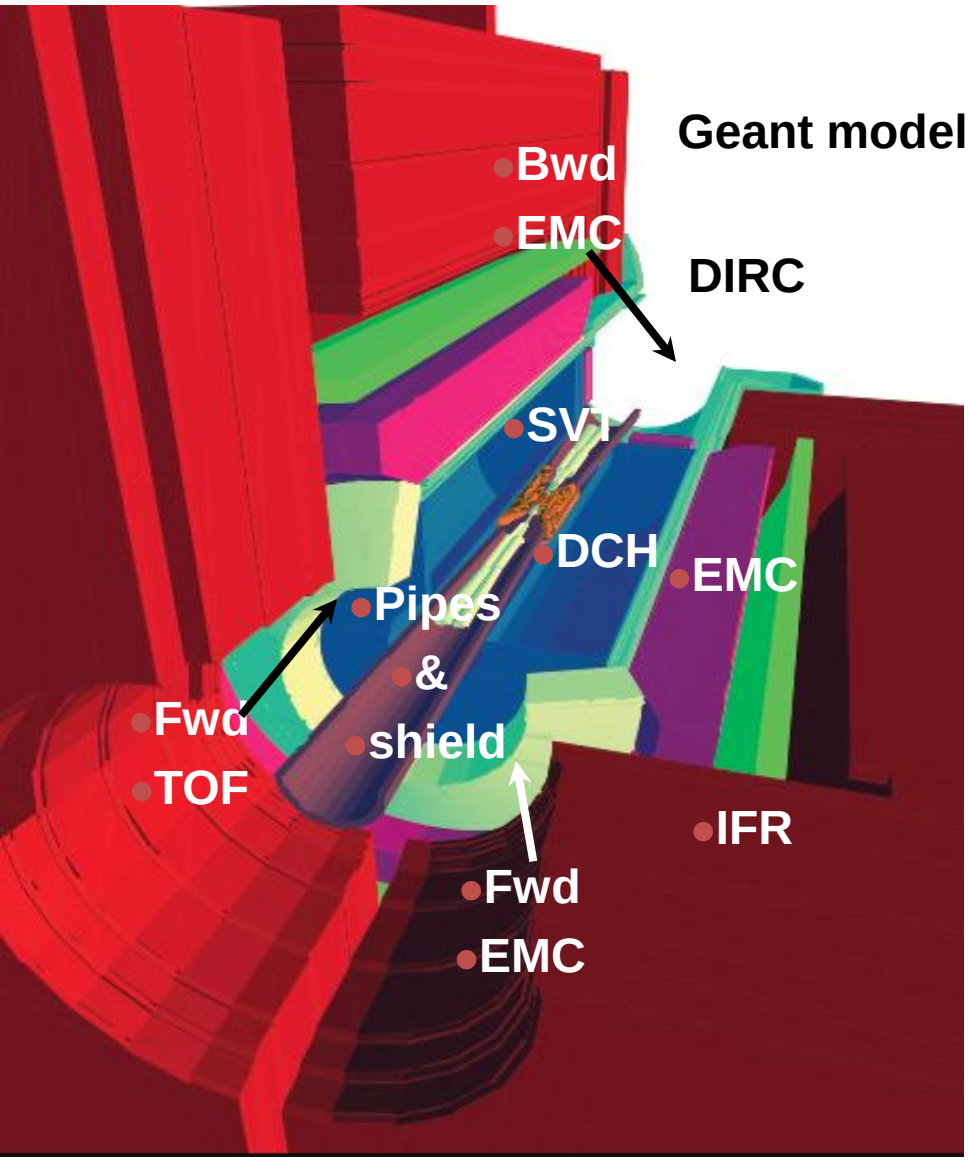
Background Simulation/MDI-Eugenio

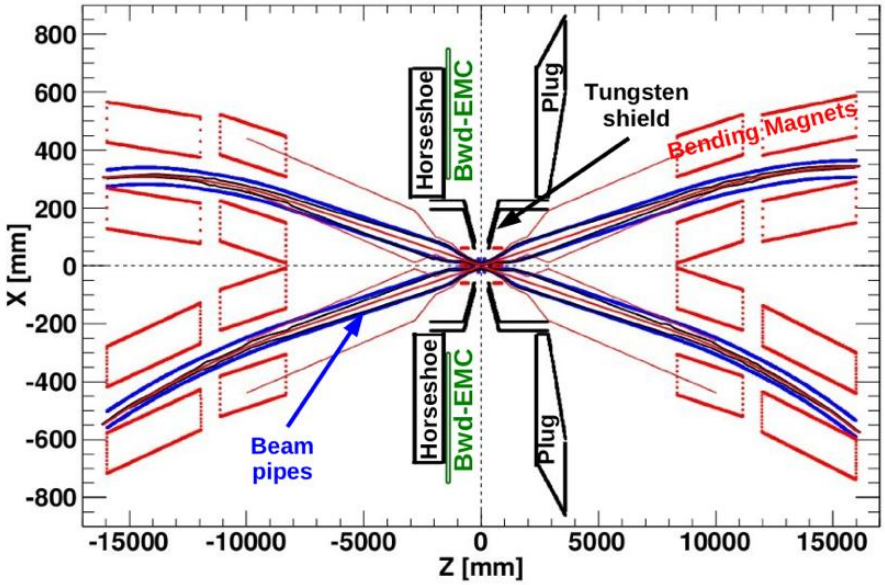
Primary Background Particle Production Rates

	Cross section	Evt/bunch xing	Rate	Generator
Radiative Bhabha	~340 mbarn (Eγ/Ebeam > 1%)	~850	0.3THz	BBBrem
e^+e^- pair production	~7.3 mbarn	~18	7GHz	Diag36
e^+e^- pair (seen by L0 @ 1.5 cm)	~0.3 mbarn	~0.8	0.3GHz	Diag36
Elastic Bhabha	$O(10^{-4})$ mbarn (Det. acceptance)	~250/Million	100KHz	Bhabhayaga/B Hwide
Y(4S)	$O(10^{-6})$ mbarn	~2.5/Million	1 KHz	
	Loss rate	Loss/bunch pass	Rate	
Touschek (LER)	14 kHz / bunch (+/- 2 m from IP)	~6/100	~14 MHz	Star (M.Boscolo)

- Primary Background Particle will eventually hit the beam pipe showering in the surrounding material
- Ad hoc Monte Carlo generator for primary particles
- Geant4 Based full simulation code for the simulation of the interaction of primary particles with the material

The Geant Simulation Program





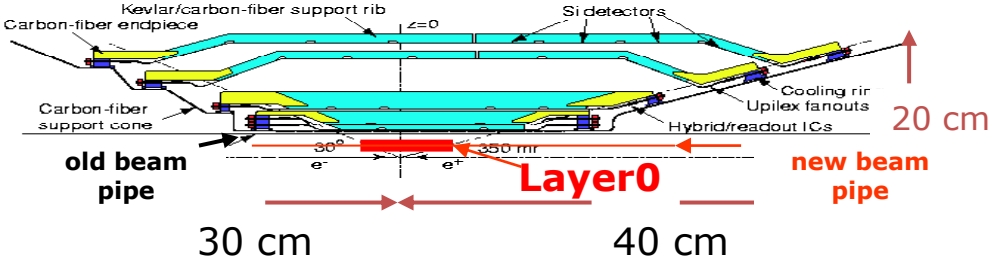
- The whole detector is modeled
- The beam lines and their magnets are modeled +/- 15m from IP
- Recent developments:
  - packaging
  - newest IR layout
  - additional truth information

New results on background simulations

- Bug fixes
  - A huge memory leak was discovered and fixed (R.Cenci). the bug prevented us from simulating more than 5 events per run with the latest detector + machine setup
    (bigger event size -> bigger leak)
    This bug does not affect the predicted rates but impacts the job management efficiency
  - Event simulation was aborted before completion of all of the HER losses (pointed out by D. Lindeman)
    - As a consequence of this the Background rates in the forward region were severely underestimated
- New results: please join the Monday parallel session devoted to
  - Analysis of the last background simulation campaign
  - Full Simulation new developments

SVT-Convener Rizzo

SVT (I)



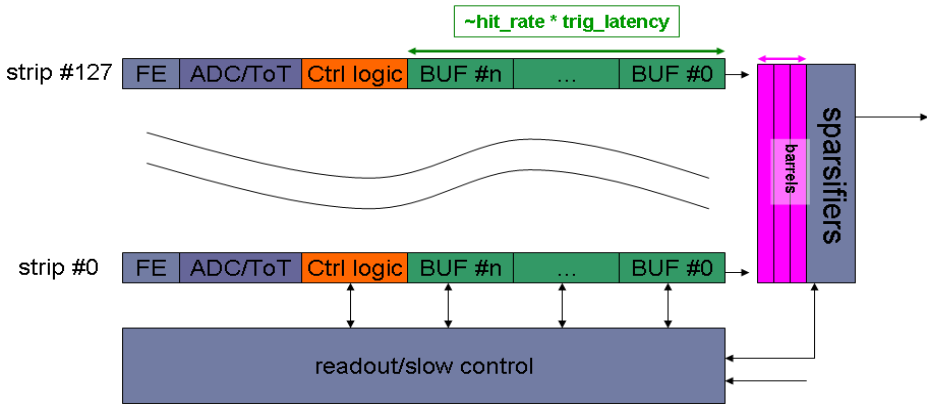
- SVT Baseline for TDR
  - Striplets in Layer0 @ R~1.5 cm
  - 5 layers of silicon strip modules (extended coverage w.r.t BaBar)
- Upgrade Layer0 to thin pixel for full luminosity run
  - more robust against background occupancy

Readout chips for striplets/strip:

- evaluation of readout architecture is ongoing:

  no obvious showstopper yet!
- First estimate of noise vs shaping time in each layer done: some optimization still needed.

FE chip for strips from pixel architecture



- Study of more detailed performance of striplets with high background (occupancy >= 10%) just started with Fastsim.

SVT (II)

Background simulation:

- Rates in strip layers 1-5 increased by a factor 3 after a bug was discovered, more checks ongoing. Layer0 was not affected.

Mechanics:

- New manpower from UK (QM) on the design of the SVT mechanics (support cones and space frames). Fruitful meeting in May in Pisa to get started

Pixel R&D:

New MAPS submission in preparation (July) with INMAPS CMOS process with high resistivity substrate & quadruple well→ to improve radiation hardness & charge collection efficiency:

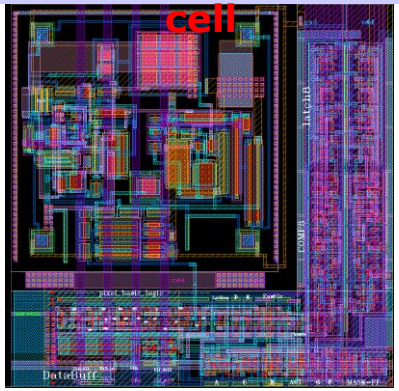
first prototype included 3x3 analog matrices and a 32x32 matrix with fast readout architecture optimized for Layer0 rates

Readout could work in data push mode & triggered mode

VHDL results for 100MHz/cm2 hit rate: Effi_triggered=98.2%, Effi_data_push=99.9%

Timestamp granularity 100 ns

•50x50 μm pixel cell



Preparation for Sept. 2011 pixel test beam ongoing: will study hybrid pixel system, CMOS MAPS with vertical integration, irradiated MAPS,…….

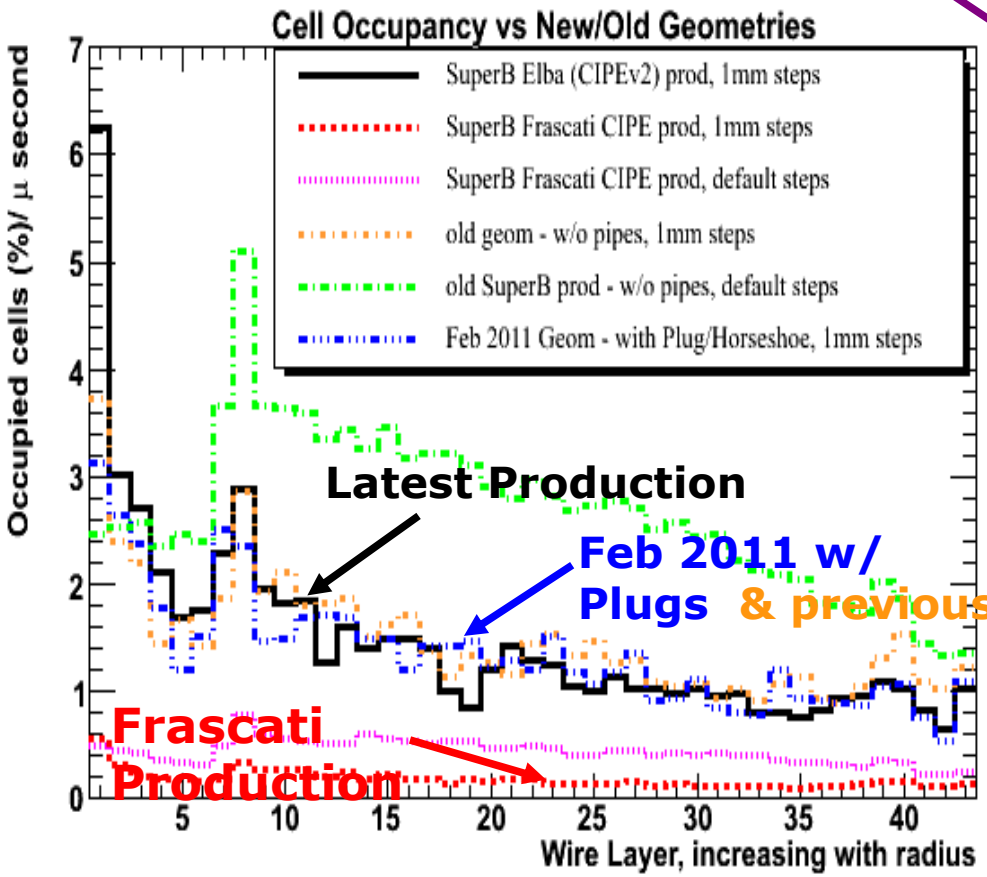
DCH-Conveners Finnocchiaro & Roney

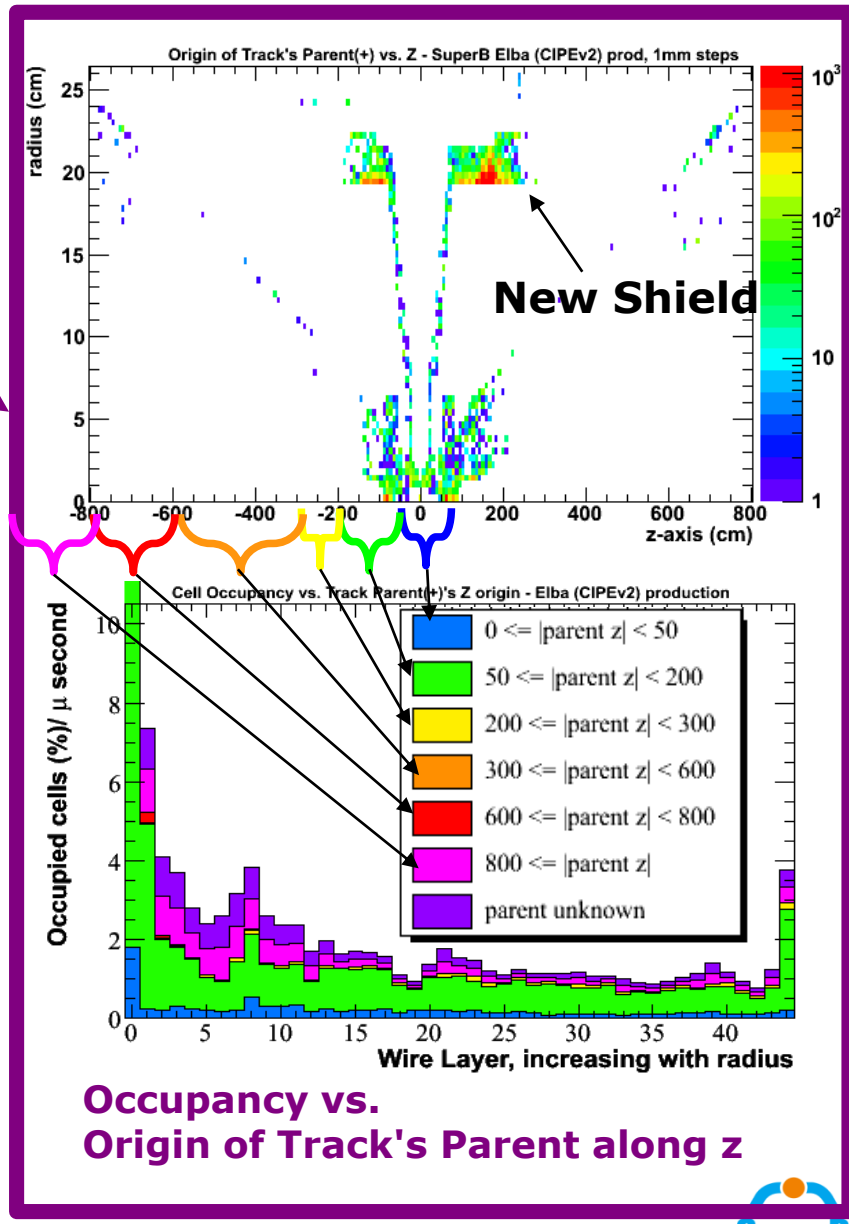
DCH results for latest FullSim prod

DCH occupancies risen since Frascati back to previous levels (1-2%) after bug fix in FullSim

1 mm step-size implemented in DCH FullSim production gives more realistic occupancies

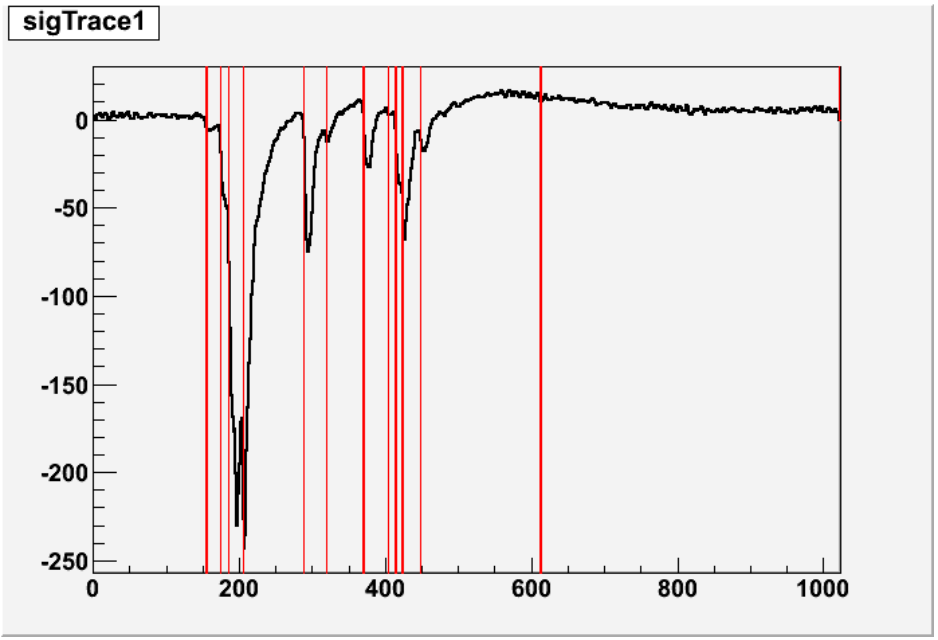
Final-Focus Truth info in FullSim production provides additional info, i.e. origin of bkg tracks

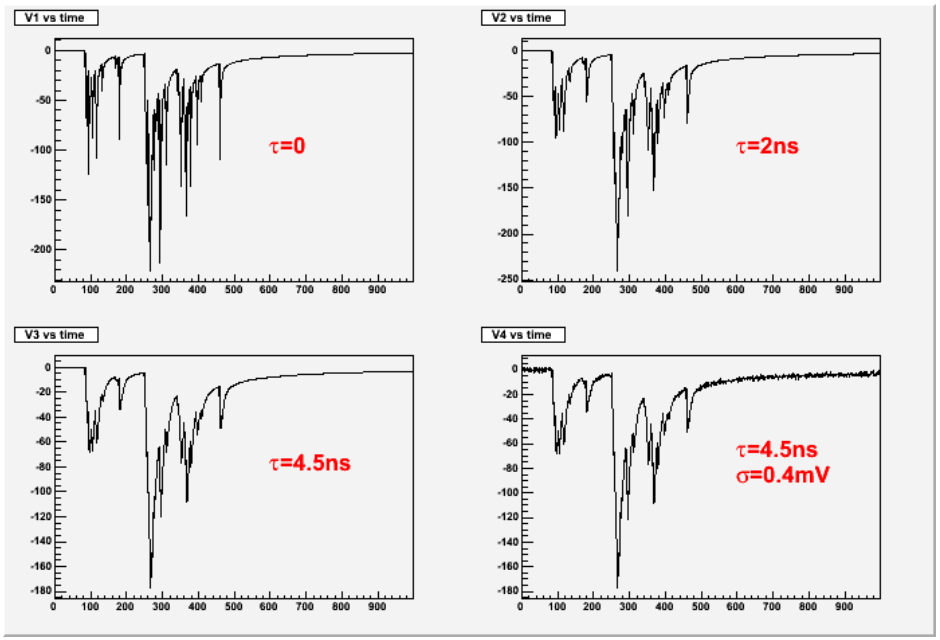




Cluster Counting in square drift tubes

- Studies are continuing on both real and simulated data
  - Different algorithms exploited to obtain good cluster counting efficiency, with low fake rates





Signal from cosmic-ray track
in 17mm-tube
90%He-10%iC_4H_{10} - *data*

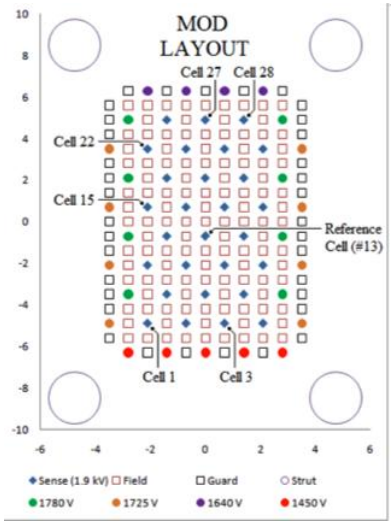
|= times of clusters found

Simulated signal from 490MeV/c π^+ in 90%He-10%iC_4H_{10} for different shaping times

Prototype 2

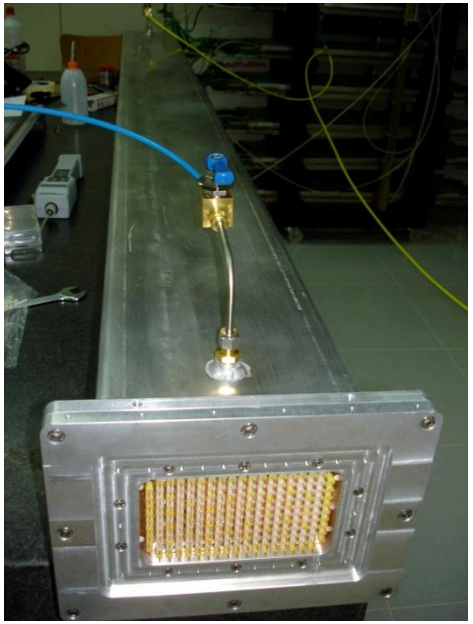
2.5m long prototype with 28 sense wires arranged in 8 layers

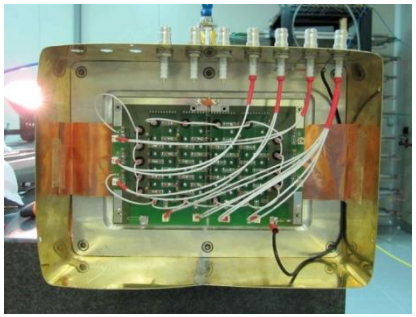
Goal: study DCH response from single clusters in a realistic environment, and serve as a test bench for the final FEE



Status:

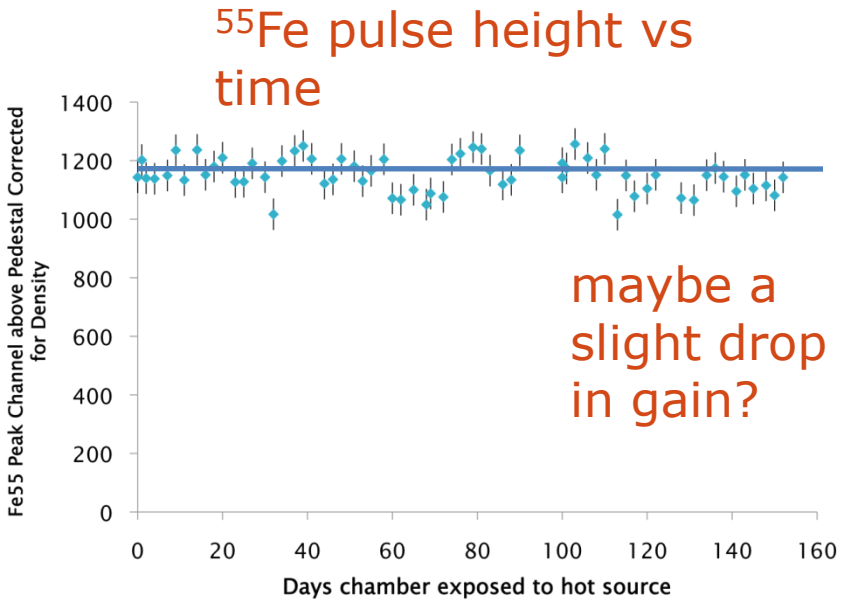
- Strung
- Gas tight
- Electronics:
  - ✓ Ground connection + HV distribution OK
  - – Fully commission preamp boards when back from Elba



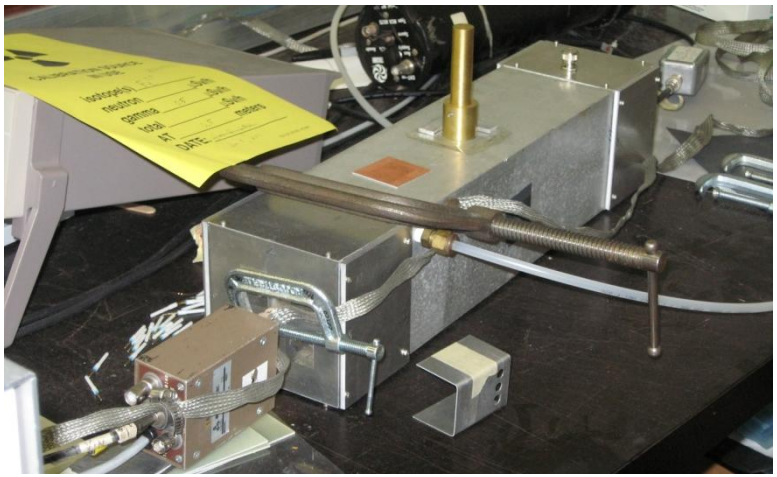


Recent DCH activities at TRIUMF

- **Aging**: BaBar wires and gas already show a lifetime >100mC/cm. Next studies will use SuperB wires and gas, and a second chamber for gain normalization.

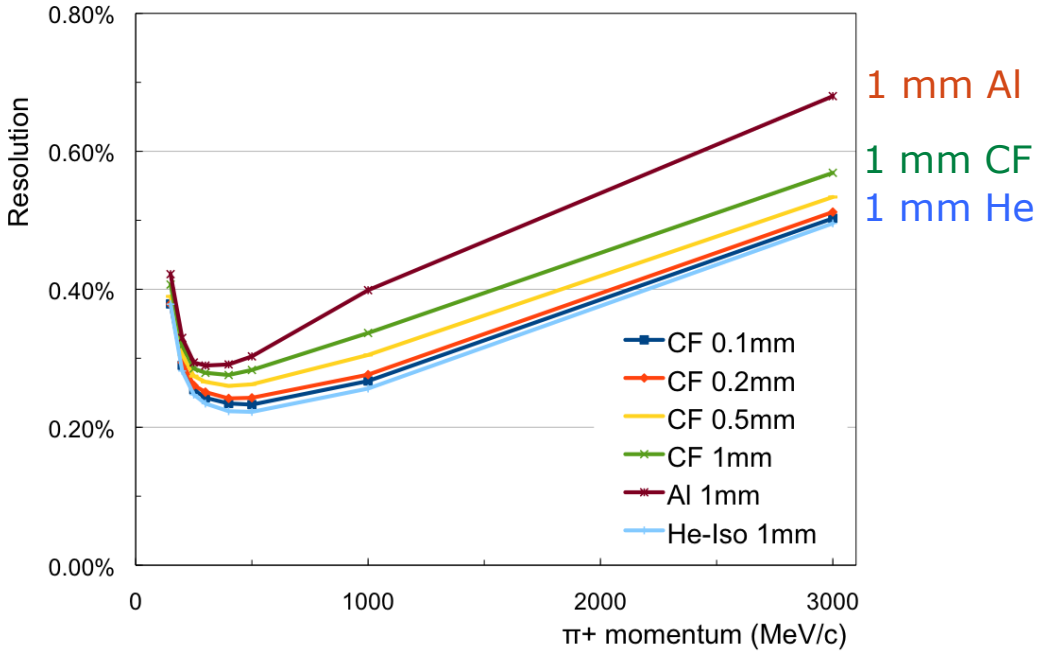


Aging chamber (BaBar wires and gas) being irradiated by 100 mCi ^{55}Fe source



New chamber has bare aluminum field wires, as planned for SuperB

- **FastSim studies** indicate that with no support tube, the thinnest possible inner cylinder (radiation lengths) is preferred.
  - thickness in mm is not as important.



- **Full length single-wire drift tube** will allow Montreal group to study preamp design with realistic signals from either ^{55}Fe or ^{90}Sr sources.
  - now on its way to Montreal

Recent Activity at LNF

- Recent work concentrating on instrumenting the new 28-channel chamber prototype.
  - Several boards have been developed, including a seven-channels preamplifier board for Cluster Counting measurement with Gain ≈ 9 mV/fC , noise ≈ 2500 e- rms @ 250 MHz BW.
  - At the same time, a study is going on to verify the feasibility of using a FLASH based FPGA to implement the standard readout system (no CC). In particular we are trying to implement a 1 ns resolution TDC that is the most demanding part of the system (it has already been successfully implemented using a Xilinx Virtex5 device).
- Continue to develop electyronic designto implement Cluster Counting

  FADC@1GHz + local feature extraction (i.e. arrival time of individual clusters)

  FADC@1GHz + buffers and remote feature extraction

  Analog derivative method + local feature extraction

  ➔All have challenges that must be further explored

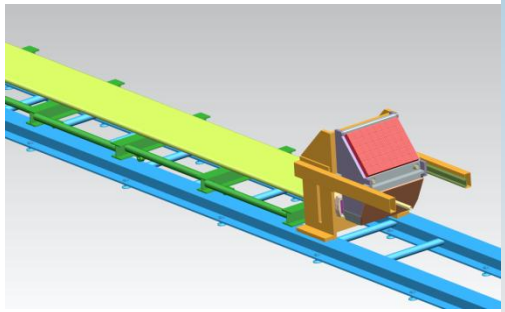
PID-Conveners Vavra & Arnaud

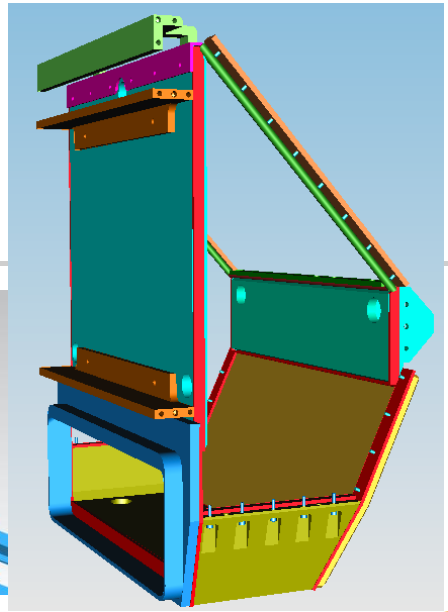
Barrel PID

- **FBLOCK** [SLAC]
  - Both New Wedge and FBLOCK precision grinding on the NC machine is finished. Polishing starts tomorrow. The last step (plating of mirrors) follows.
  - Finished the R&D study how to couple large areas surfaces optically.
  - Finished a study how to bring the calibration light into the FBLOCK.

- **Geant4 simulation** [Maryland]
  - MC program updated for the latest mechanical geometry.

- **Mechanics** [SLAC + Padova + Bari]
  - Working on parts for the Fbox, and the FDIRC ptototype mechanical support in CRT.

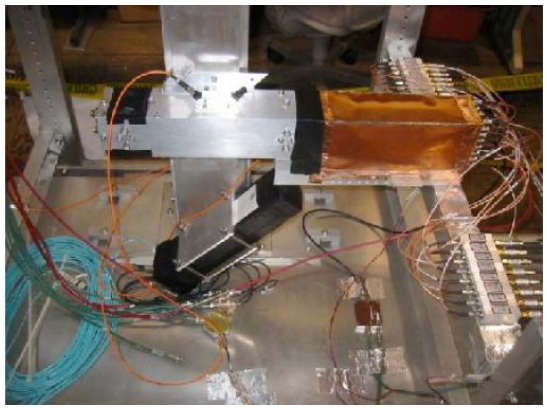




Forward PID

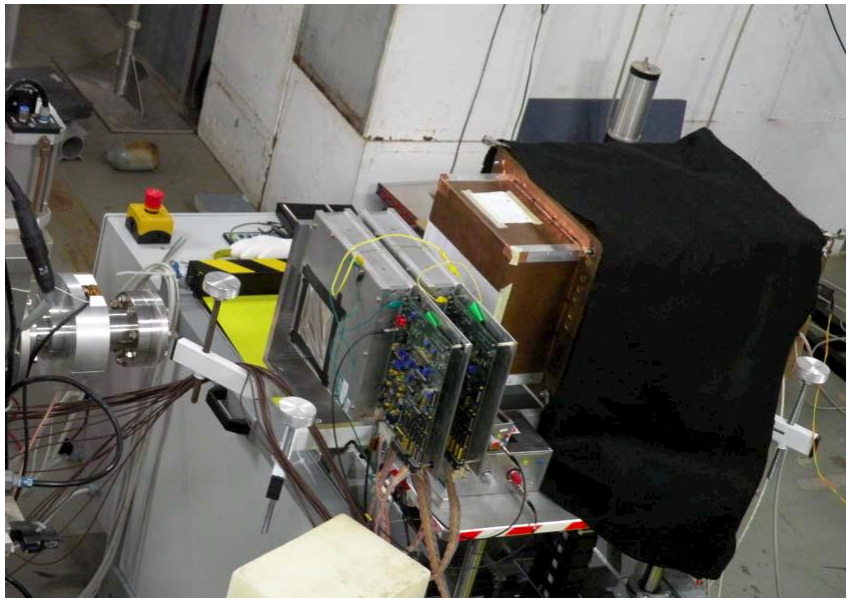
- **FARICH** [Novosibirsk]
  - Test beam results from the FARICH prototype (see parallel session)

- **FTOF** [LAL-Orsay + SLAC]
  - CRT test at SLAC finished data taking. Data analysis is in progress.
  - Analysis of the latest background simulation at SuperB.
  - Design of the 16-channel USBWC board in progress.



EMC-Conveners (Cecchi & Porter)

New Test Beam@LNF in May



We tried to reproduce about the same matrix configuration as in the CERN TB

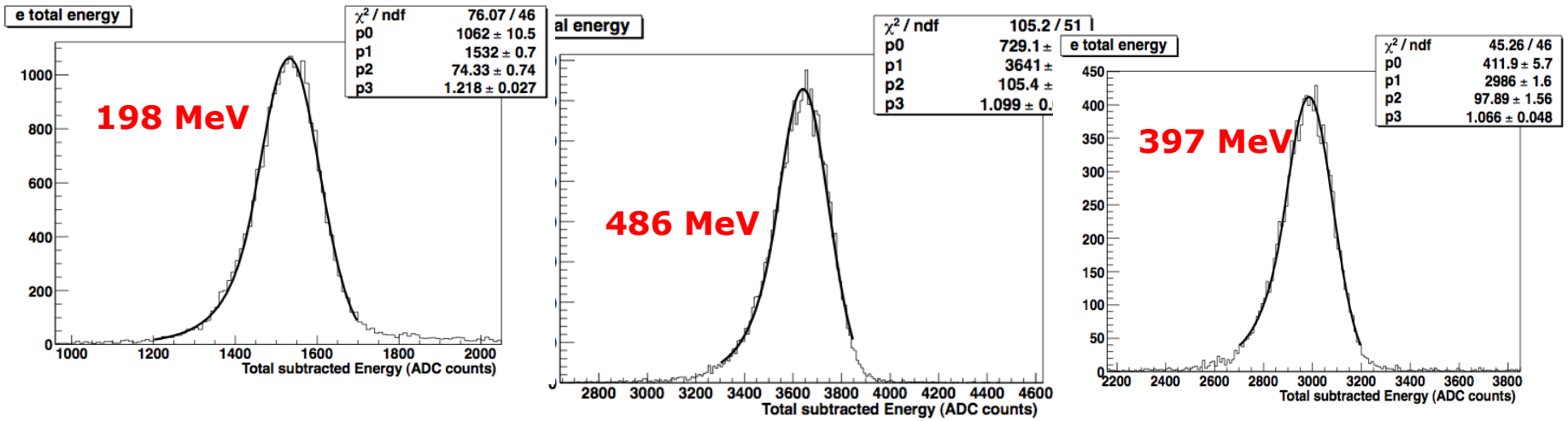
- 1.5cm black strip painted on each crystals

except one: SIC3 crystals has one side roughened

One APD for each crystal

- A successful run in spite of a number of technical issues, including a bad cable, and about 2% cross talk in the electronics
- Results will be discussed in parallel sessions.
- Please note that the Sunday EMC session will start at 15:30 today.

Examples of energy distributions in Crystals

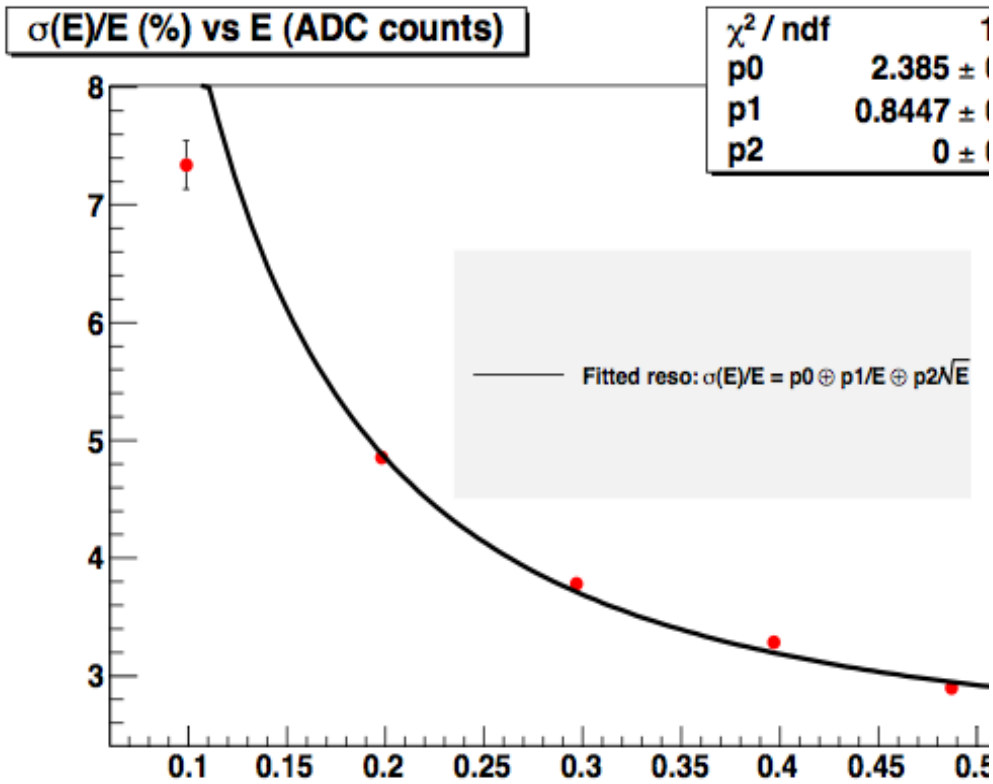


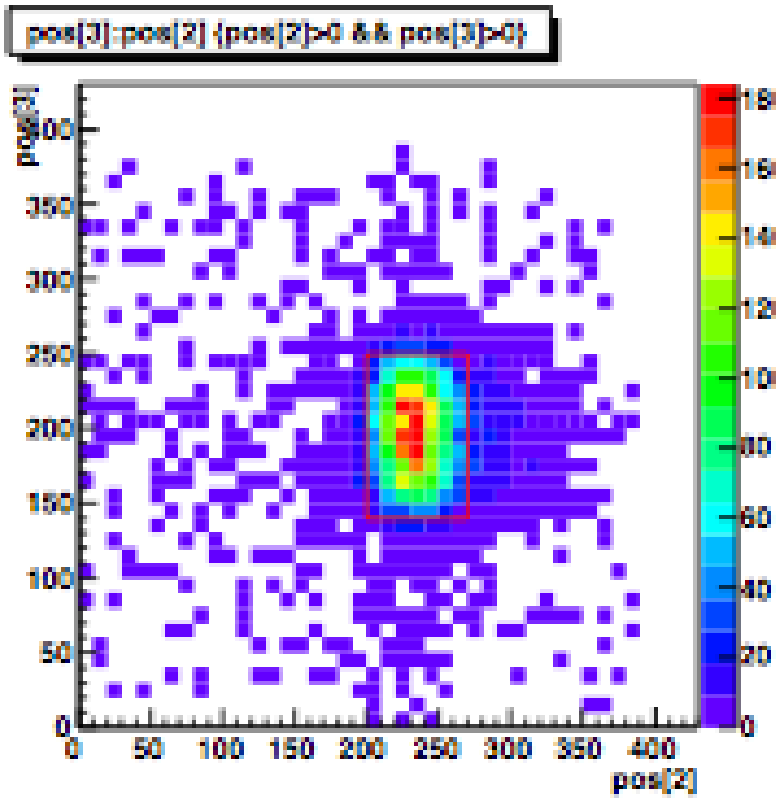
→Electrons on crystal 12 (matrix center)

→Position Selection applied

→Inter-calibration with e- resolution minimization

Energy resolution fit – Position Selected





→**no selection :** 3.0 +/- 0.02 %

→**loose selection :** 2.9 +/- 0.03 % ; x = [200,270] , y = [140,250] 1.6x2.3 cm

→**tight selection :** 2.7 +/- 0.02 %; x = [220,250] , y = [160,220] 0.7x1.4 cm

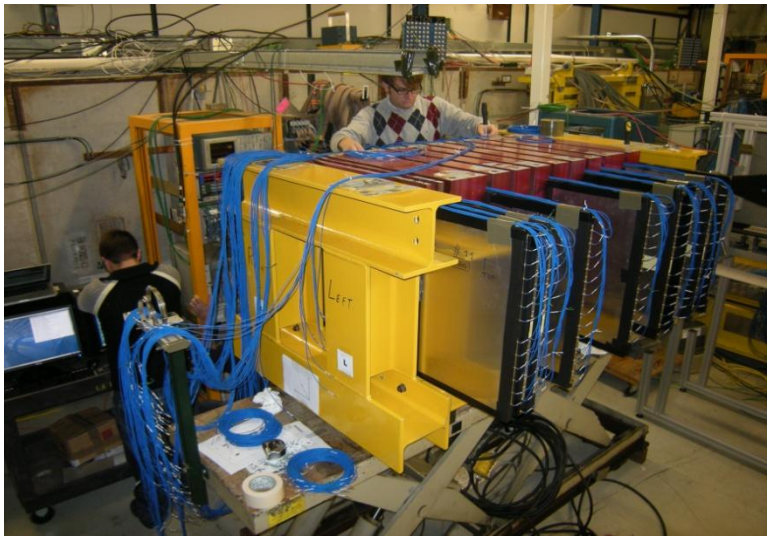
→**very tight selection : 2.6 +/- 0.003 %; x = [220,240] , y = [180,220] 0.5x0.9 cm**

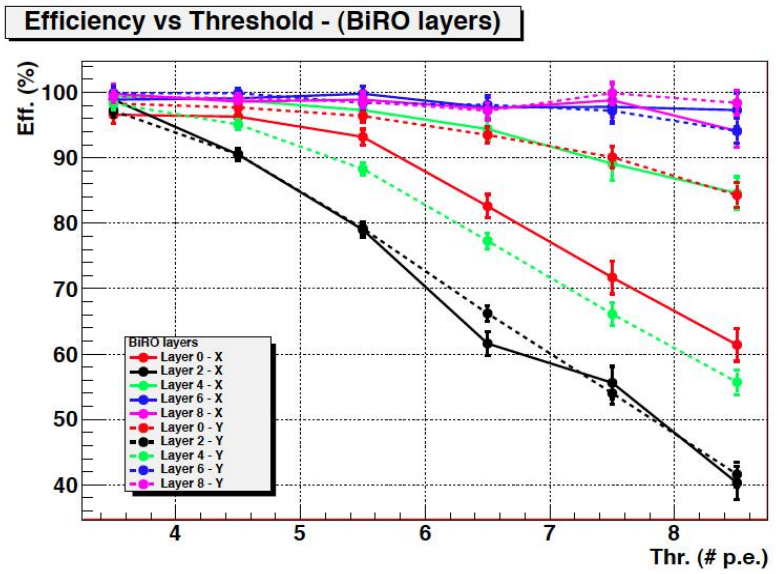
Another Test Beam planned in September with optimized LYSO uniformization (roughening of the crystal surface + 2 APD's per crystal)

Detector Elements-IFR-Convener Calabrese

IFR R&D status

- A full depth Prototype tested (1-7 Dec 2010) at the Fermilab Test Beam Facility (Meson Area)
- 9 layer configuration tested with different readout schemes (5 BiRO layers and 4 TDC layers)
- Beam Test Data analysis ongoing
- Prototype shipped back and reassembled in Ferrara (no Iron) to continue the test with cosmics
- New Beam Test planned for this summer





Preparation for next beam test

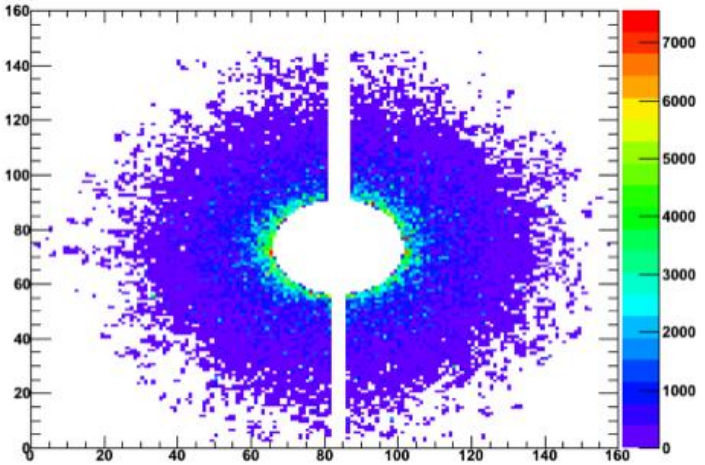
- The prototype is now up and running in Ferrara
  - during the day….. software and DAQ development
  - night and weekend…..run with cosmics for detector calibration
- R&D results confirm good performance and provide a proof of principle of the detector readout.

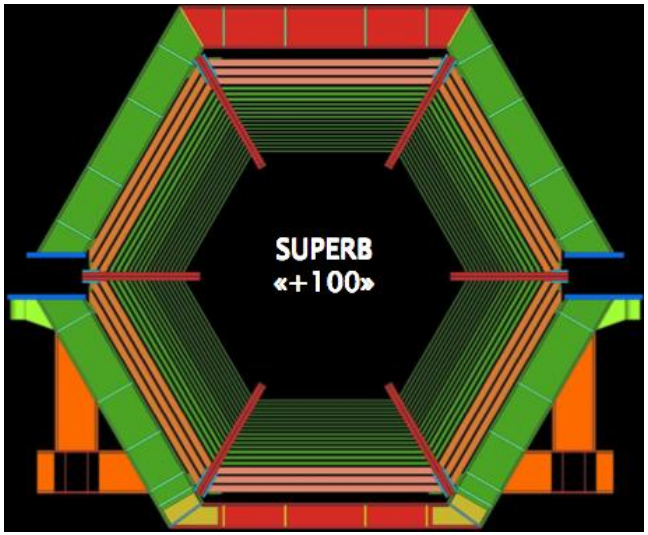
- Beam test analysis still in progress. First PID results expected at this meeting. Main difficulties are the understanding the beam composition and contamination and the MC tuning.
- Careful review of results from the last beam test will improve the setup for the next run (July 2011).

Toward the TDR

Major issue to be resolved before finalizing the detector design

- Neutron background evaluation for SiPM damage
  - has impact on photodetector location
  - addressed with simulation and irradiation tests
- Flux return modeling: evaluation of costs, mechanical feasibility, performance
  - impact on the iron layout
  - addressed with FEA and beam test analysis
- TDC performance
  - impact on the detector readout and design
  - addressed with beam test data analysis and full simulation





Three Krakow groups (AGH, CUT, INP PAN) just joined the IFR group: welcome!

IFR Goals for this meeting

- Review advancements and achievements in all the development areas
- Focus on prototype beam test
- Analyze the TDR preparation process and prioritize the short and medium term activities

Electronics, Trigger and DAQ- Conveners,Breton, Luitz, & Marconi

ETD (1)

We will have 3 sessions during this workshop:

- one dedicated to hardware trigger => Monday 8:30
- one concerning common items => Tuesday 8:30
- one concerning front-end electronics=> Tuesday 11:00

During the trigger session, Steffen will present an introductory talk to ETD for newcomers.

During the front-end session, a special focus will be made on the implementation, volume, power (cooling) and location of subdetector electronics.

Clock and control links:

- Xilinx FPGA radiation tolerance will be described by Raffaele
- A new simple link encoding will be introduced by Sergio.
- The use of mezzanines vs firmware blocks will be discussed again for the FCTS and ROM sides
- We have to define plans to start qualifying components of the optical layer
- One talk submitted to IEEE NSS 2011 in Valencia

ETD (2)

ROM: first measurements of the rate of FPGA-driven data transmission via PCI-express was measured in Bologna.

- Xilinx Virtex6 PCIe evaluation board plugged on a high-end PC motherboard
- FPGA was programmed to generate and transmit data through PCIe to the PC via a 8x PCIe lanes @ 2.5 Gb/s per lane
- A very encouraging transmission rate of 14.5 Gb/s was measured
- This is already above the 10Gb/s of the output NIC card
- A summary of these results will be presented by Umberto

Common Front-End Electronics: simulations of the actual hardware implementation (VERILOG model) of the front-end derandomizer of will be presented by Jihane

- the goal here is to give to subdetectors a table with the necessary derandomizer depth and number of bits per event per link with respect to the width of their own trigger time window

Trigger:

- One talk submitted to IEEE NSS 2011 in Valencia
- Simulation work has been started to determine Bhabha rates

All these subjects will be analysed in view of the TDR writing.

DGWG-Rama & Stocchi

Detector geometry working group

Since the last meeting in Frascati:

NEW STUDIES OF

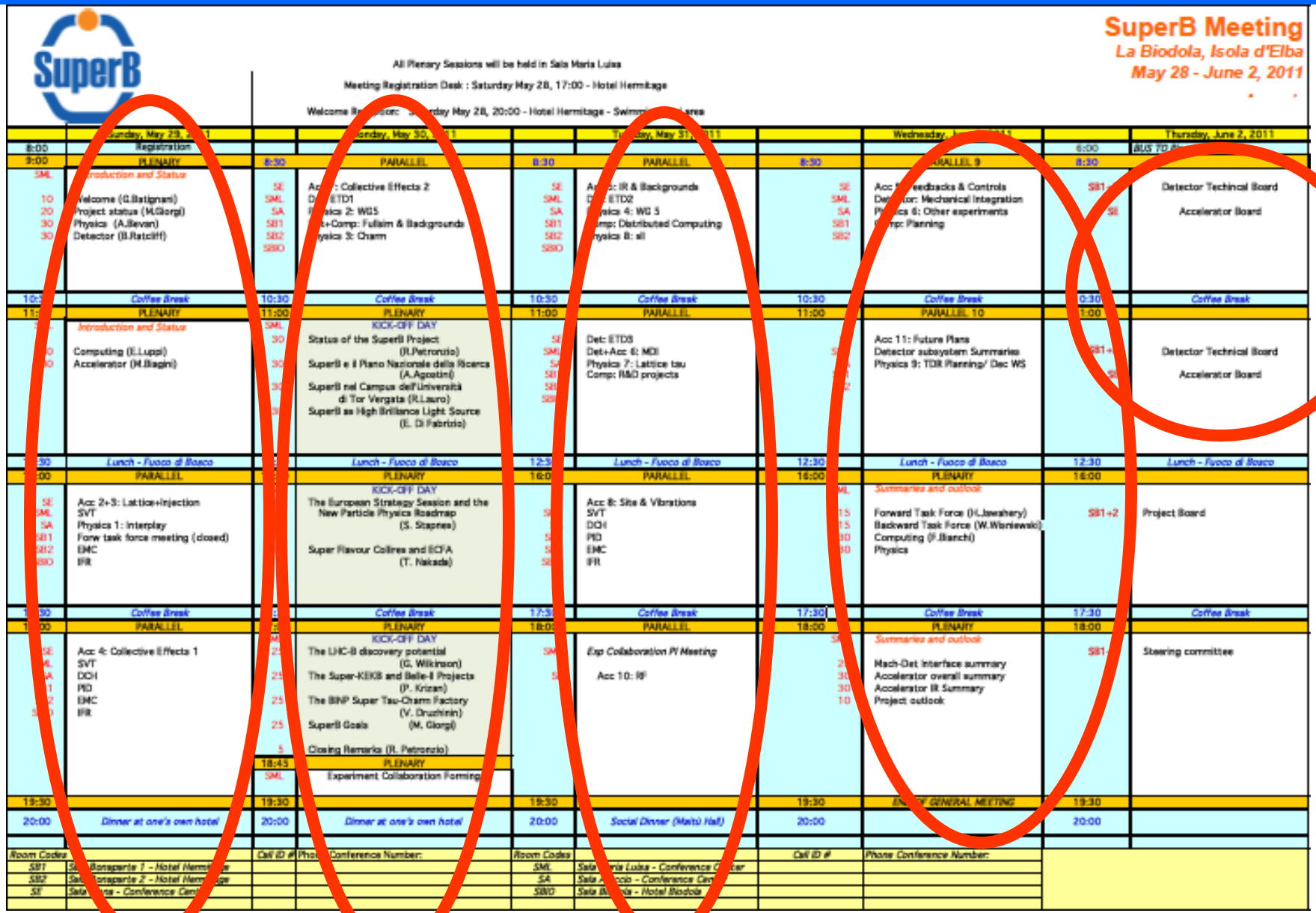
- Impact of backward EM calorimeter on Physics
  $B \rightarrow K^{(*)}\nu\nu$, $B \rightarrow \tau\nu$ hadronic and SL tag
- Impact of material on π^0 reconstruction and efficiency
  request from the Forward Task Force

Joint DGWG – EMC session

Tuesday at 16:00

Agenda

Detector Related Workshop Sessions



SuperB Meeting
La Biodola, Isola d'Elba
May 28 - June 2, 2011

All Plenary Sessions will be held in Sala Maria Luisa

Meeting Registration Desk : Saturday May 28, 17:00 - Hotel Hermitage

Welcome Reception : Saturday May 28, 20:00 - Hotel Hermitage - Swimming pool area

	Sunday, May 29, 2011		Monday, May 30, 2011		Tuesday, May 31, 2011		Wednesday, June 1, 2011		Thursday, June 2, 2011
8:00	Registration							8:00	BUS TO Pisa
9:00	PLENARY	8:30	PARALLEL	8:30	PARALLEL	8:30	PARALLEL 9	8:30	
SML	Introduction and Status	SE	Acc: Collective Effects 2	SE	Acc: IR & Backgrounds	SE	Acc 9: Feedbacks & Controls	SB1	Detector Technical Board
10	Welcome (G.Batignani)	SML	Det: ETD1	SML	Det: ETD2	SML	Det+Acc: Mechanical Integration	SE	Accelerator Board
20	Project status (M.Giorgi)	SA	Physics 2: WG5	SA	Physics 4: WG 5	SA	Physics 6: Other experiments		
30	Physics (A.Bevan)	SB1	Det+Comp: Fullsim & Backgrounds	SB1	Comp: Distributed Computing	SB1	Comp: Planning		
30	Detector (B.Ratcliff)	SB2	Physics 3: Charm	SB2	Physics 8: all	SB2			
		SBIO							
10:30	Coffee Break	10:30	Coffee Break	10:30	Coffee Break	10:30	Coffee Break	10:30	Coffee Break
11:00	PLENARY	11:00	PLENARY	11:00	PARALLEL	11:00	PARALLEL 10	11:00	
SML	Introduction and Status	SML	KICK-OFF DAY						
30	Computing (E.Luppi)	30	Status of the SuperB Project (R.Petronzio)	SE	Det: ETD3		Acc 11: Future Plans	SB1+	Detector Technical Board
50	Accelerator (M.Biagini)	50	SuperB e il Piano Nazionale della Ricerca (A.Agostini)	SML	Det+Acc 6: MDI		Detector subsystem Summaries		Accelerator Board
			SuperB nel Campus dell'Università di Tor Vergata (R.Lauro)	SA	Physics 7: Lattice tau		Physics 9: TDR Planning/ Dec WS	SE	
			SuperB as High Brilliance Light Source (E. Di Fabrizio)	SB1	Comp: R&D projects				
12:30	Lunch - Fuoco di Bosco	12:30	Lunch - Fuoco di Bosco	12:30	Lunch - Fuoco di Bosco	12:30	Lunch - Fuoco di Bosco	12:30	Lunch - Fuoco di Bosco
14:00	PARALLEL	14:00	PLENARY	14:00	PARALLEL	14:00	PLENARY	14:00	
			KICK-OFF DAY			SML	Summaries and outlook		
SE	Acc 2+3: Lattice+Injection		The European Strategy Session and the New Particle Physics Roadmap (S. Stapnes)		Acc 8: Site & Vibrations	15	Forward Task Force (H.Jawahery)	SB1+2	Project Board
SML	SVT			SVT	15	Backward Task Force (W.Wisniewski)			
SA	Physics 1: Interplay			DCH	30	Computing (F.Bianchi)			
SB1	Form task force meeting (closed)		Super Flavour Colliders and ECFA (T. Nakada)	PID	30	Physics			
SB2	EMC			EMC	10				
SBIO	IFR			IFR					
15:30	Coffee Break	15:30	Coffee Break	15:30	Coffee Break	15:30	Coffee Break	15:30	Coffee Break
16:00	PARALLEL	16:00	PLENARY	16:00	PARALLEL	16:00	PLENARY	16:00	
			KICK-OFF DAY				Summaries and outlook		
SE	Acc 4: Collective Effects 1	25	The LHC-B discovery potential (G. Wilkinson)	SML	Exp Collaboration PI Meeting	20	Mach-Det Interface summary	SB1	Steering committee
SML	SVT	25	The Super-KEKB and Belle-II Projects (P. Krizan)			30	Accelerator overall summary		
SA	DCH				Acc 10: RF	30	Accelerator IR Summary		
SB1	PID	25	The BINP Super Tau-Charm Factory (V. Druzhinin)			10	Project outlook		
SB2	EMC								
SBIO	IFR	25	SuperB Goals (M. Giorgi)						
		5	Closing Remarks (R. Petronzio)						
		18:45	PLENARY						
		SML	Experiment Collaboration Forming						
19:30		19:30		19:30		19:30	ENJOY GENERAL MEETING	19:30	
20:00	Dinner at one's own hotel	20:00	Dinner at one's own hotel	20:00	Social Dinner (Main) Hall	20:00		20:00	

Room Codes		Call ID #	Phone Conference Number:
SB1	Sala Bonaparte 1 - Hotel Hermitage		
SB2	Sala Bonaparte 2 - Hotel Hermitage		
SE	Sala Elba - Conference Center		

Room Codes		Call ID #	Phone Conference Number:
SML	Sala Maria Luisa - Conference Center		
SA	Sala Auditorio - Conference Center		
SBIO	Sala Biodola - Hotel Biodola		

Focus of Workshop

- Global System and Integration Issues
  - Complete Work of Forward and Backward Task Forces
  - Computing & Simulation
- Review ongoing R&D
- Refine understanding needed towards final subsystem and general system design
  - Complete Design
  - R&D (Beam Tests & Milestones)
  - Integration
  - Organization
  - Build Manpower, Add Institutions
  - Deeper WBS
  - Define Specific Resource (Manpower and Budget Needs)
  - Specific TDR Production Plans
- Documents and Planning

  Now → Detailed Resource Planning & Requirements for TDR phase.

  → TDR (~ 1year).
- Build Collaboration. Many opportunities for active physicists, engineers and students to get involved at all levels.