Preliminary DC Trigger view

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Let's remember the specs in SuperB

Baseline:

- re-implement BaBar L1 trigger with some improvements
  - Shorter latency (~6us instead of 12us)
  - Higher sampling frequencies (DCH and EMC)
  - 2-d map for calorimeter

Possible additions

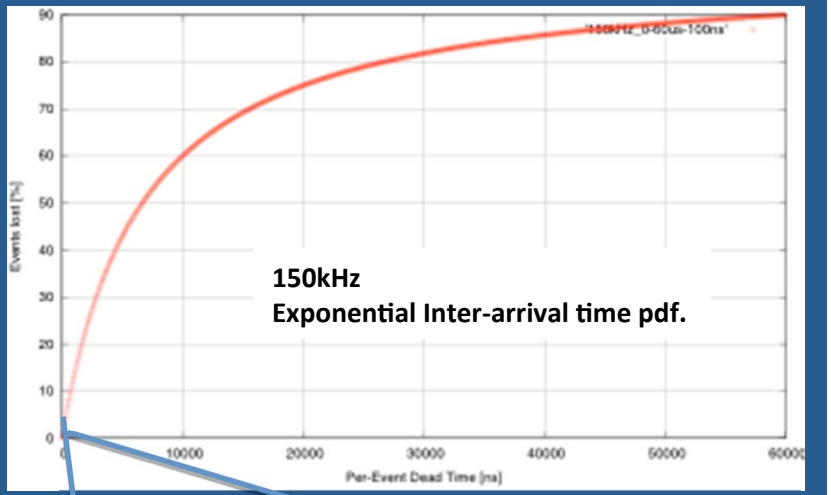
- SVT trigger
- What about the TOF ? (in DELPHI we used it in the trigger)
- Bhabha Veto
- Do we need an absolute time stamp at the trigger level?

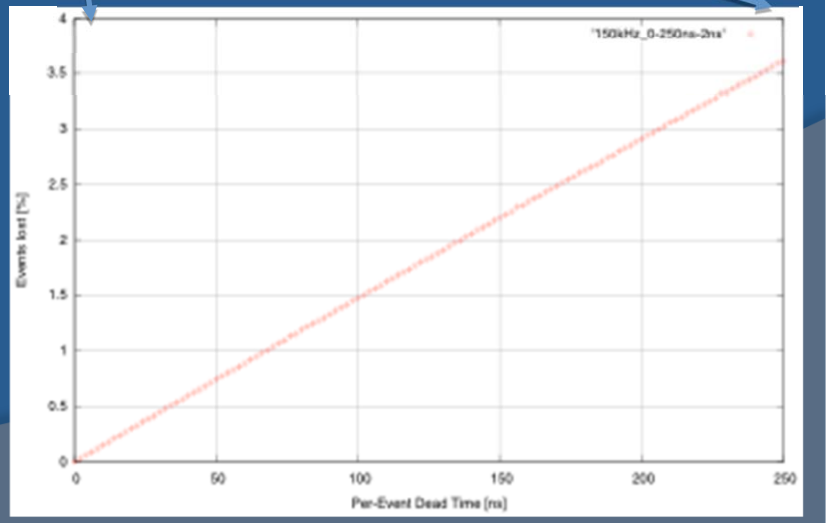
Challenge

- To keep the event loss due to dead time below 1% => a maximum of ~70ns "per-event dead time" is allowed in trigger and FCTS

Other considerations

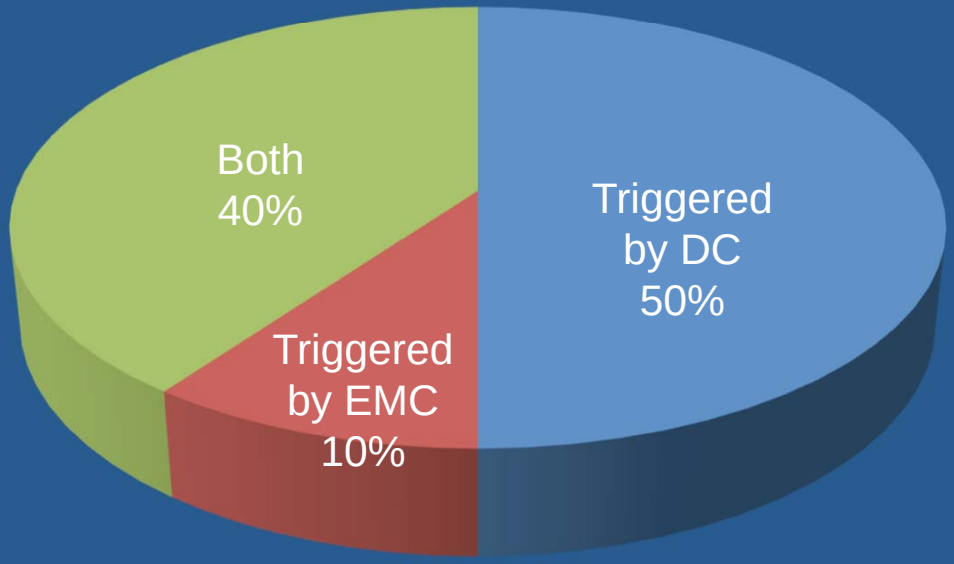
- What goes in L1, what in L3, what's the optimum?





Luitz 2010

Triggered event apple pie



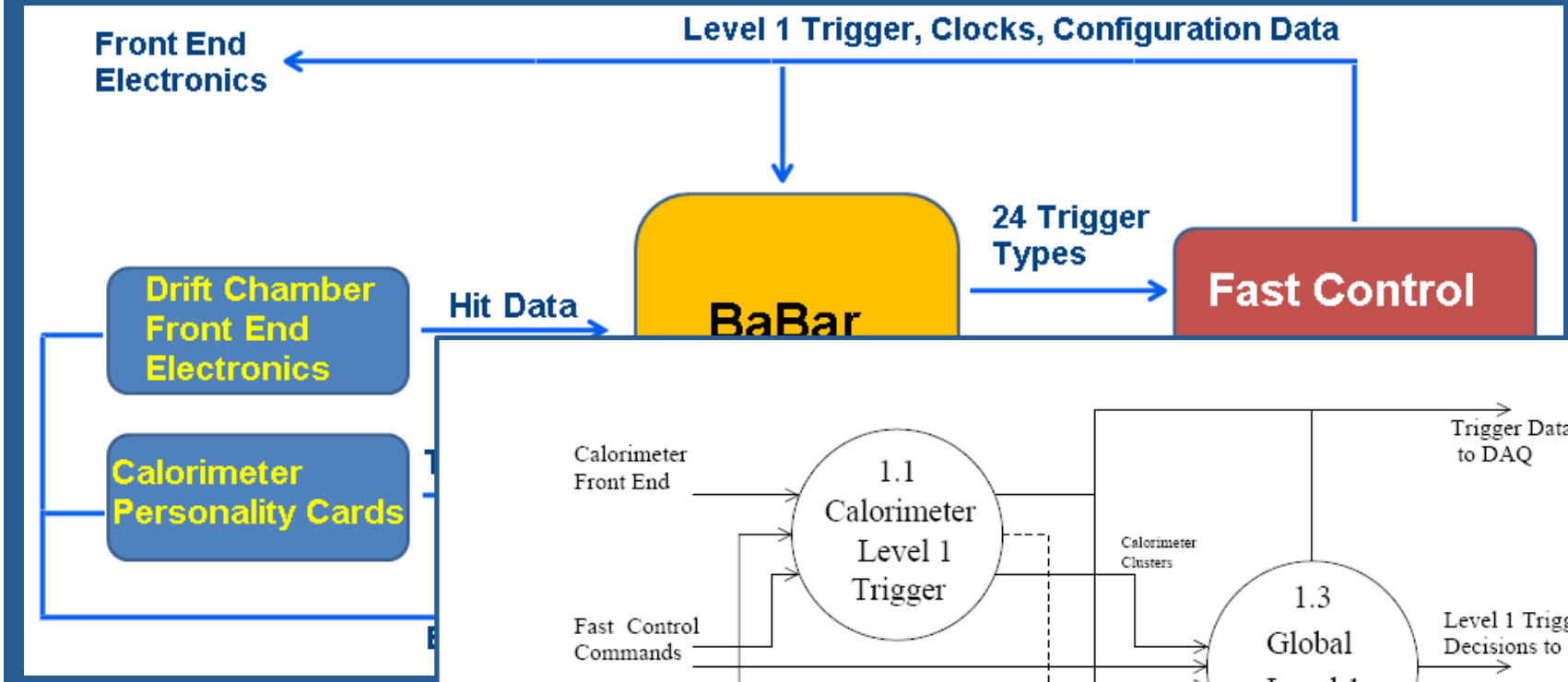
The original BaBar trigger time resolution was about 100 ns.
Can we improve it?

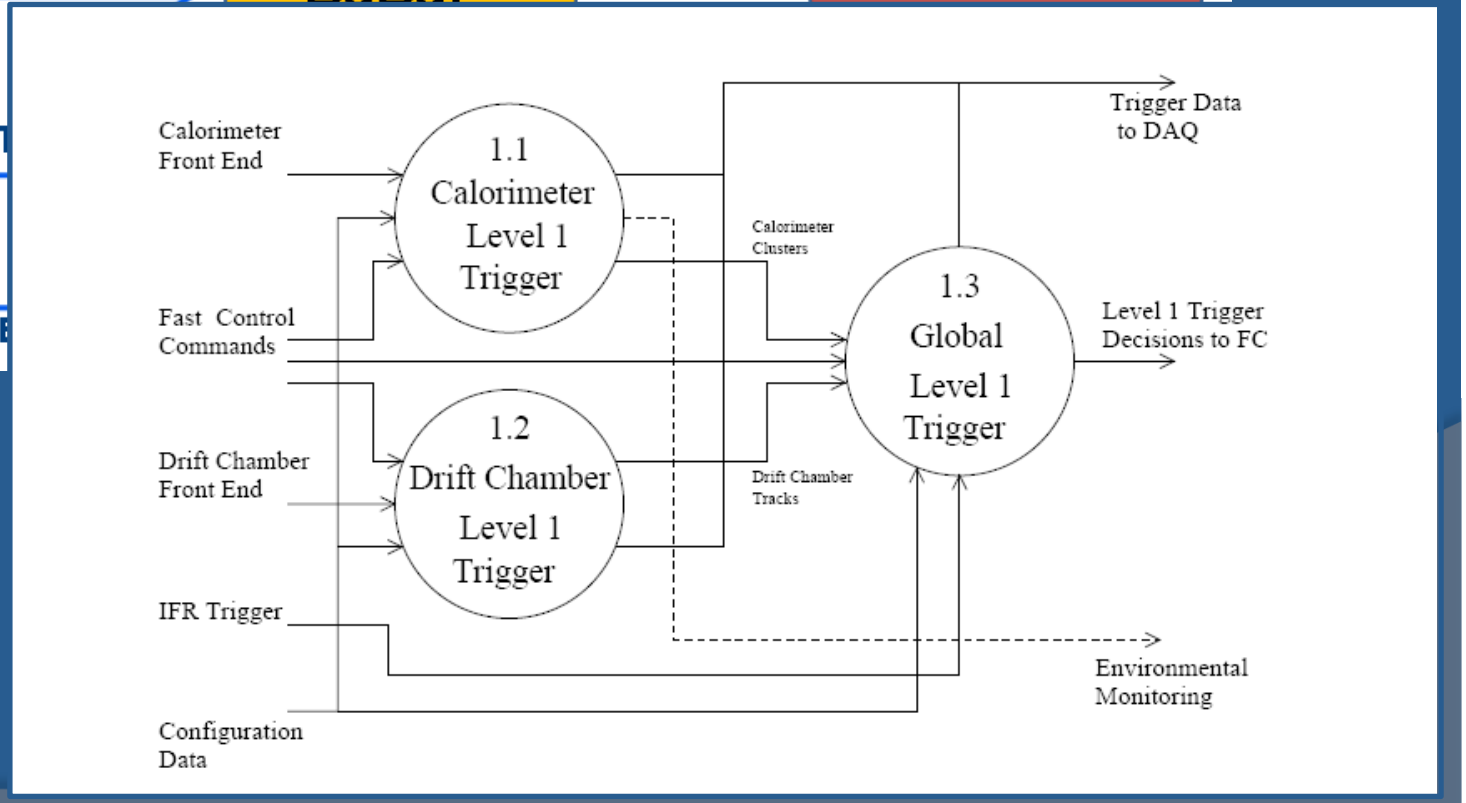
100 ns good for BaBar running@2.2 μs dead time.
We should aim at 30 ns since SuperB dead time is estimated to be 70 ns.

P. D. Dauncey et Al., "Design and performance of the level 1 calorimeter trigger for the BABAR detector" (2001)

BaBar: Trigger Layout

J. C. Andress et Al., “BaBar Calorimeter Level 1 Trigger Design” , BaBar Note (1998)





Latency in DC

- Latency in BaBar :
  - DC event processing about 6 μs +
  - GLT event processing 3 μs +
  - trigger data movement 3,8 μs

  Total: 12.8 μs

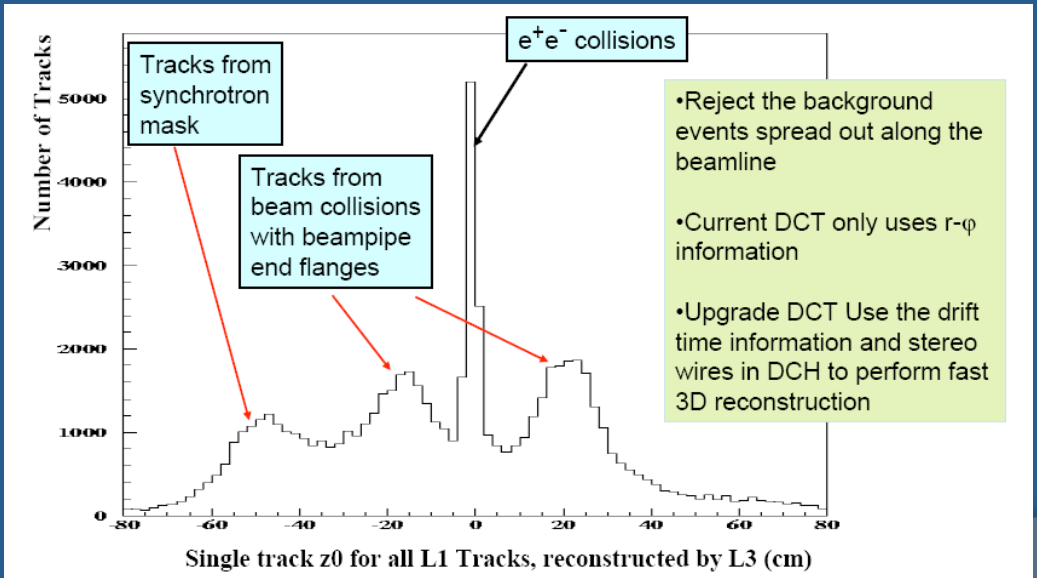
- How to reach about 6 μs ?

- Latency of the system is dominated by DC processing. It depends on how fast data processing is.
- We should be able to be faster with new FPGAs.

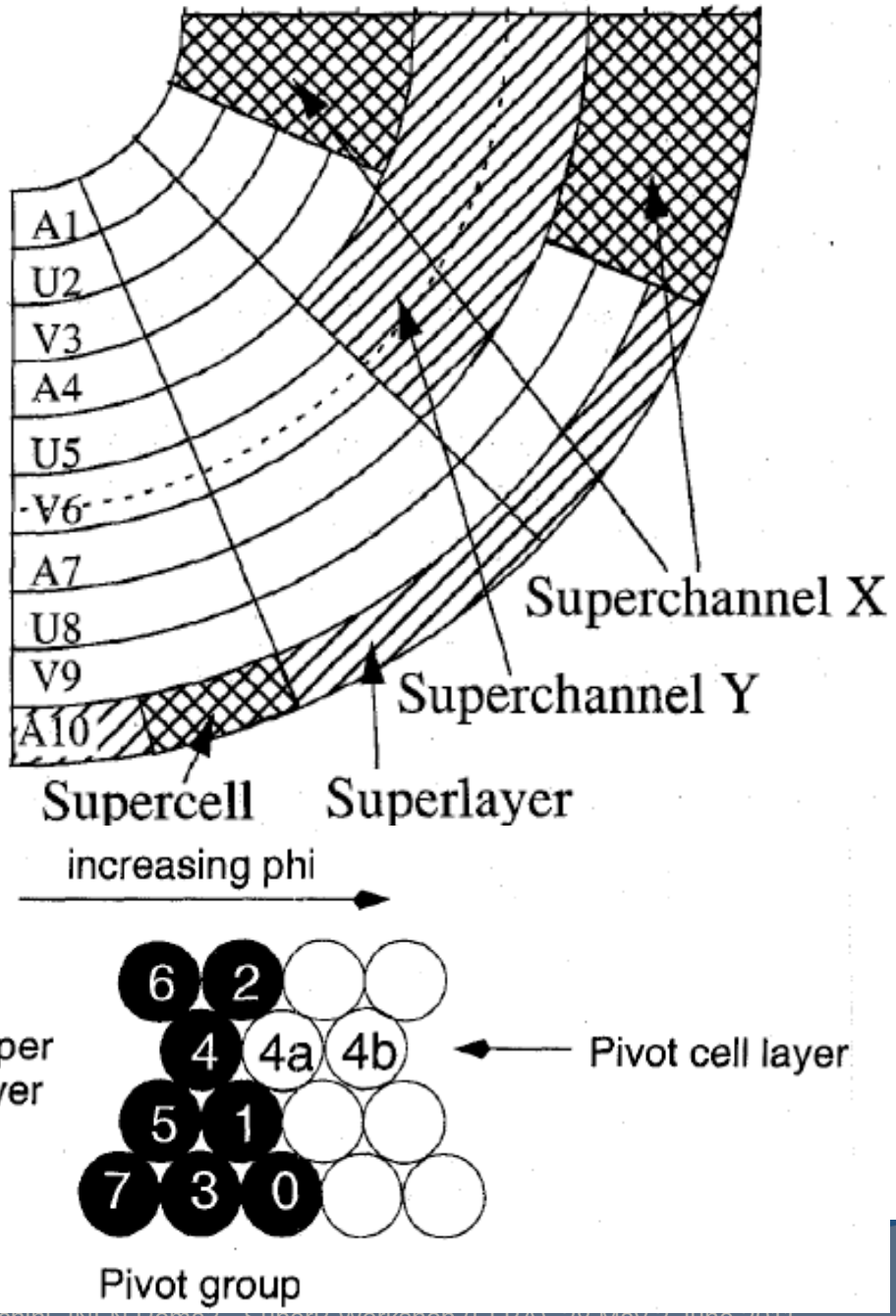
SuperB DC trigger

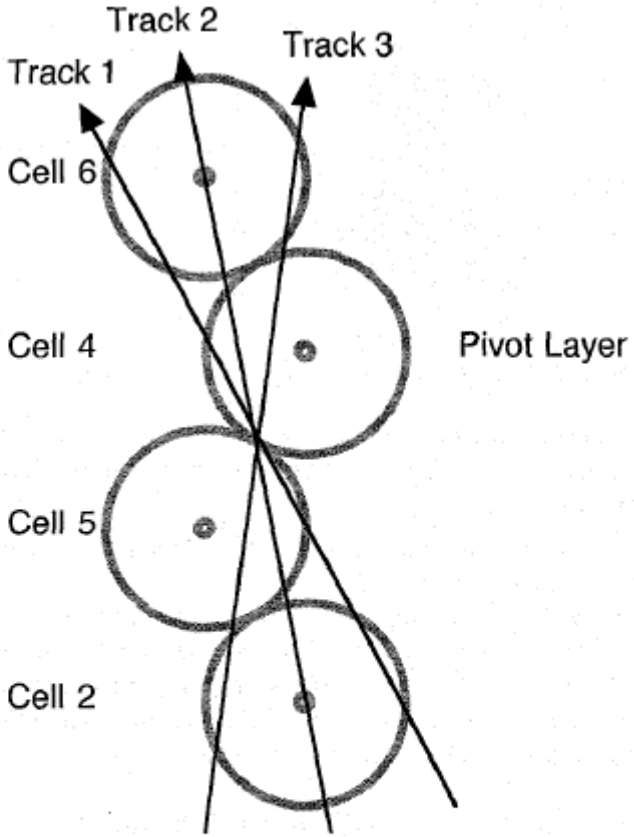
Following BaBar strategy we would like to implement fast tracking but why?

- For background reduction in L3 trigger(see picture below)
- For event classification
- Real time data quality check and detector monitoring
- ……



Z0 distrib. of triggered events before zed measurement upgrade

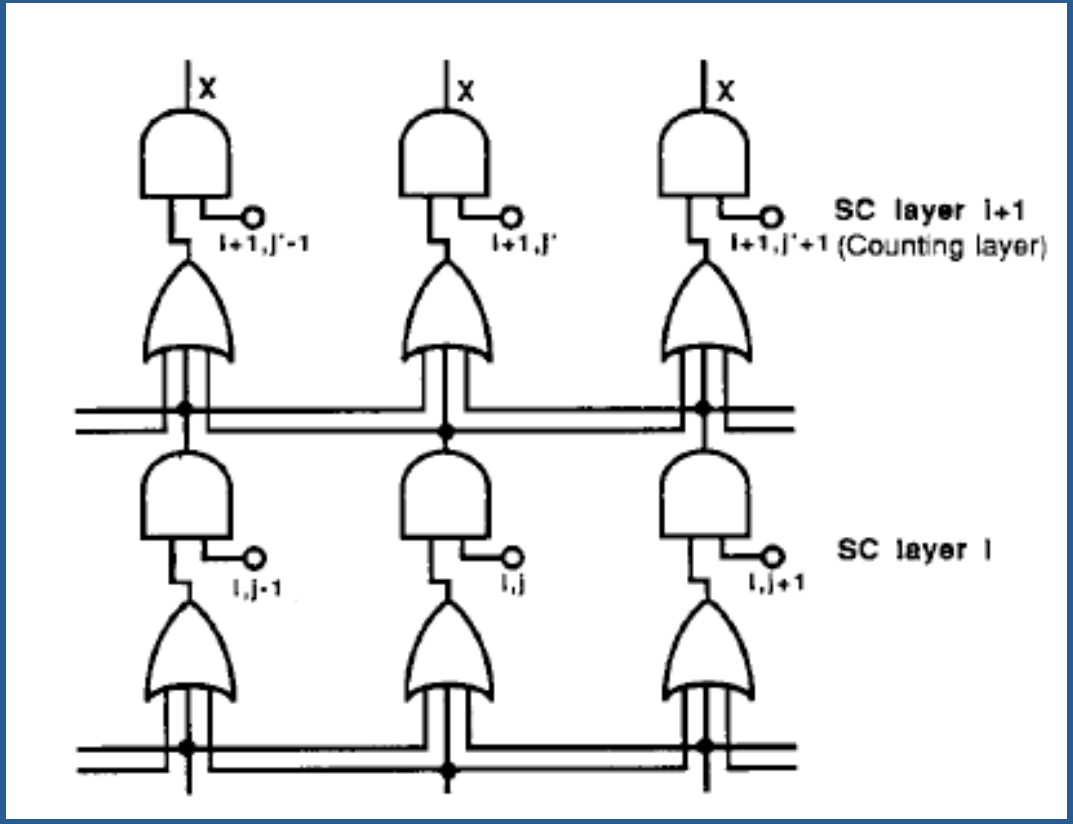




Clock 8 Ticks

Cell	T0	1	2	3	4	T0	1	2	3	4	T0	1	2	3	4
6	0	0	0	1	2	0	1	2	3	0	0	0	0	1	2
4	0	0	0	1	2	0	0	0	1	2	0	0	1	2	3
5	0	0	0	1	2	0	0	0	1	2	0	0	1	2	3
3	0	0	0	1	2	0	1	2	3	0	0	0	0	1	2
	Track 1					Track 2					Track 3				

Track finder



DC track finder algorithm

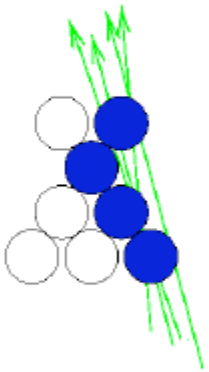
Use drift time information to better determine track postion and event time

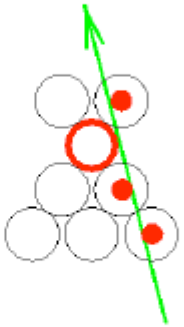
Utilize the 267ns sampling
over the max ~1ms drift time

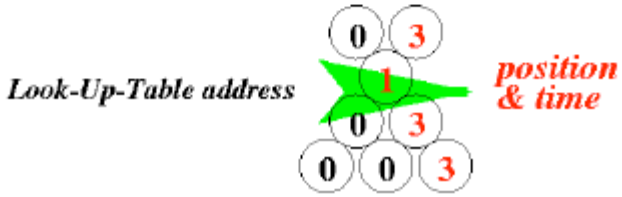
⇒ 0.8mm spatial resolution
for a segment

Translates to ~1.5cm δ_Z
for stereo layers.

One - shot *versus* ***Counter - Based***



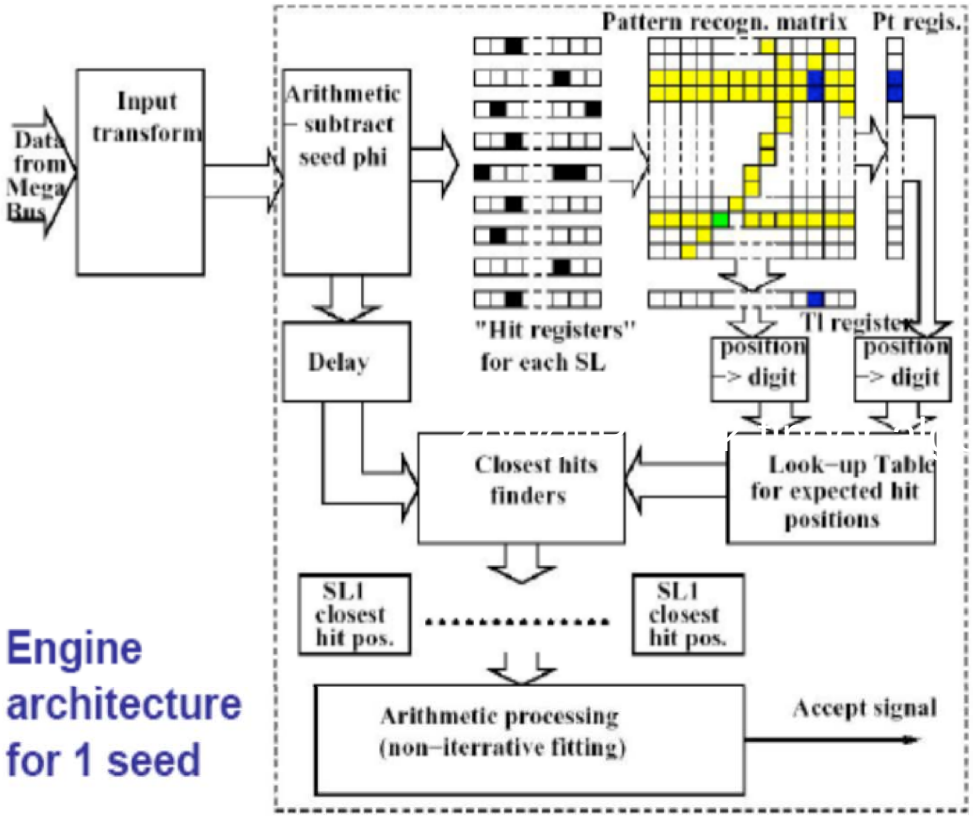




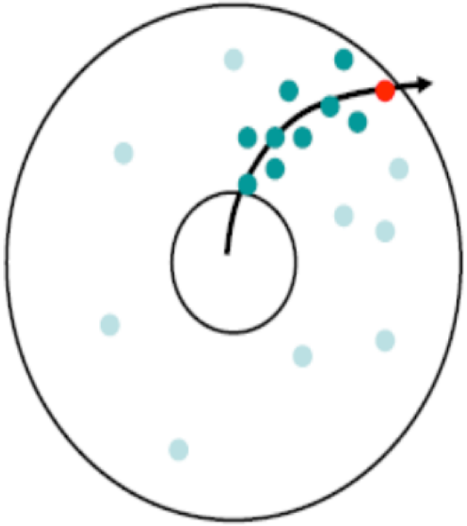
Faster sampling means better precision
(if the gas mixture is the same) do we need it?

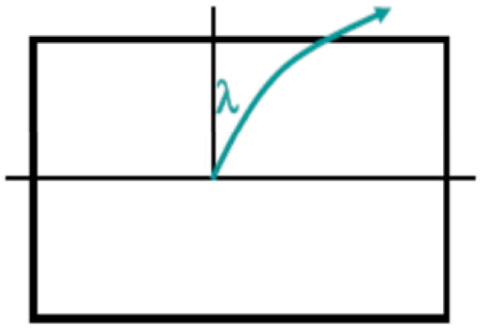
Chai 2004

Zed@IP track finder algorithm



Engine architecture for 1 seed





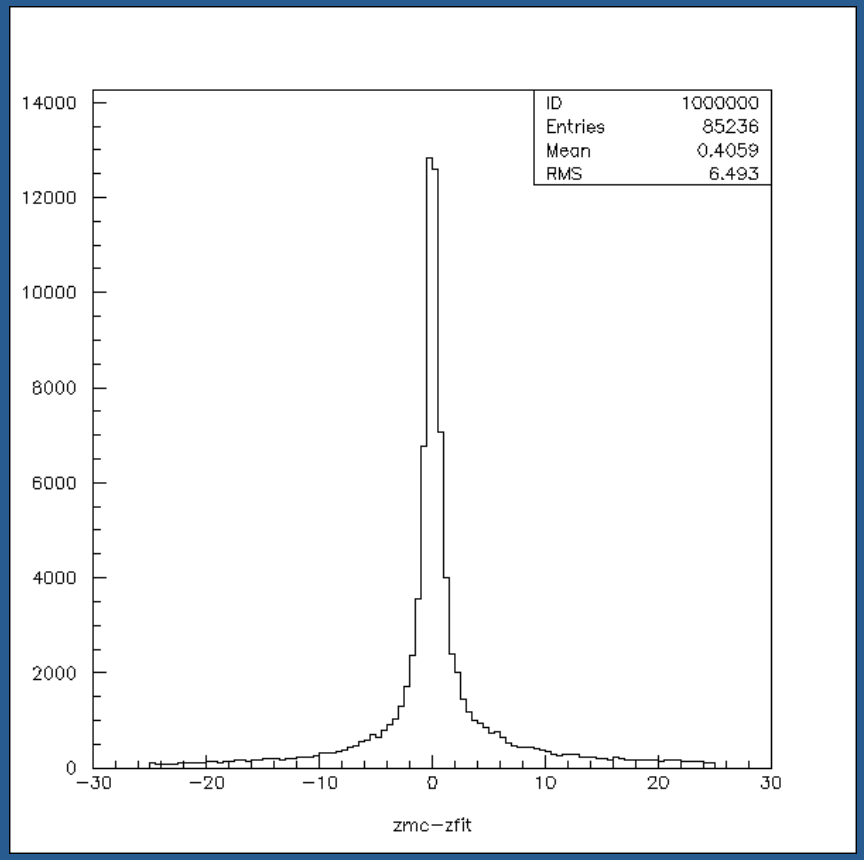
Pattern recognition: by *Hough transform*

Seed segment and IP pin track arc.Other segments on track can be represented as a line in (tanλ, Pt) space.

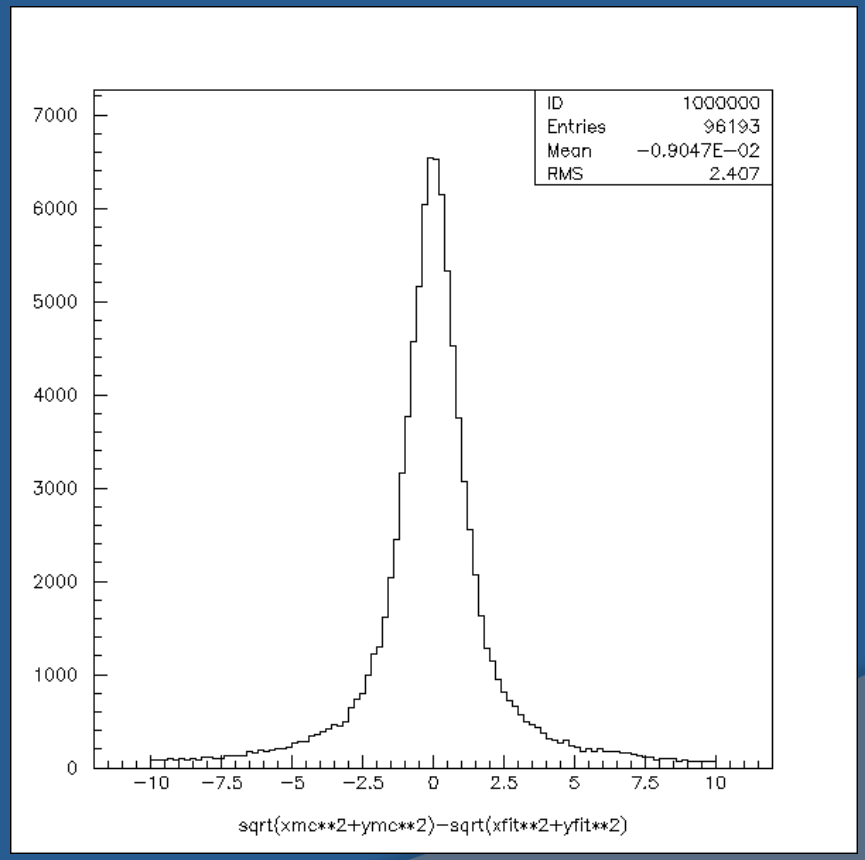
Coincidence of hits from many layers with same tan λ,Pt identifies Track.

What we get in the B-> D* K sample

Zed resolution RMS=6.5 cm

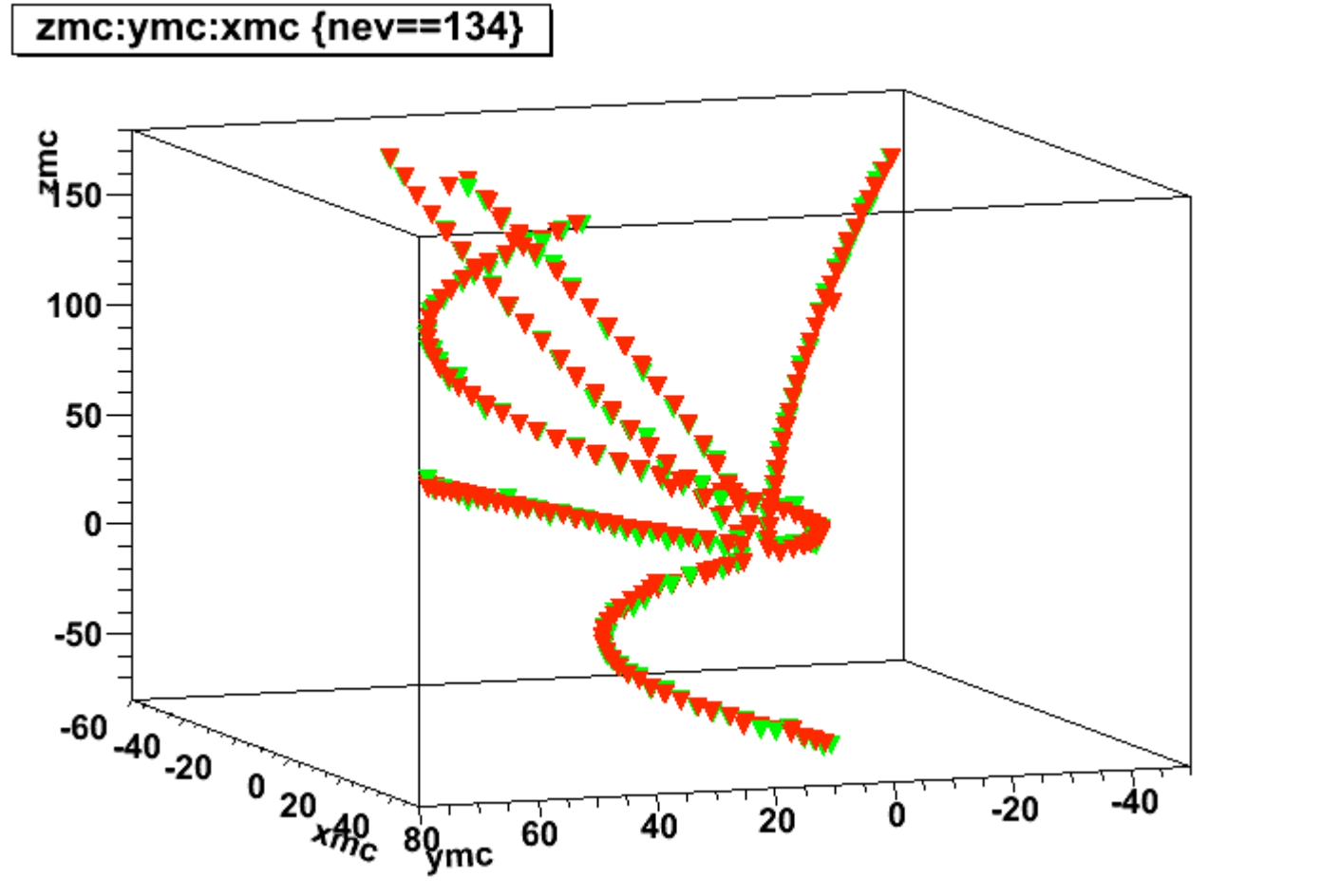


R resolution RMS = 2.4 cm



Hypothesis: error on x coordinate = error on y coordinate : gaussian, sigma 0.8 mm
error on z coordinate : gaussian, sigma = 1.5 cm

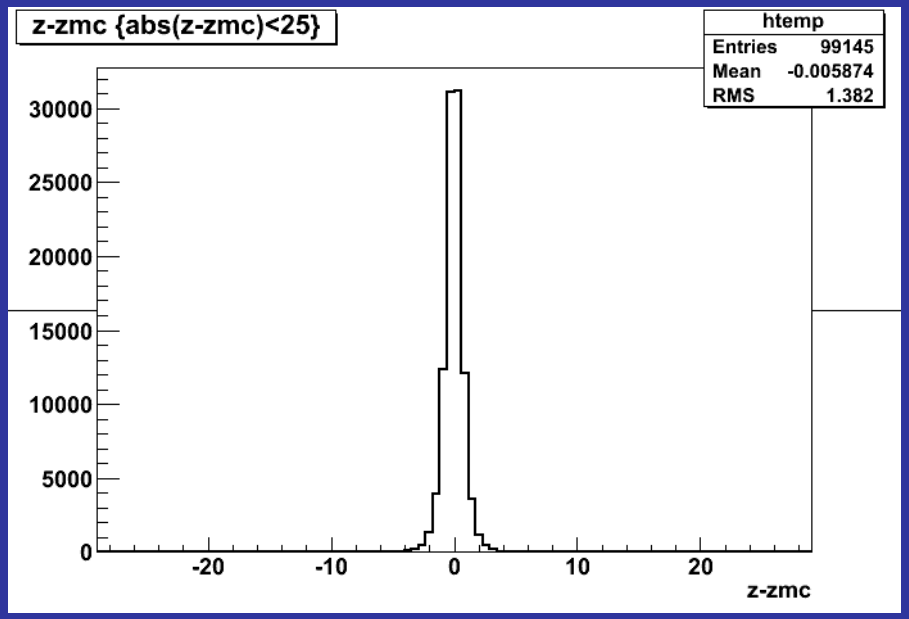
τ sample



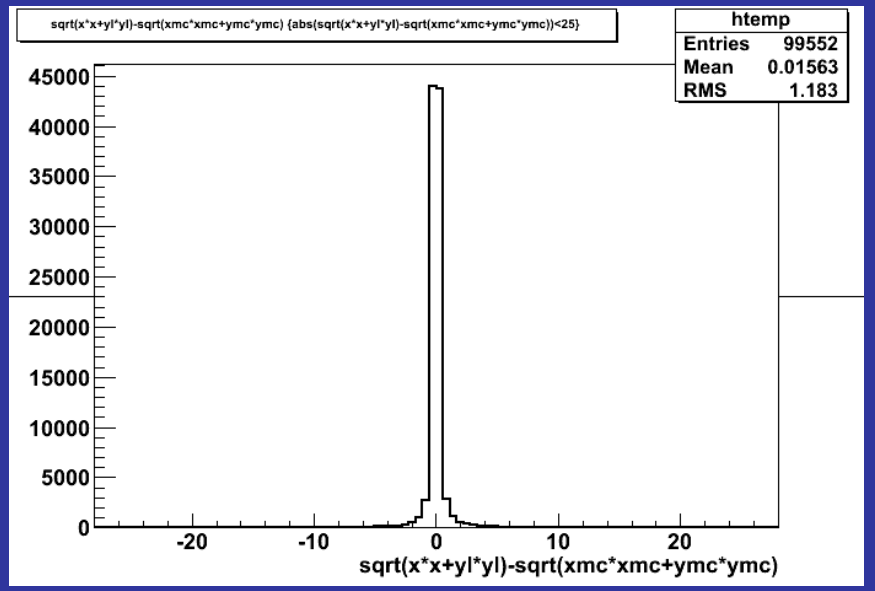
Red: fast reconstruction , green MC

What we get in the τ sample

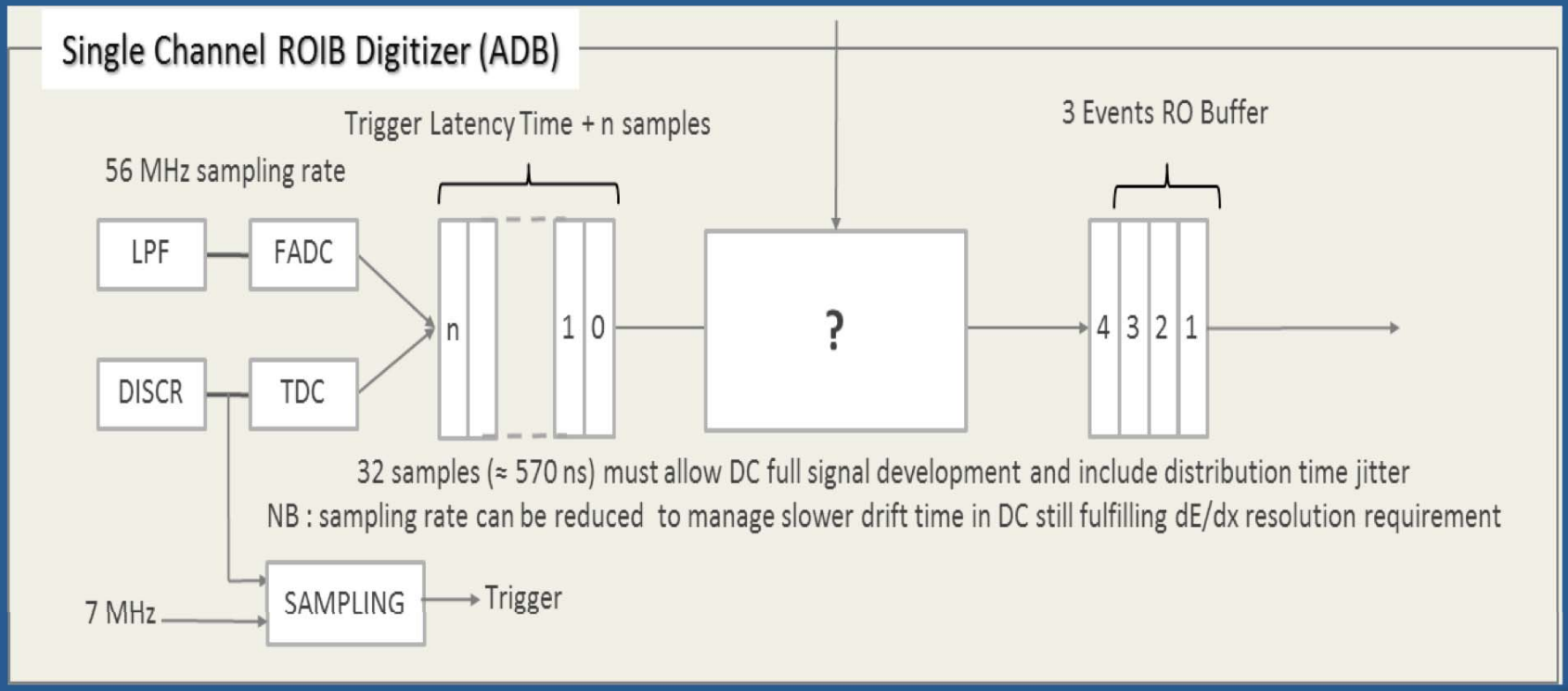
Zed resolution RMS=1.4 cm



R resolution RMS = 1.2 cm

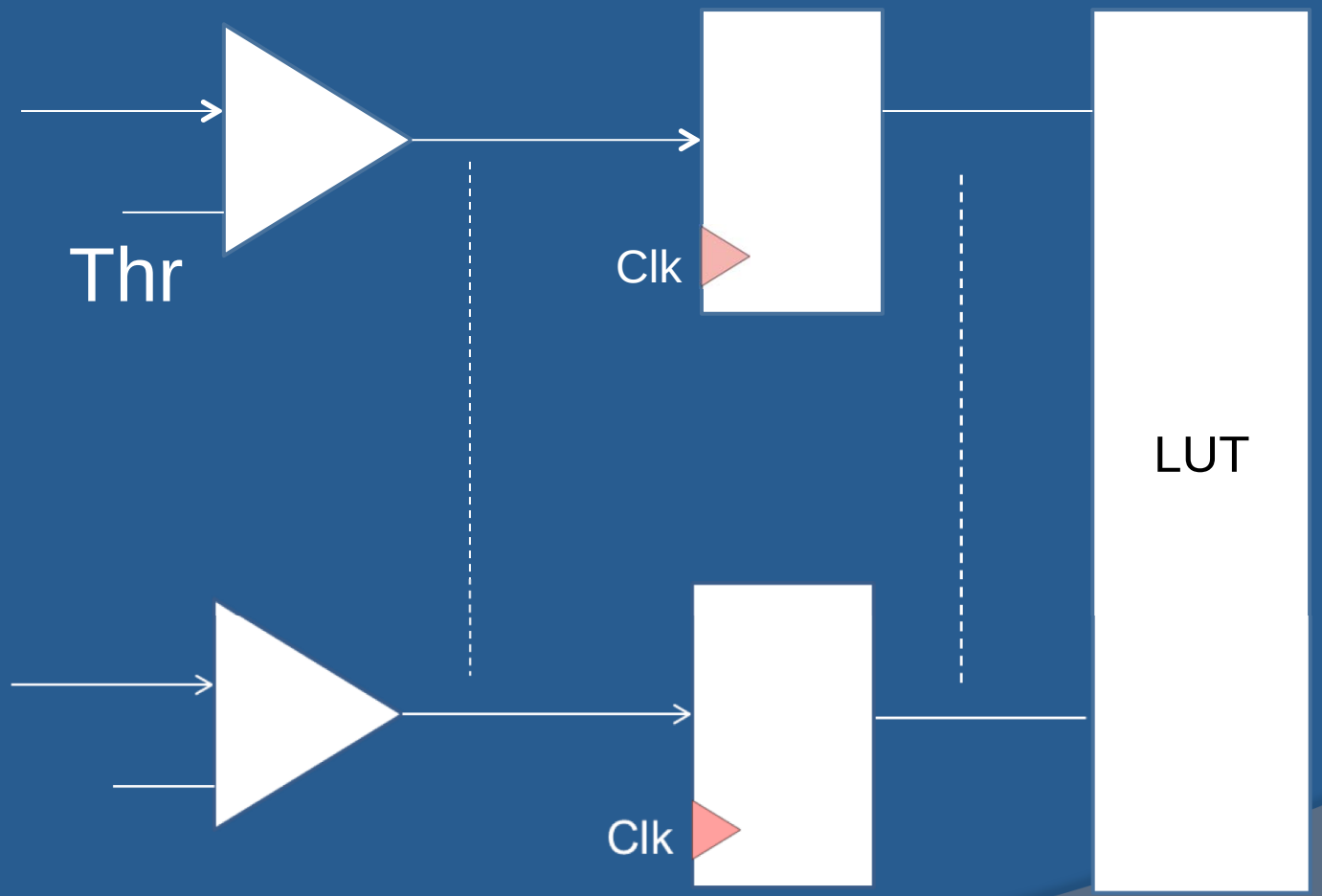


DC daq and trigger paths



A dedicated path for the trigger is already foreseen for the DC.

Trigger Path



dedicated trigger path

The information from the fast path feeds a 1 bit flash adc (a prototype is being drawn by Roma3).

The sampling frequency should be optimised

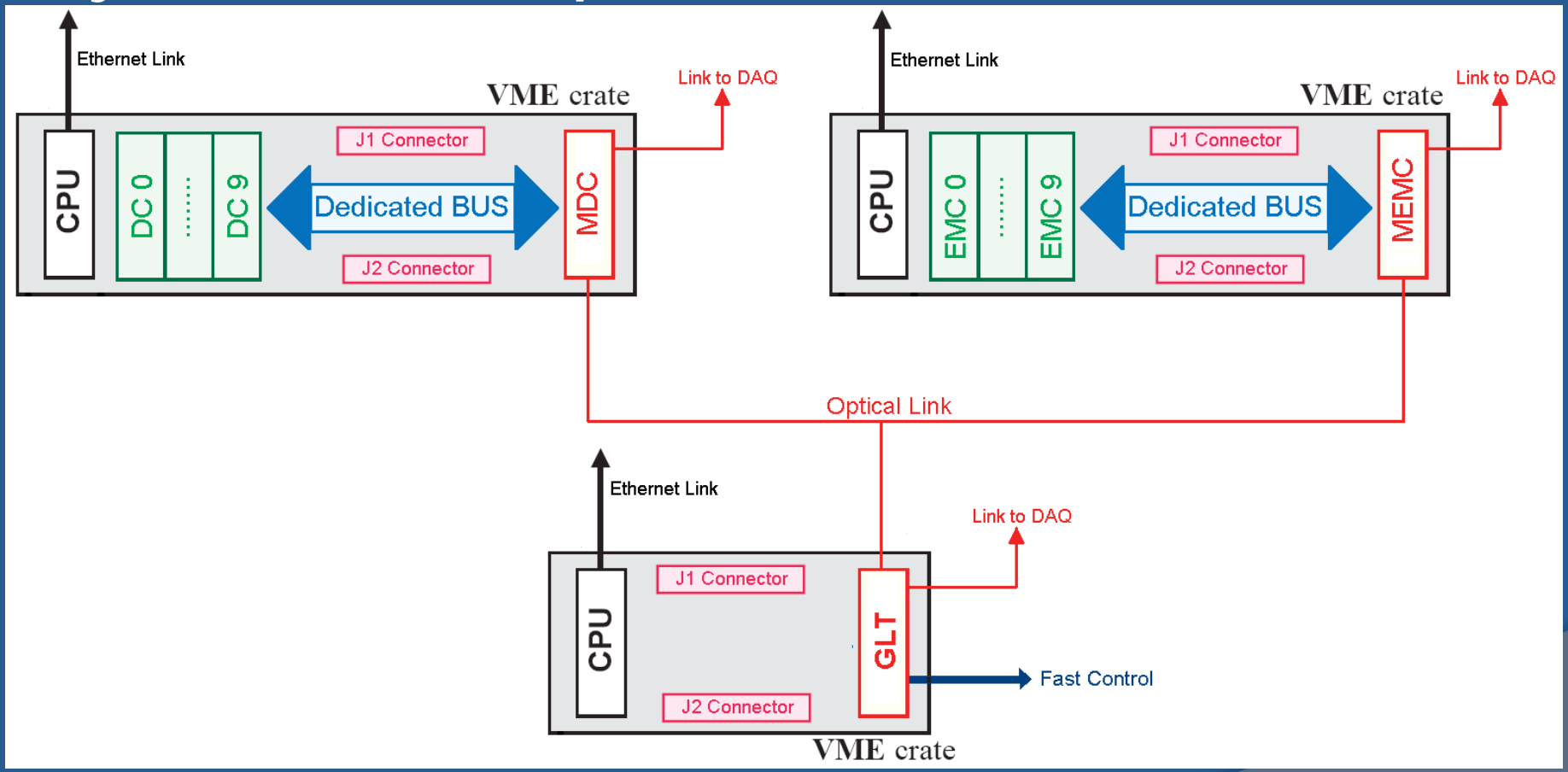
Possible range:(from 3.5 to 56 MHz).

In the prototype we would like to be able to vary the sampling frequency.

We would like to test prototype and strategy on the LNF DC prototype.

These bits (one for each wire) are delivered to a FPGAs via LVDS links (EMC like).

A possible sketch of trigger system in SuperB



DC and EMC trigger crates have a common inteface (LVDS or optical) with pertaining sub-detectors. EMC(i) and DC(i) boards share a common hw platform and only differ in firmware.

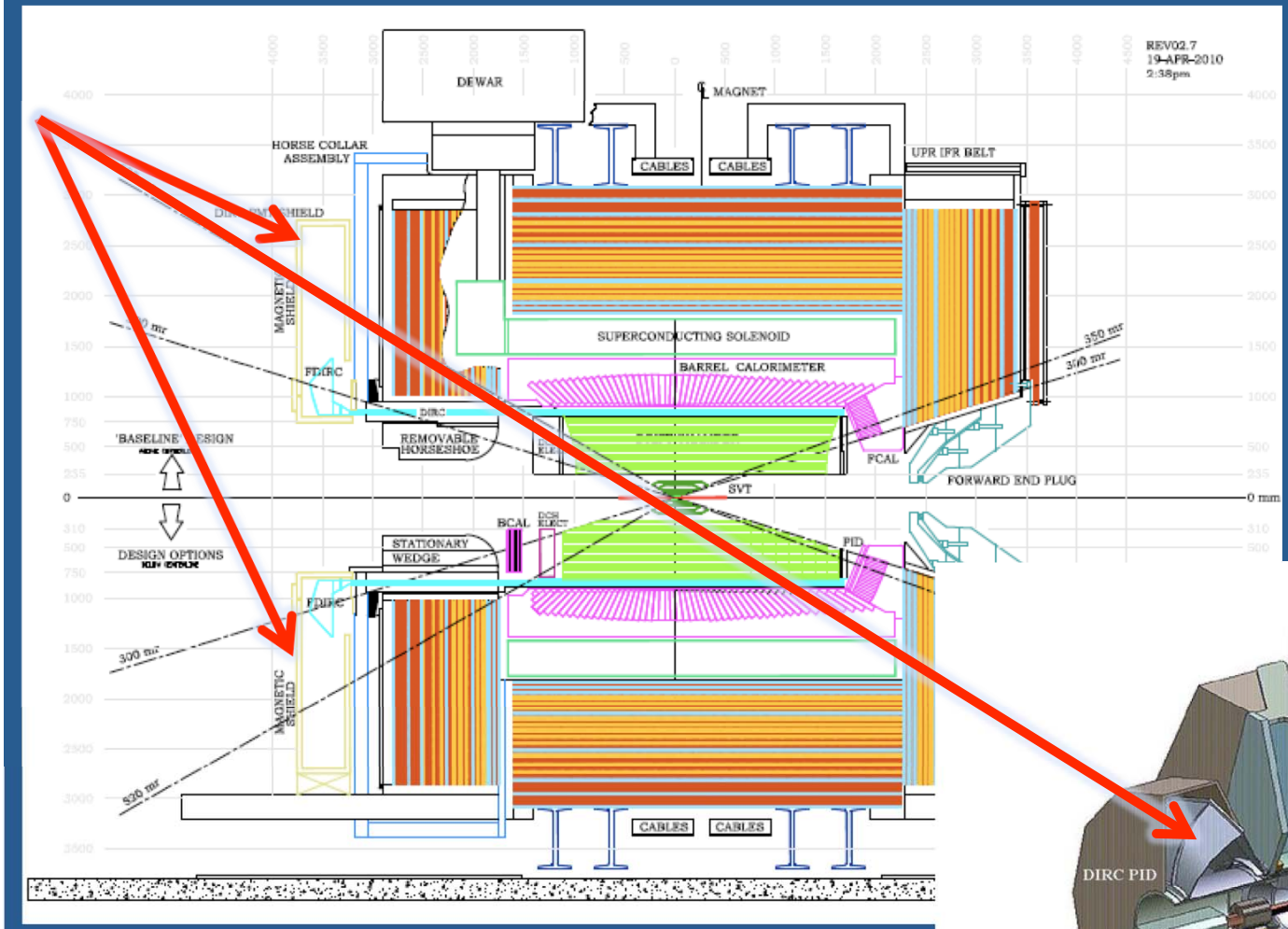
Do we need rad hard equipment?

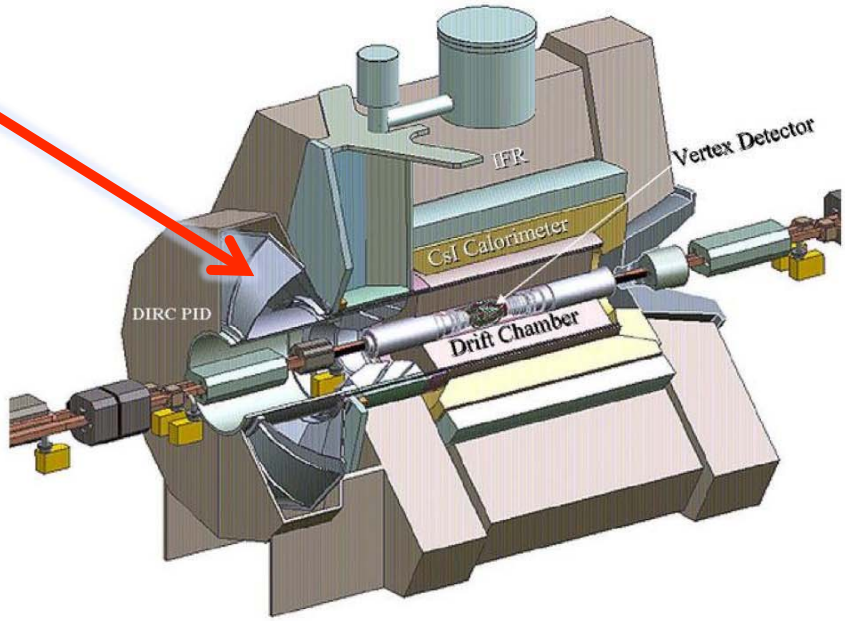
I’m not completely convinced.

We could extensively make use of protocol correction error, thus avoiding to use real rad hard equipment if not strictly necessary.

Moreover we could also think to house the most critical part of the radiation sensitive hardware in a shielded zone.

For instance...





Thank you for your kind attention !

Latency in the EMC Barrel

	(μs)	(μs)
Preamplifier	0.1	
CARE Sample and Hold	0.3	
ADC Clock-through	1.1	
Transmission to UPC	0.2	
UPC Tower Summing	0.5	
Transmission to EMC Trigger	0.1	
Total before EMC Trigger		2.3
Synchronisation	0.1	
Summing ϕ, X, Y	0.4	
Summing Nearest Neighbours	0.4	
Filter Calculation	0.8	
Zero-Crossing Time	1.9	
Gating of Global Maps	0.4	
Average Jitter Gate Stretch	0.5	
Transmission to Global Trigger	0.2	
Total within EMC Trigger		4.8
Total		7.2

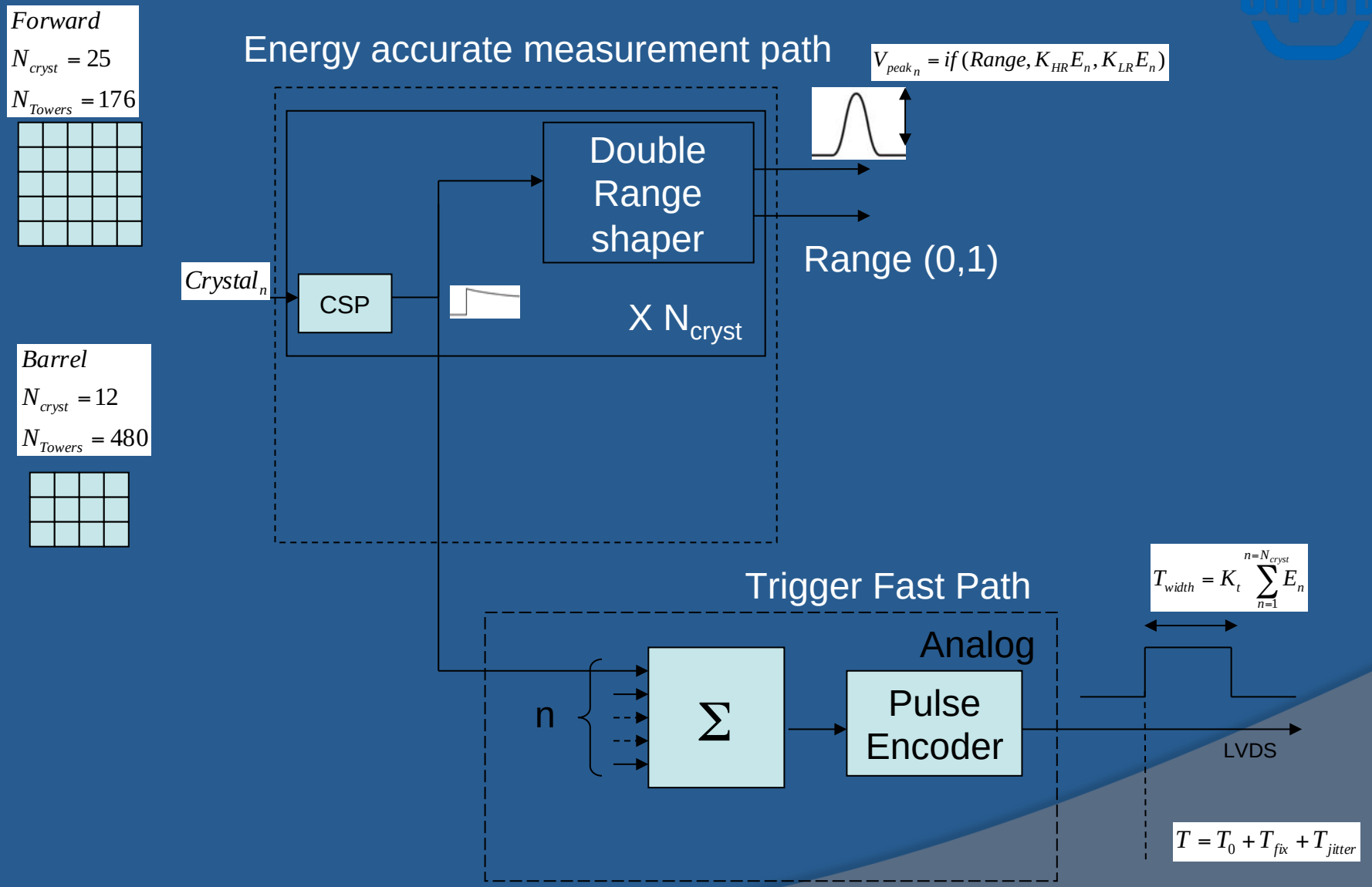
ADC conversion time.

Depends on Shaping, can it be changed?

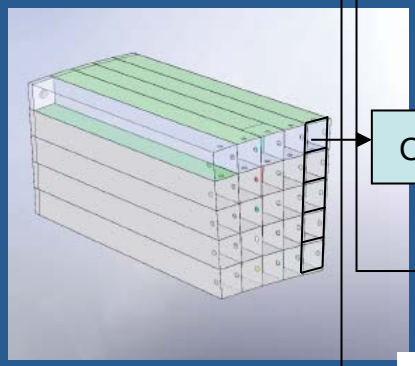
J. C. Andress et Al., “Babar Calorimeter Level 1 Trigger Design” , BaBar Note (1998)

Can we improve latency here?

EMC fast trigger path and energy one



EMC forward tentative implementation



CSP

X5

5 input

Σ

VFE

X5

Double Range shaper

X5

Range

VME Range Shaper

New Circuit Analog Sum over 5 input.

5 input

Σ

Analog Pulse Encoder

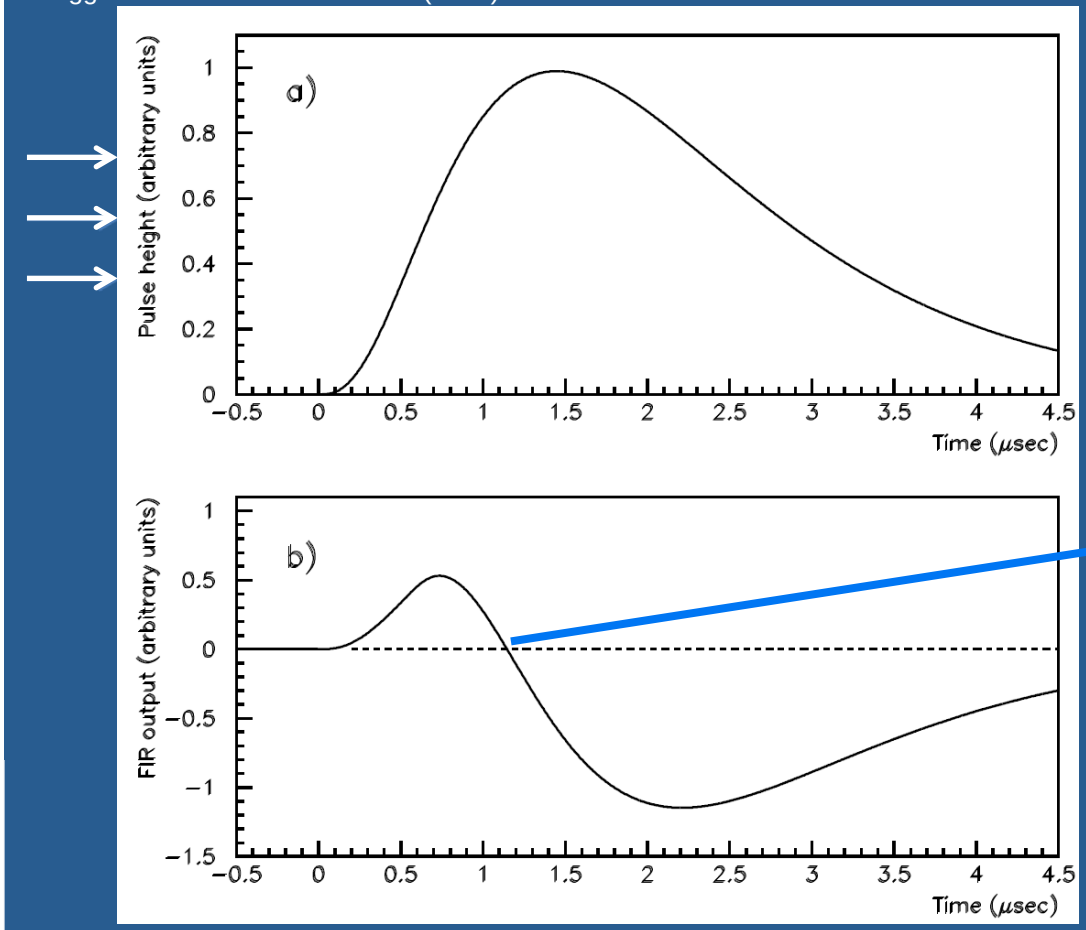
LVDS

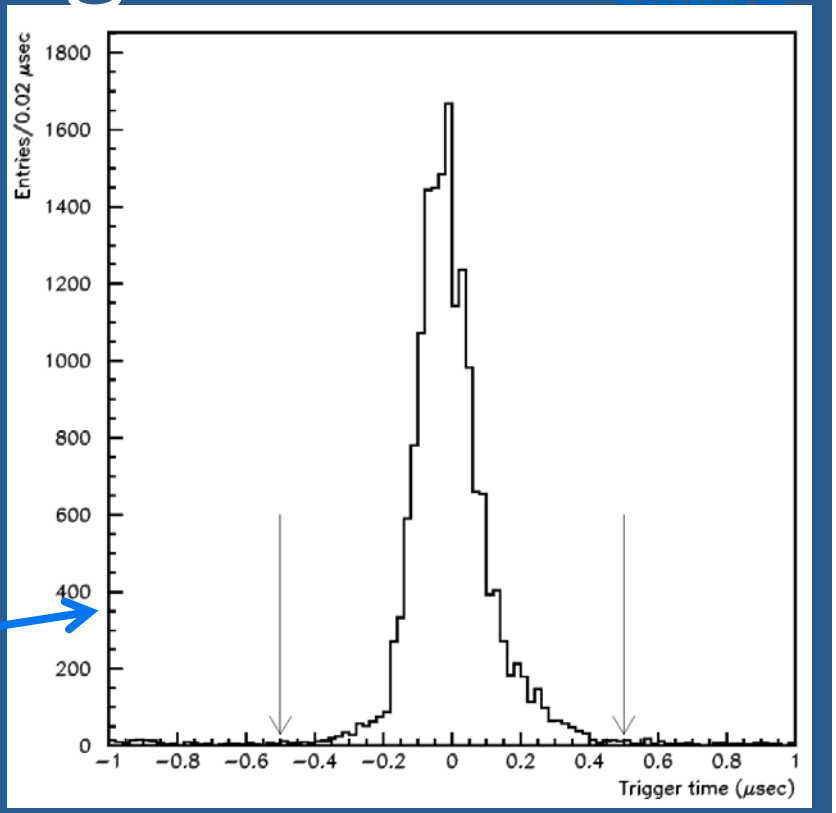
$T = T_0 + T_{fix} + T_{jitter}$

Trigger Tower module

Barrel CsI (Tl doped) original BaBar

P. D. Dauncey et Al., "Design and performance of the level 1 calorimeter trigger for the BABAR detector" (2001)

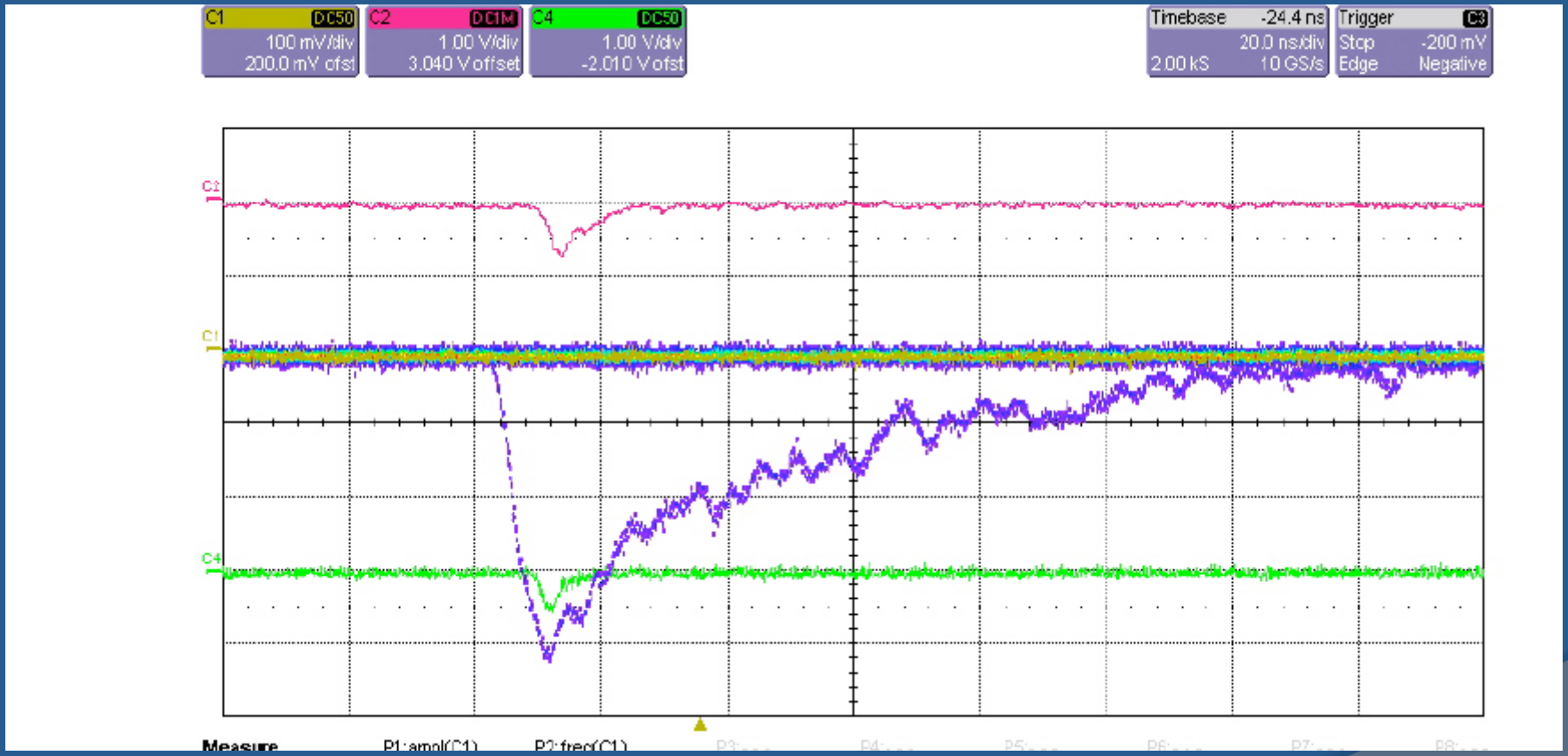




The plot shows the difference between the EMC trigger time and the DC trigger time.
μ+μ- events used to select good resolution in DC.

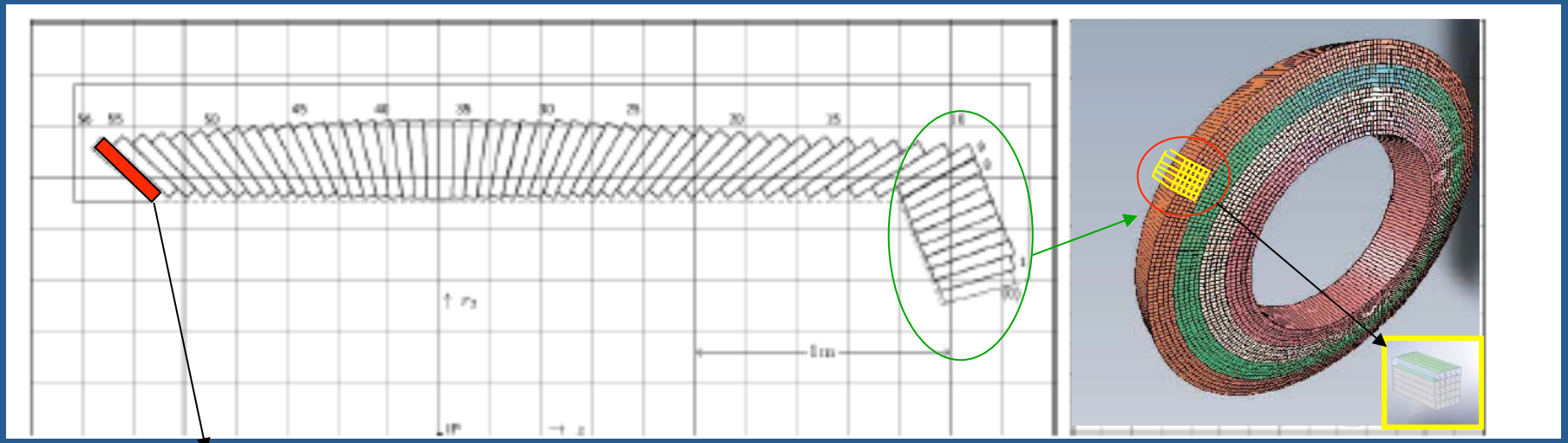
A FIR Filter with 8 parameters was applied to the signal. Its zero-crossing occurred at roughly a fixed time distance from the start of the signal, it was used to gate the threshold information. Due to this mechanism the time resolution was about **100 ns**.

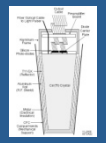
Forward Lyso signal



The Lyso has been read out by a PMT (signal lasts 150 ns)
we should not have problems here. Moreover a resolution on 1 ns has been reached on the peak charge distribution at CERN test beam.

SuperB EMC





EMC Barrel :
5760 CsI(Tl) Crystals

EMC Forward =
4400 Lyso Crystals
(176 modules)

Comments I

- The afore mentioned strategy worked fine for BaBar.

  Unfortunately latency is dominated by adc conversion and peak finding.

  Peak finding determined time jiitter too.

  We really should try to improve this part.

Comments II

- At the moment we could immagine to assert a trigger signal using only a part of the energy deposit in the CsI.

  Resolution could be worse by the sqrt(energy fraction collected).

  But we do not have any crystal to play with.

We are waiting for a small sample of BaBar crystals From Bill