Testing Rad-Tolerance of Serial Links Based on Xilinx FPGAs with a SEU Emulator

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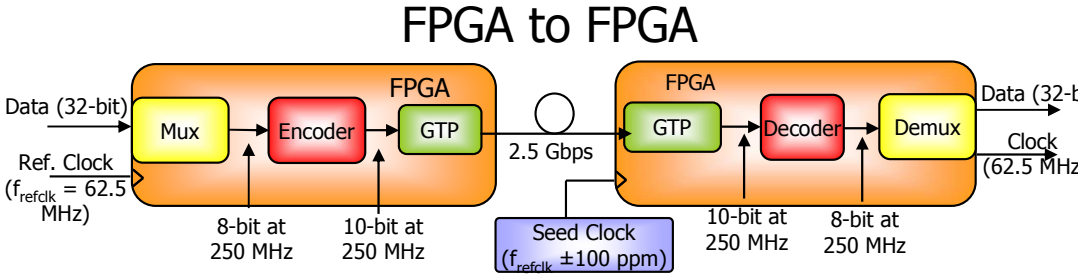
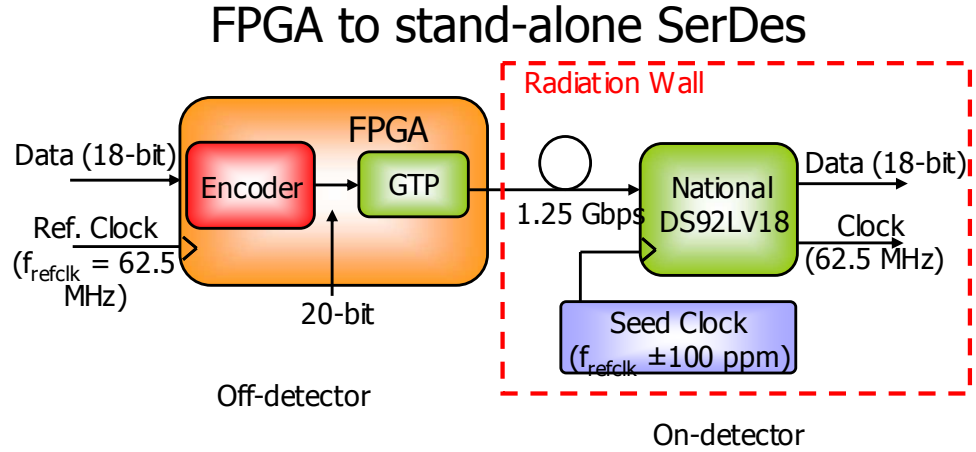
Outline

- Present (foreseen) architecture of fast links
- Benefits of homogeneous FPGA<->FPGA links
- FPGAs and radiation issues
- SEU emulation for tests in lab.
- Test bench architecture
- Error results and recovery strategies
- SEU->bit-flip cross-section and link error estimate
- Conclusions

Present Architecture of SuperB Links

- In the present ETD architecture, fast links can be divided in two types:
  - Symmetrical links for transfers in the off-detector area: FPGAs on both sides of the link
  - Hybrid links for transfers to and from the detector: stand-alone serdeses on-detector and FPGAs off-detector
- for further details see white paper





Can We Use FPGAs On-Detector ?

- S-RAM FPGAs traditionally excluded from radiation areas
  - Configuration is stored in a static RAM
  - Static RAM is sensitive to single event upsets (SEUs) => bit-flips
  - A bit flip in the configuration memory might change design functionality
- This problem can be mitigated by correcting the configuration
- Mid-range Xilinx FPGAs include tools for error detection and correction

What if FPGAs Could be Used

- The fast link sub-system will be dramatically simplified: we would only have symmetrical links! (FPGA<->FPGA)
- No constraints imposed by line encodings of stand-alone SerDeses (i.e. start/stop bits of DS92LV18 and 8b10b coding TLK2711-A)
- Just one type of links, protocol and line coding customized to ETD requirements
- Fixed-latency proof and thoroughly tested
- Artix-7: cheap Xilinx FPGAs (~ 40$) with ~ 8 embedded SerDeses (GTPs)
  - More than one link per chip
  - Data-rates up to 3 Gbps on all links (including FCTS)
  - (actually SerDes could go even faster : 6.6 Gbps)
  - # of links could be halved or better

Need to Estimate Rad-Tolerance

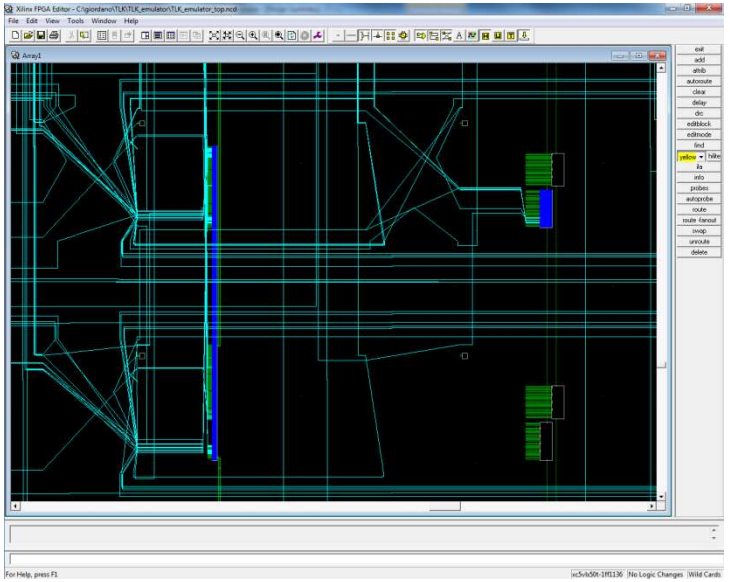
- Two kind of issues :
  - Total Ionizing Dose (common to all ICs)
  - SEUs
    - Logic errors
    - Configuration errors
      - Lab test (SEU Injector)
      - Beam test
- However, configuration SEUs have been largely over-estimated in the past: they rarely impact the design functionality
- In this talk we will not cover logic errors, they are common to every digital device

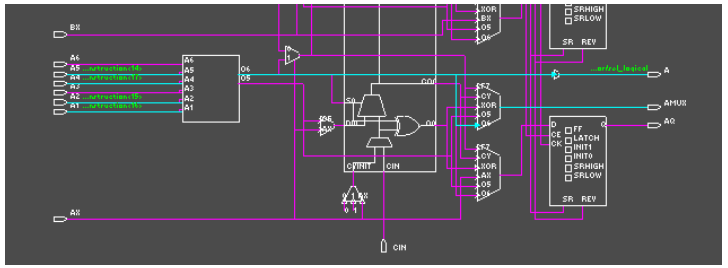
Device

- Xilinx Virtex 5 LX50T
  - Includes high-speed SerDeses
  - Mid-range size, yet large enough to fit our needs
  - Tested by Xilinx, NASA, Lawrence Berkeley Lab. and Los Alamos Lab.
  - Embeds configuration CRC with ECC blocks and partial reconfiguration capabilities
  - Two versions: rad-hard (70k$) and industrial (400$) (we focus on the latter, guess why)

Device Facts

- Configuration size 11.37 Mbits
  - CLBs&routing ~ 9 Mbit
  - IOB, DSP, BRAM-interconnect ~ 2.37 Mbit
- Clock cycles per Readback 355,190
- Readback time 7.1 ms (at 50 MHz)



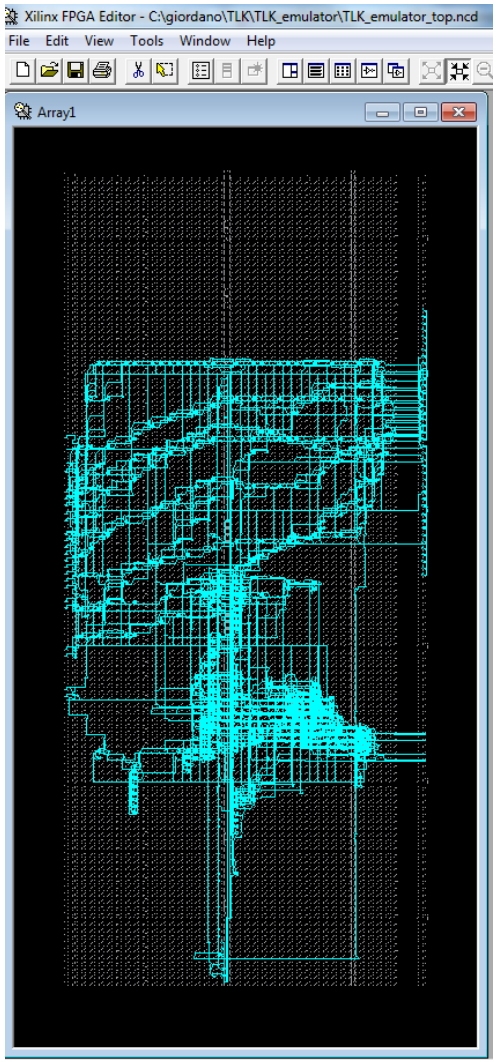


Emulating Configuration SEUs

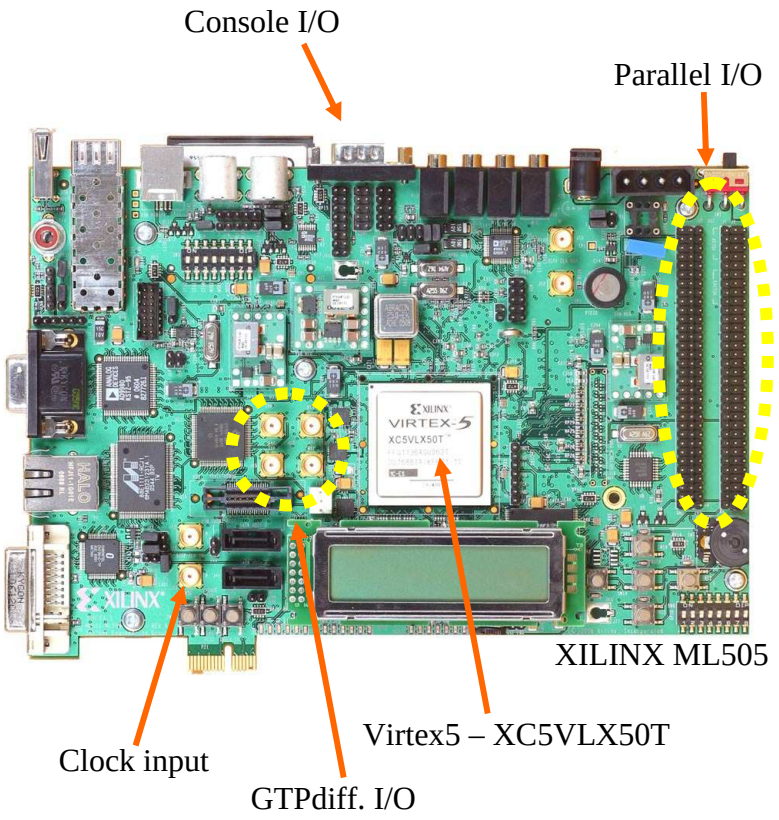
- Investigate impact of configuration SEUs on design functionality
  - Flip configuration bits by means of internal configuration access port (ICAP)
  - Optional error correction thank to integrated CRC calculator and ECC (FRAME_ECC)
- Programmable integrated controller:
  - SEU generation without correction (error accumulation)
  - SEU generation and on-the-fly correction
- Custom design derivative of a Xilinx core (so called SEU Controller)

Benchmark Design

- Serial Link running at 2 Gbps (compatible with the TLK2711-A)
  - 16-bit parallel words (18-bit including control bits)
  - 100 MHz parallel clock
  - 8b10b encoding
  - Explicit lock flag
- Dummy Logic on Tx and Rx parallel data-path to observe realistic SEU effects
  - 2x 16 levels of 18-bit registers and combinational logic
- SEU Controller
- Resource Occupation
  - GTPs : 1 (10%)
  - Slices: 376 (5%)
    - FFs: 926 (3%)
    - LUTs: 980 (3%)
  - BRAM: 1 (1%)
  - PLLs: 1 (16%)
  - Clock Buffers: 6 (18%)
  - IOBs: 47 (10%)

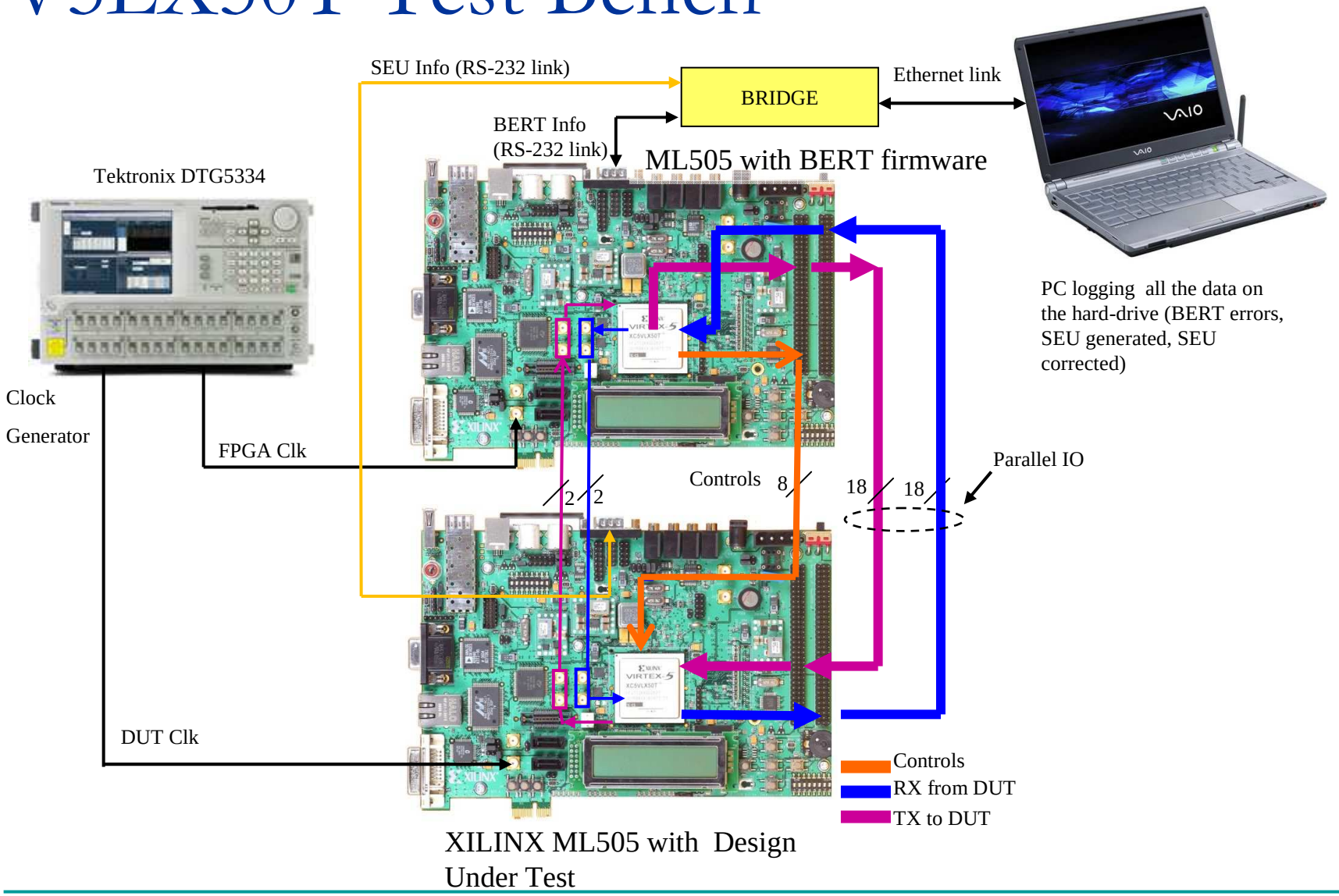


Tester Board



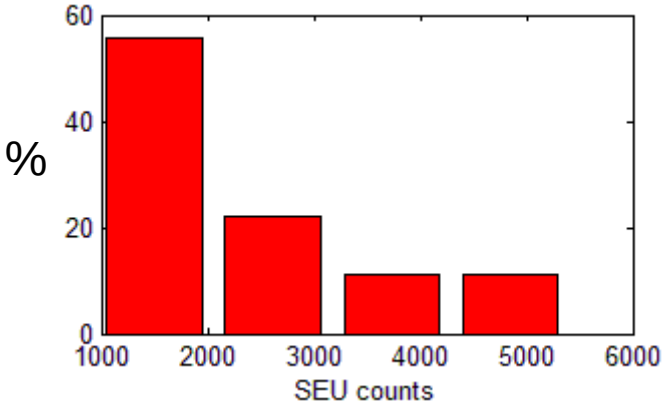
- Two identical off-the-shelf boards (Xilinx ML505) used for implementing the tester and the Design Under Test (DUT)
- Data pattern stored in the FPGA firmware
- TX and RX sections of the benchmark link design are tested independently and simultaneuosly
- Console IO
  - Status and errors are logged on a console handle by an embedded micro

V5LX50T Test Bench



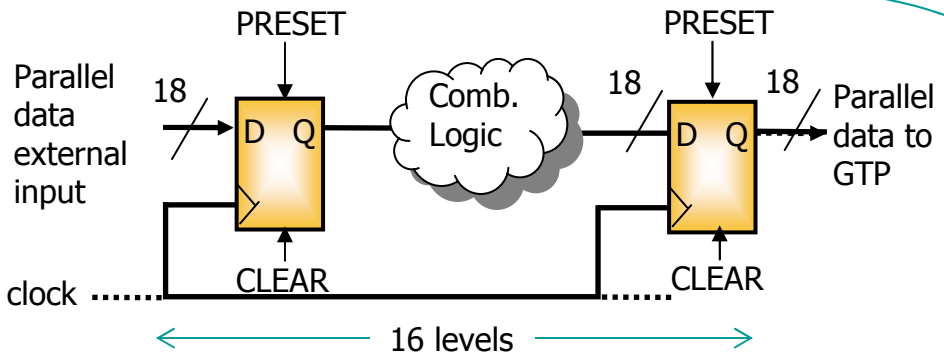
SEU Accumulation Test Results

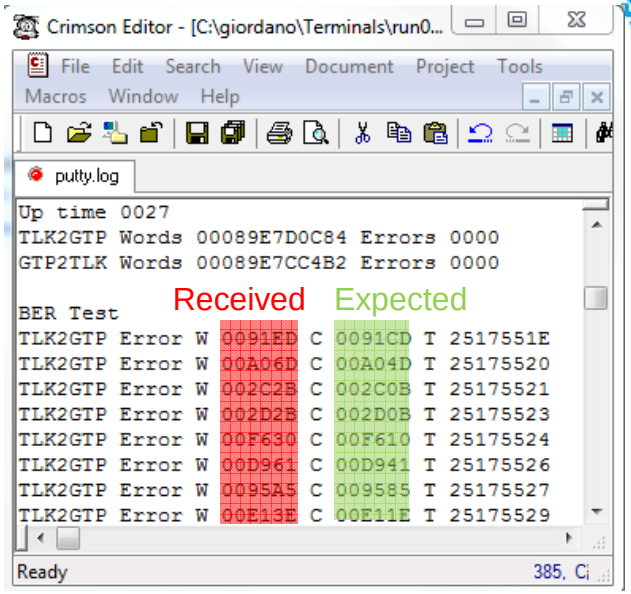
- SEU generated at 20 Hz
- We measured # of SEUs before failure
- On average 2250 SEUs needed to observe BERT errors

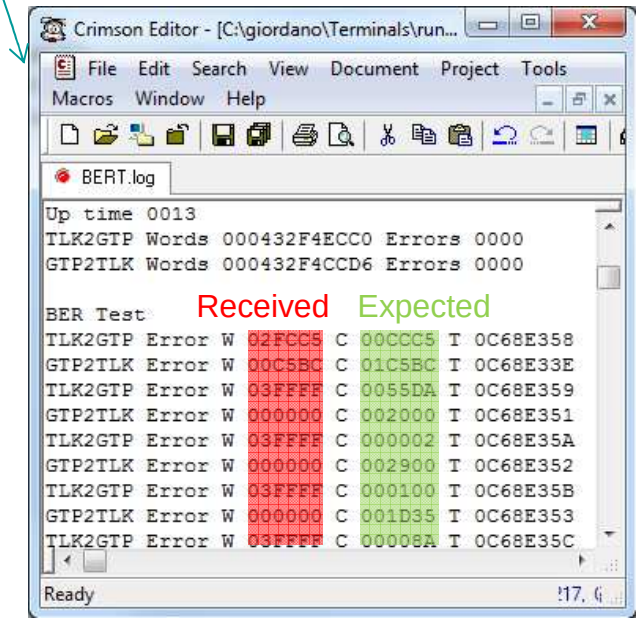


Errors Anatomy

- Different errors
  - Single bit gets stuck
  - Whole bus gets stuck



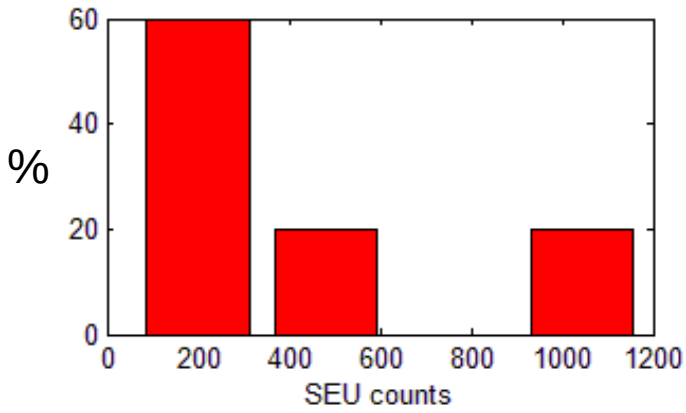




- Possible causes
  - Preset/Reset stuck ?
  - Node open, stuck@GND or @V_{DD} ?
  - Missing clock? (for 'whole bus stuck' errors)

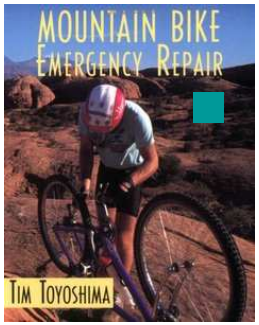
SEU Generation&Correction Results

- SEUs generated at 1 Hz (due to limitations of the original Xilinx SEU controller)
- Measured # of (generated&corrected) SEUs before failure
- On average ~ 400 SEUs needed to observe BERT errors
- Very likely the difference is due to reconfiguration=>even correctly working blocks are affected

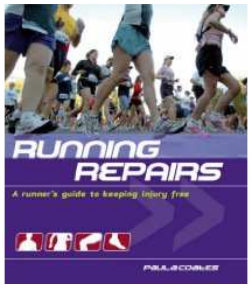


Recovery Strategies

- Scheduled maintenance
  - Reconfigure the FPGA at regular intervals, e.g. once a day, no matter what



- Emergency maintenance
  - Reconfigure as soon as the service can be interrupted, e.g. exploit any reset or power-cycle of the link to reconfigure

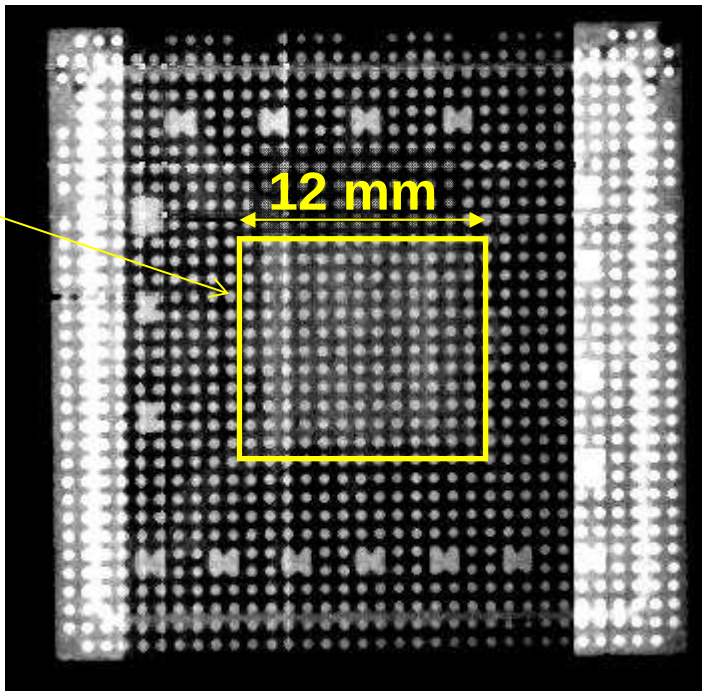


- Repair-while-running
  - Partial reconfigure as soon as the error is detected, even if the link is working => interruptio of service, i.e. dead time

Configuration Bit-flip Cross-section

- V5LX50T device
  - Die size = 1.4 cm^2
  - p @ 62MeV : $\sigma = 6.4 \cdot 10^{-14}$ cm^2/bit, see [1]
  - Effective x-section is design-dependent
  - For our benchmark design $\sigma_{eff} = \sigma \cdot 10^{-2}$ according to Xilinx guidelines
  - 0.5 kGy(Si)/year (a) => $4.3 \cdot 10^{11}$ protons/year on device
- ·#sys.failures/year = 125 (on average)
- Expected one link failure every 3 days (only configuration failure)

X-ray image
Package



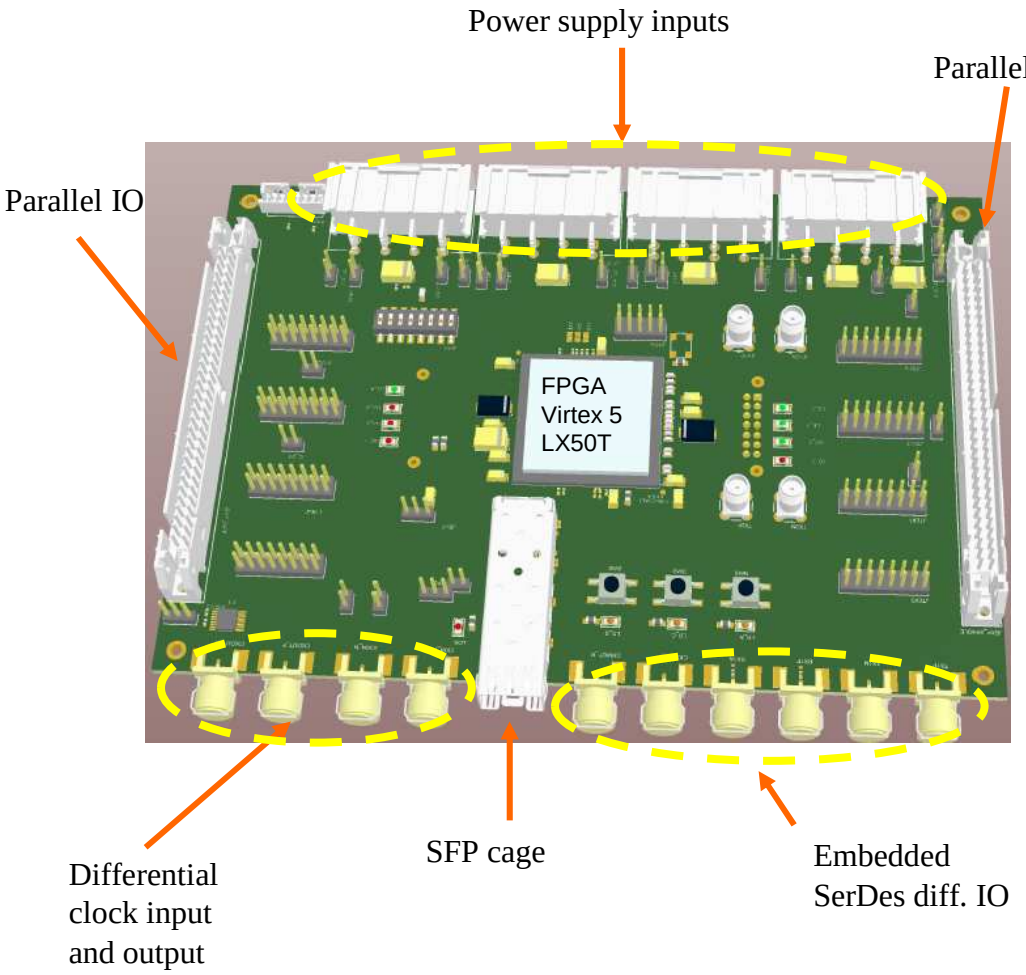
Reference:

[1] Quinn et al., Proceedings of 2007 IEE Radiation Effetcs Data Workshop, Page(s): 177-184

Note:

(a) Estimated by R. Cenci, INFN Pisa

FPGA Board for Beam Test



- FPGA board for beam test design completed, presently under manufacturing
- Compatible with the Xilinx ML505 board used for the presented lab. tests (implements sub-set of features)
- SMAs for clocking and serial IO
- No active components
- 4-wires connectors for current sensing power supply
- SFP cage for optional testing of opto-electronics

Conclusions

- Encouraging results: failure rate due to configuration upsets seems tolerable
- Test on beam scheduled on July 10th at LNS (Catania, Italy) will provide us with precious information about Xilinx FPGAs
- Design of test board for V5LX50T FPGA completed, presently under manufacturing
- Need for TID tests, likely at ENEA, La Casaccia
- Logic error mitigation (TMR, fault-tolerant FSMs)
- If FPGAs could be used on-detector, a completely new scenario will open for fast links implementation

Back-up Slides

Quick Facts

- $\rho_{Si} = 2.3\ g/cm^3$
- $(dE/dx)_{p@60MeV}$ in Si = 1.8 MeV/mm (or 600 keV in 300 μm)
- $\sigma = (1 / F) * n_{errors}$

- $N_{SEU} = (N_p * \sigma_{bit} * N_{bit(eff.)}) / * S_{FPGA}$
- $N_{sysfail} = N_{SEU} * N_{SEU->failure}$