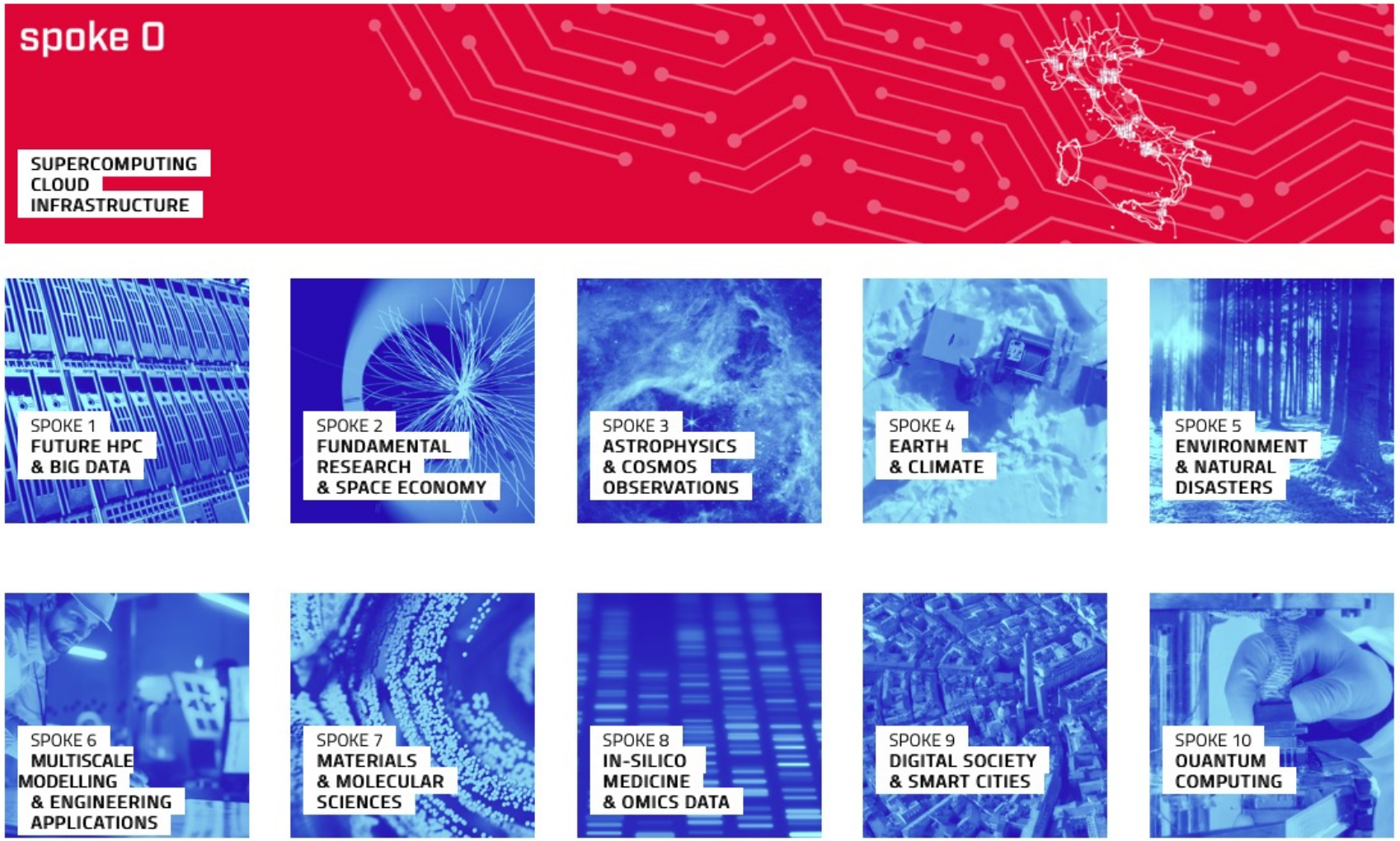
Quantum Computing With SC Qubits At The National Centre For High Performance Computing

C GATTI

National Centre For High Performance Computing, Big Data and Quantum Computing

- The National Research Center in High Performance Computing, Big Data and Quantum Computing, created and managed by the ICSC Foundation, is one of the five National Centers established by the PNRR National Recovery and Resilience Plan, dedicated to strategic sectors for the development of the country: Simulations, high-performance computing and data analysis, Agritech, Development of gene therapy and drugs with RNA technology, Sustainable mobility, Biodiversity.
- The ICSC Foundation has 51 founding members distributed throughout the national territory, coming from the public and private sectors, from the world of scientific research and industry.

https://www.supercomputing-icsc.it/en/icsc-home/



https://www.supercomputing-icsc.it/en/icsc-home/

SPOKE 10 - Quantum Computing

- **WP1. Software. Development and application of high-level quantum software for algorithms solving general purpose problems, scientific and industrial applications.**
- **WP2. Mapping, compilation and quantum computing emulation. Development of software toolchain for compilation, benchmarking, verification, emulation of quantum computers and algorithms.**
- **WP3. Firmware and hardware platforms. Development of low-level software for the physical operation of quantum computers. Development and support of the quantum computer hardware chain.**
  - T3.1 Photonic hardware
  - T3.2 Superconducting circuits
  - T3.3 Atomic hardware
  - T3.4 Models and firmware

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WP3 - Superconducting Circuits

- "Superconducting Circuits" Task: Napoli, INFN, Bicocca, CNR, Catania.
- Main Hardware deliverable at end of Year 3: One platform with 5+ qubits (HW)

INFN will:

1. Design single or paired SC qubits
2. Characterize at low temperature various SC components
3. Realize a low-temperature set-up with broadband superconducting parametric amplifiers for the dispersive and multiplexed reading of multiple SC qubits.
4. Characterization of circuits with one or more coupled qubits.
5. Measure the coherence times of qubits in a radio-pure environment.
6. Write the firmware code for boards with Altera and Xilinx FPGAs necessary for sending pulse sequences, executing commands and checking the result.
7. Develop drivers and communication protocols for the interface between QIBO and FPGA.
8. Use of broadband RF DACs to directly synthesize control pulses.

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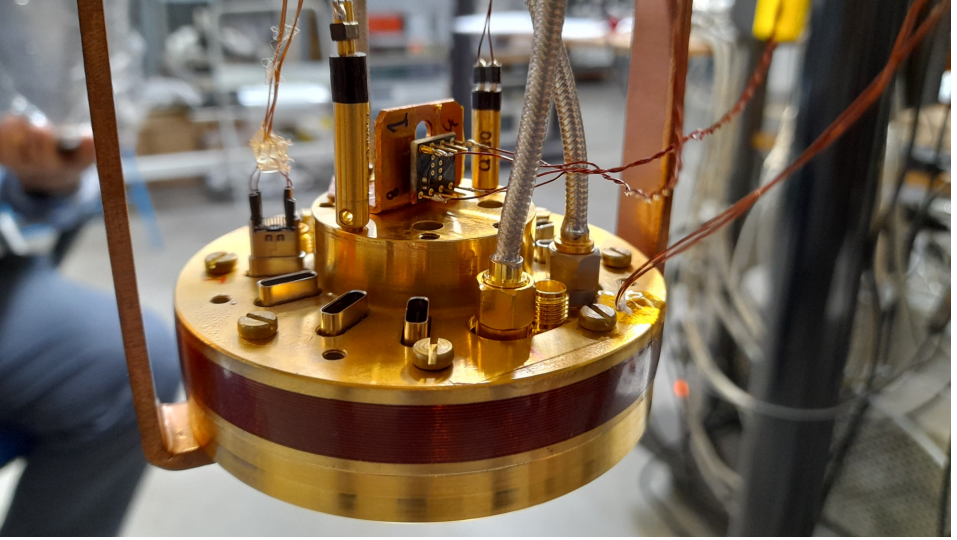
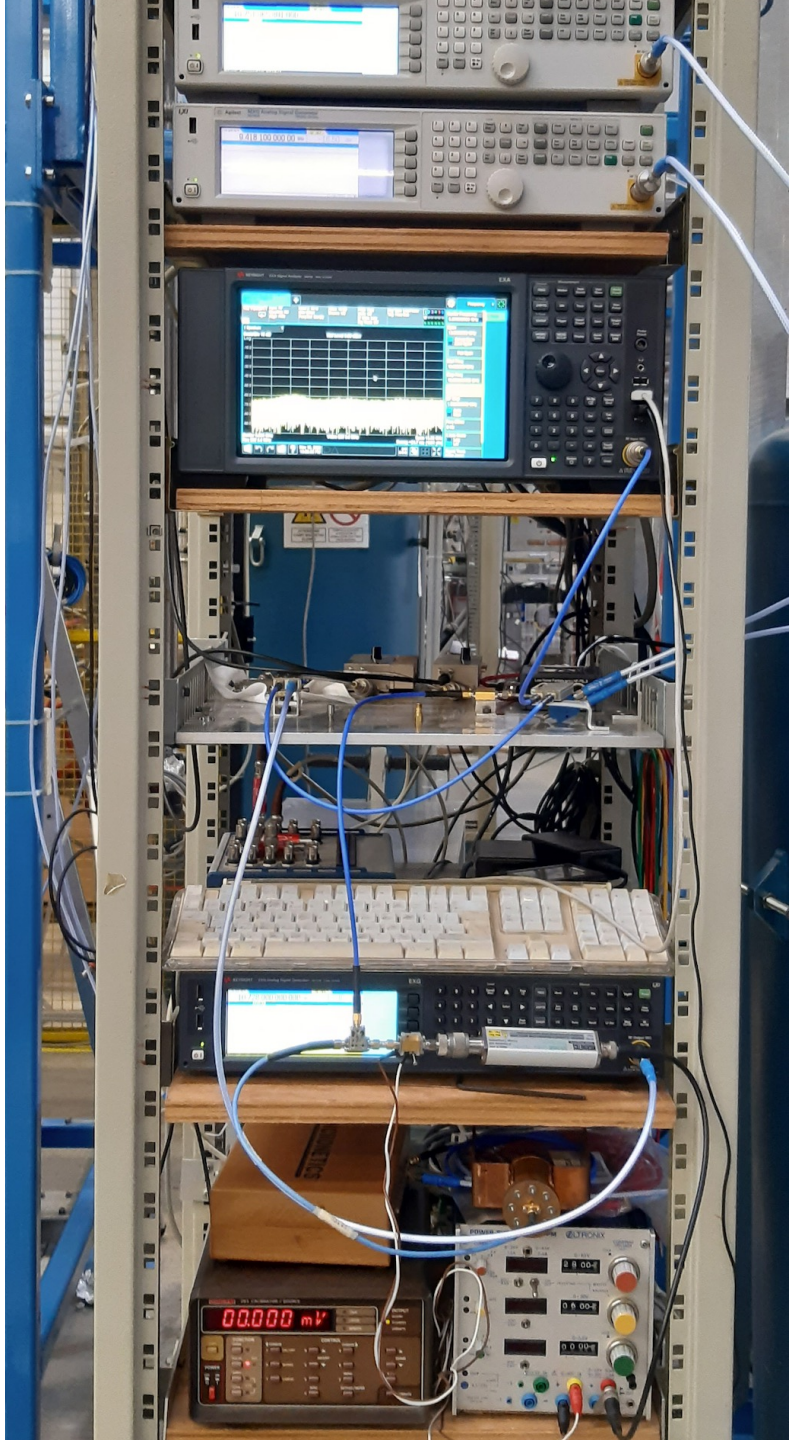




5 INFN laboratories instrumented with dilution refrigerators and RF electronics

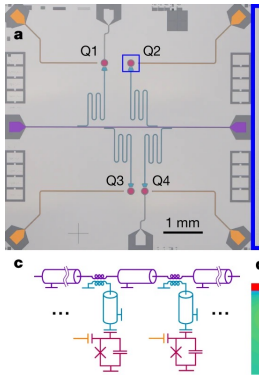
- LNF
- LNL
- LNGS
- INFN Roma
- INFN Pisa

In collaboration with MIB

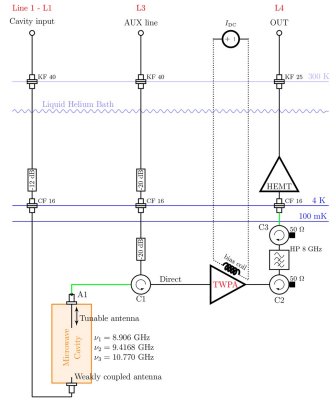
INFN Background in SC Circuits

Many experiments and projects in which INFN participates contribute to its background in superconducting circuits:

- Test of qubits in radiopure environment (DEMETRA/SQMS see talks by L. Cardani and A. Cruciani)
- Tests of TWPAs (QUAX and Dart Wars see talk by M. Faverzani)
- Realization and test of SC circuits with qubits (Qub-IT, Supergalax)



SQMS



DART WARS

SUPERGALAX

Qub-IT

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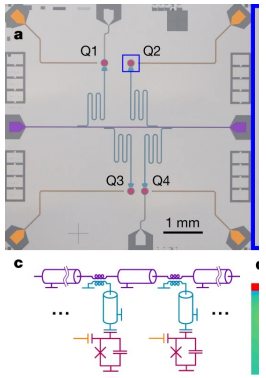
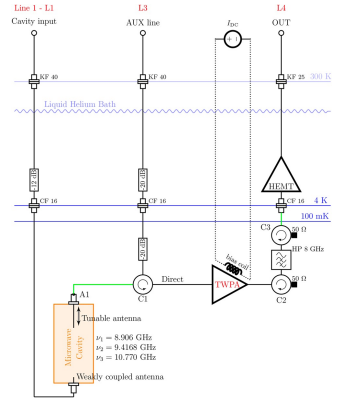
I'll focus on this activity to complement previous talks



SQMS

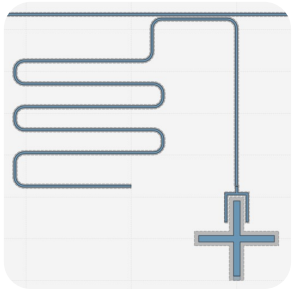


DART WARS

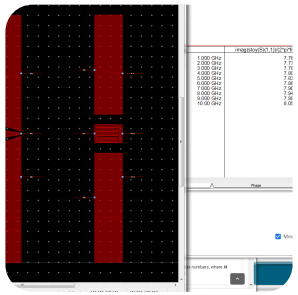
SUPERGALAX

Qub-IT

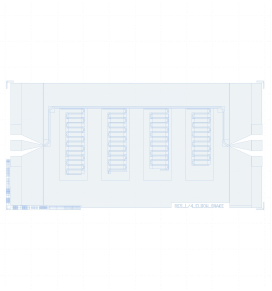
- Chip Design



Qubit circuit design and simulation

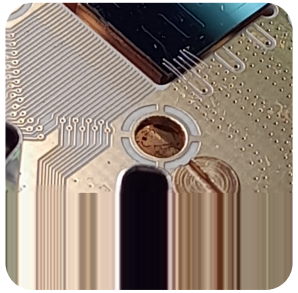


E.M. simulation



Design of circuits layout

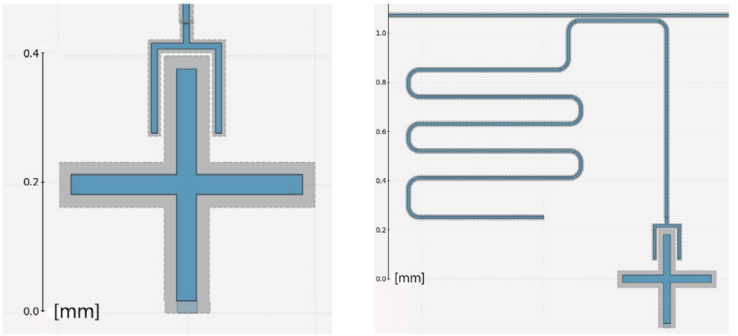
Chip realization



Measurement

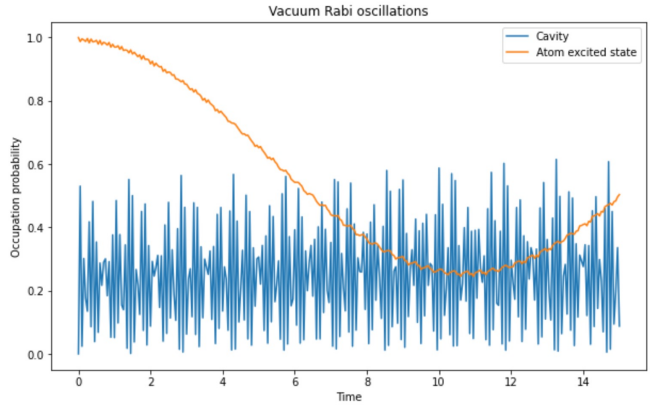
Qubit Design

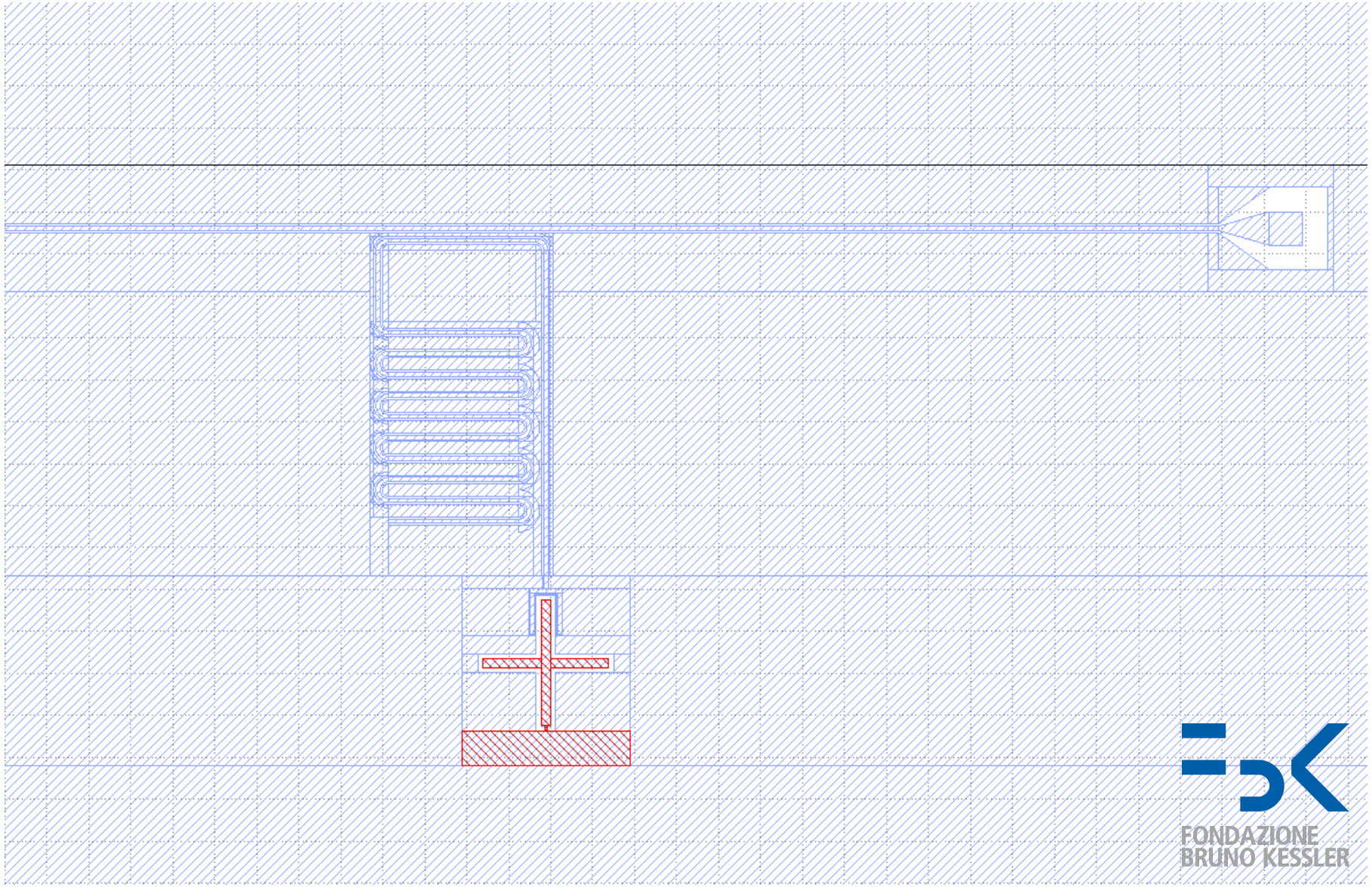
- Focus on transmon qubit of Xmon type
- Preliminary design with analytical calculations
- Circuit design with Kiskit Metal
- Simulation with Ansys Q3D to extract circuit capacitances
- Ansys HFSS and pyEPR analysis to extract qubit and resonator frequencies, anharmonicities and dispersive shifts.
- Qutip for evolution of the quantum system (Rabi oscillation)
- Good agreement between simulation results and analytical calculations



(a) (b)

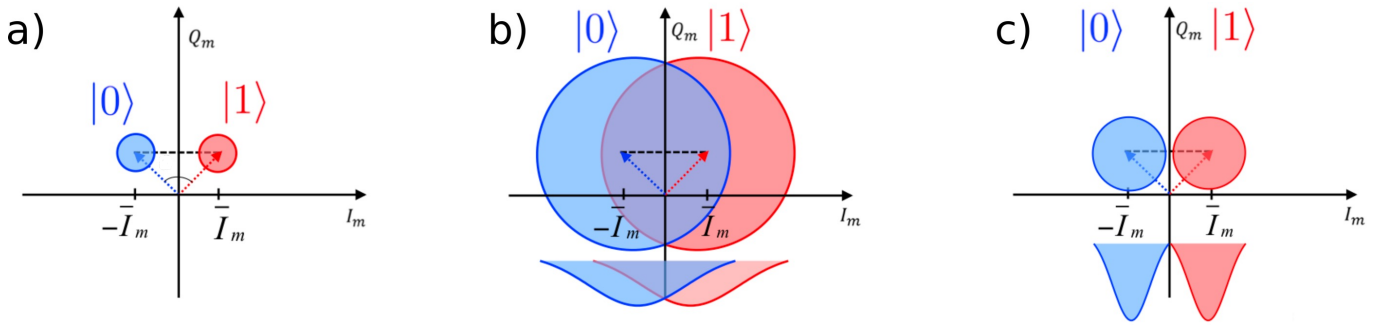
D. Labranca et al. https://doi.org/10.1016/j.nima.2022.167716





FONDAZIONE
BRUNO KESSLER

- Amplification



TWPA

IEEE TRANSACTIONS ON
APPLIED SUPERCONDUCTIVITY

A PUBLICATION OF THE IEEE COUNCIL ON SUPERCONDUCTIVITY

JANUARY 2023 VOLUME 33 NUMBER 1 ITASE9 (ISSN 1051-8223)

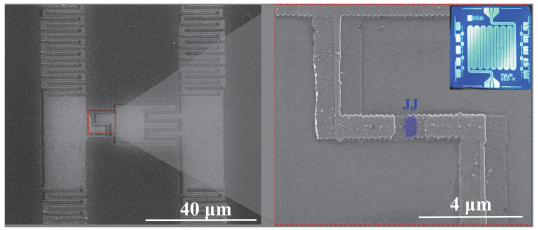


Fig. 1 from "Characterization of Traveling-Wave Josephson Parametric Amplifiers at T = 0.3 K," by Granata et al., 0500107.

IEEE

V. Granata et al. (DART WARS), IEEE Trans. Appl. Supercond. Volume 33, Issue: 1, 0500107, 2022

See talk M.Faverzani

Review of Scientific Instruments ARTICLE scitation.org/journal/rsi

A haloscope amplification chain based on a traveling wave parametric amplifier

Cite as: Rev. Sci. Instrum. 93, 094701 (2022); doi: 10.1063/5.0098039
Submitted: 4 May 2022 • Accepted: 28 July 2022 •
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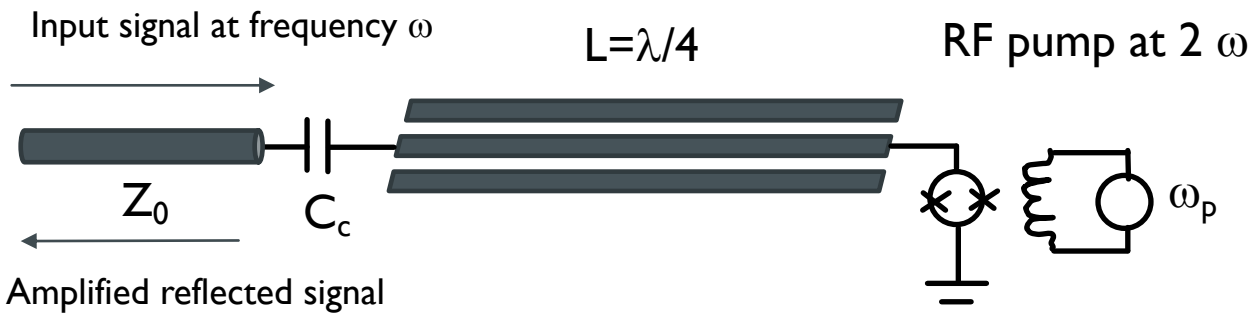
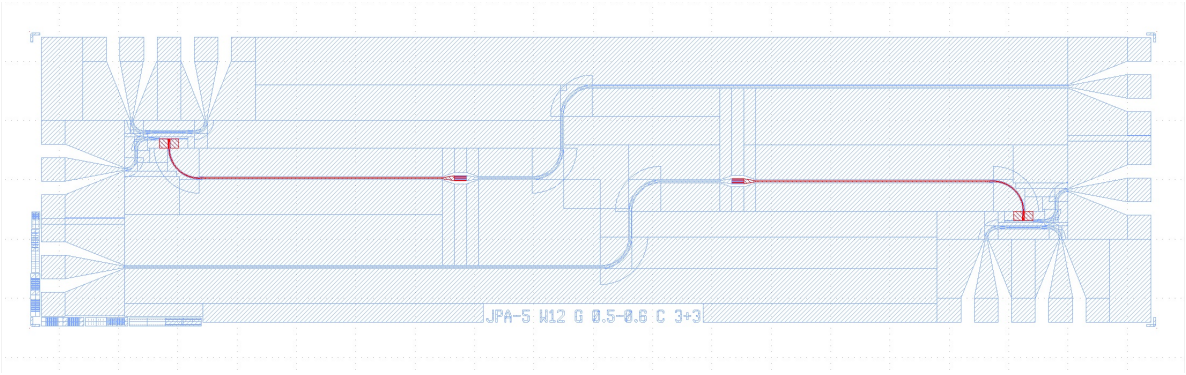
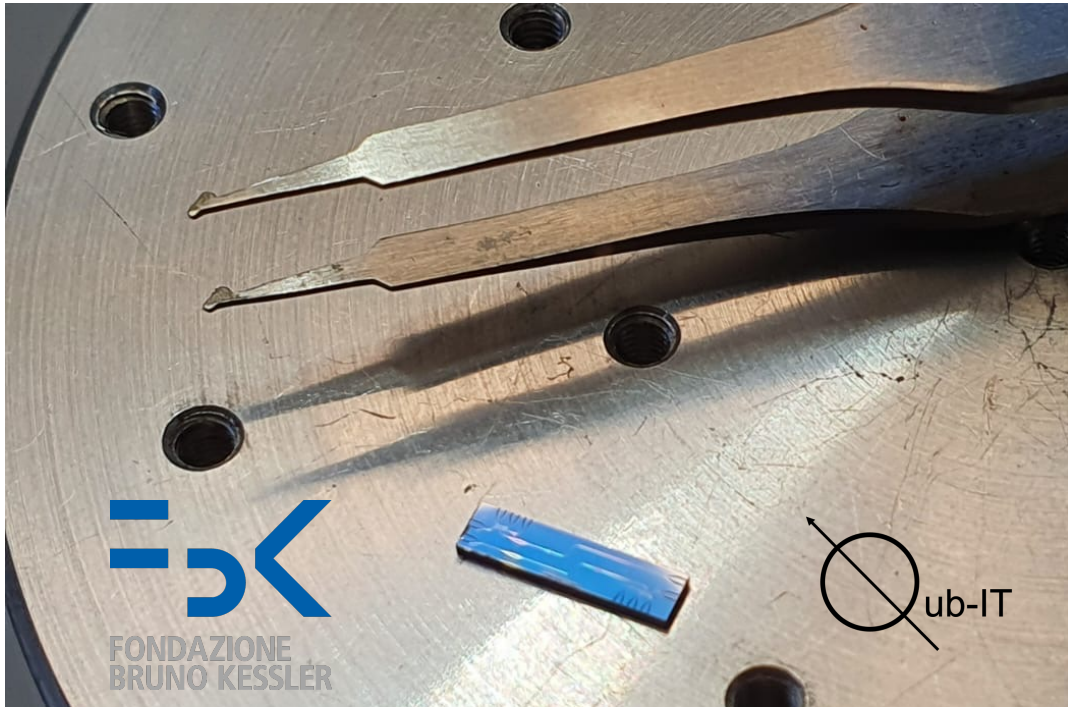
Caterina Braggio,[1,2] Giulio Cappelli,[3] Giovanni Carugno,[2] Nicolò Crescini,[3] Raffaele Di Vora,[2,4] Martina Esposito,[3,5] Antonello Ortolan,[6] Luca Planat,[3] Arpit Ranadive,[3] Nicolas Roch,[3] and Giuseppe Ruoso[6,a)]

C. Braggio et al. https://doi.org/10.1063/5.0098039

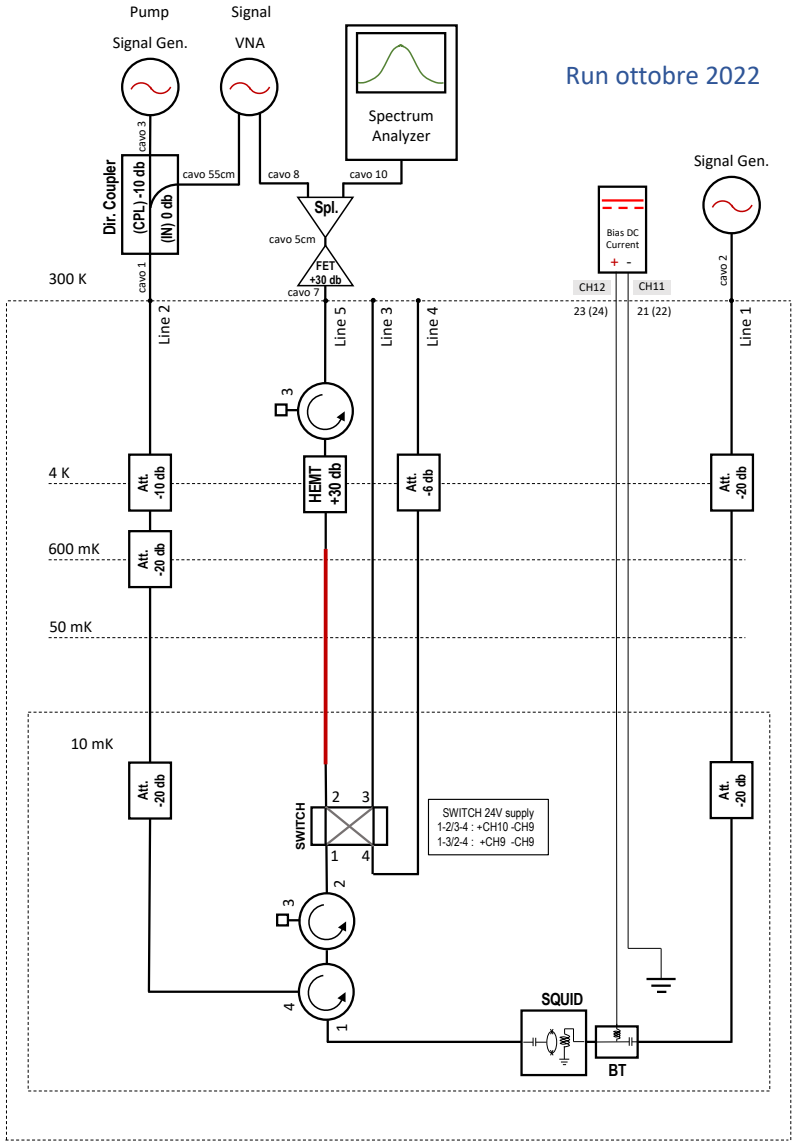
Flux JPA

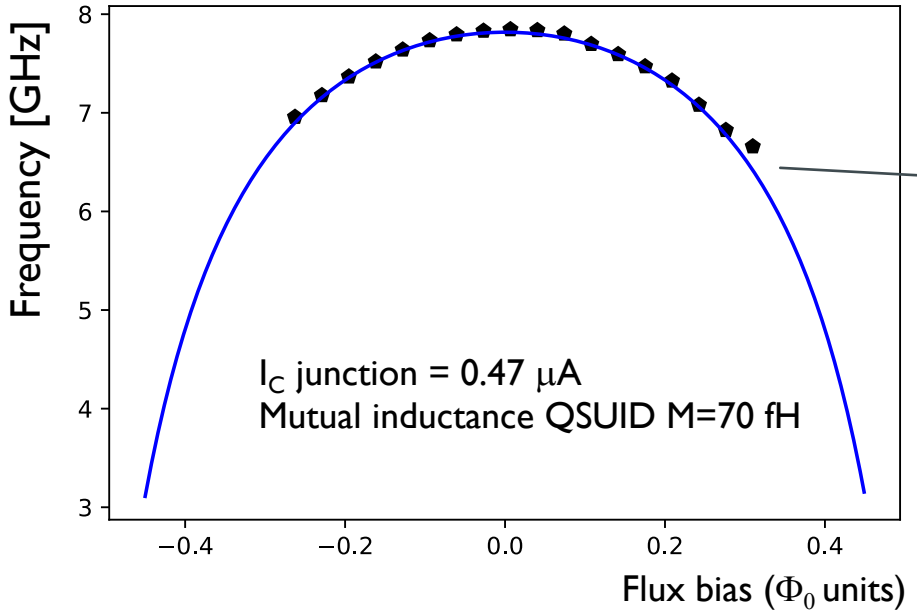


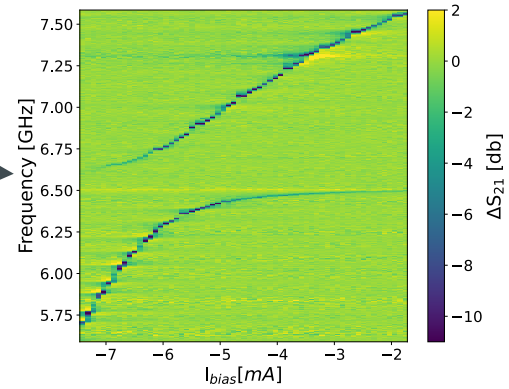




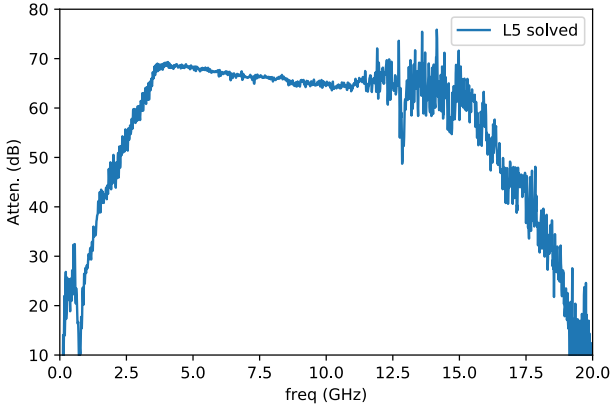
Chip realized at FBK with submicrometric optical lithography and Al shadow evaporation technique.







Hybridization with spurious mode



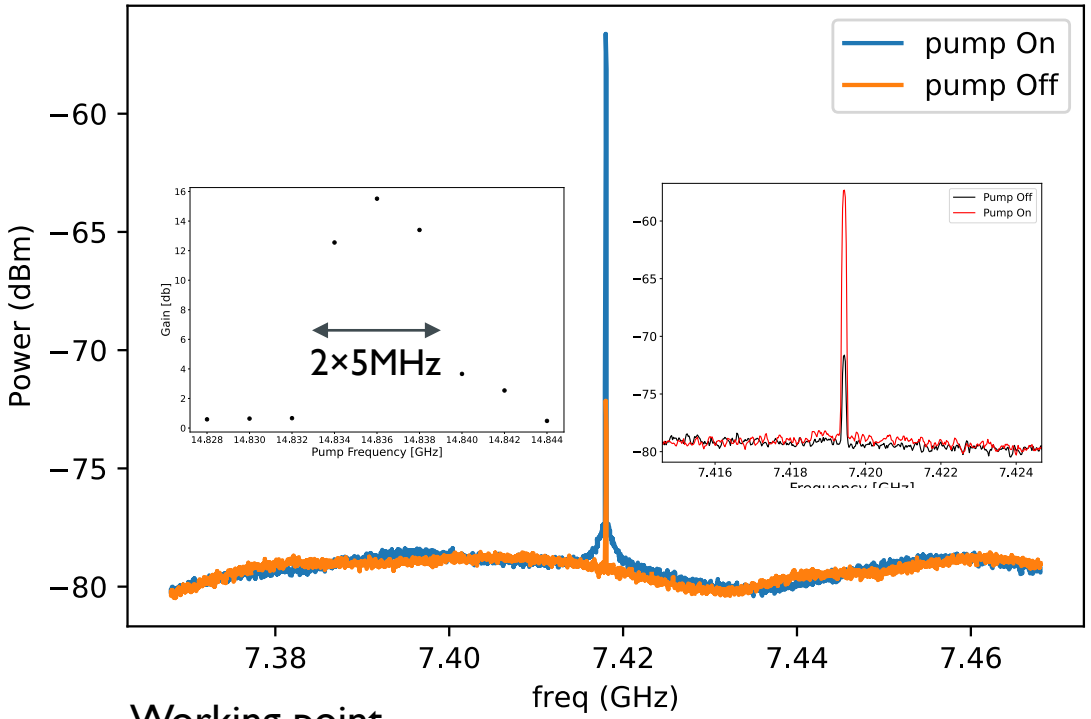
HEMT line gain calibration:

$$Gain = (64.5 \pm 2.0)\ \text{dB}$$

$$T_n^{HEMT} = \frac{P_n}{k_B\ \Delta\nu\ G5} = (3.3\ \pm^{1.9}_{1.2})\ K$$

~3K from Low Noise Factory datasheet

Degenerate JPA Gain and Noise



Working point

f_{signal}=7.418 GHz

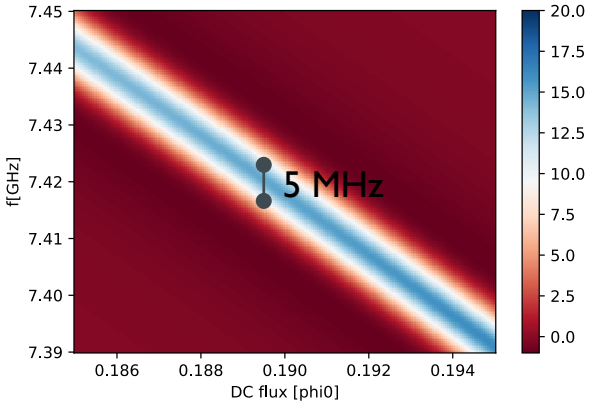
$f_{pump}=2f_{signal}$

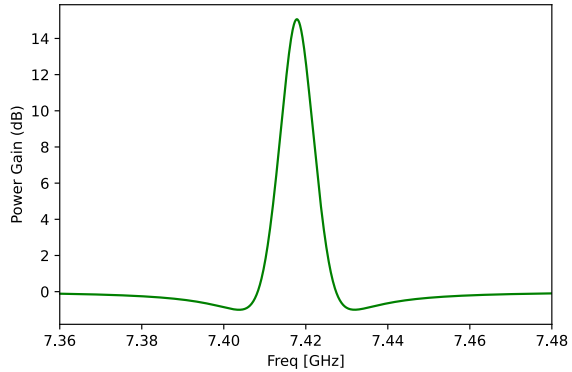
P_{signal}= -135 dbm

P_{pump}= -45 dbm

$\Phi=0.19\ \Phi_0$

Theoretical expectation





Measured Gain

$G_{JPA} = 15.5$ dB

Measured Noise

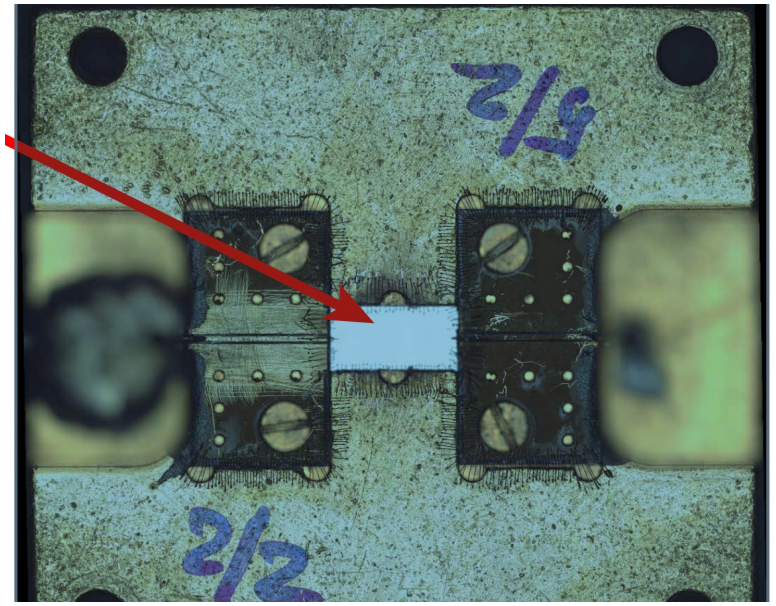
$$T_n^{JPA} = \frac{P_n}{k_B\,\Delta\nu\,(G5 + G_{JPA})} = \left(0.130\ \pm^{0.075}_{0.049}\right) K$$

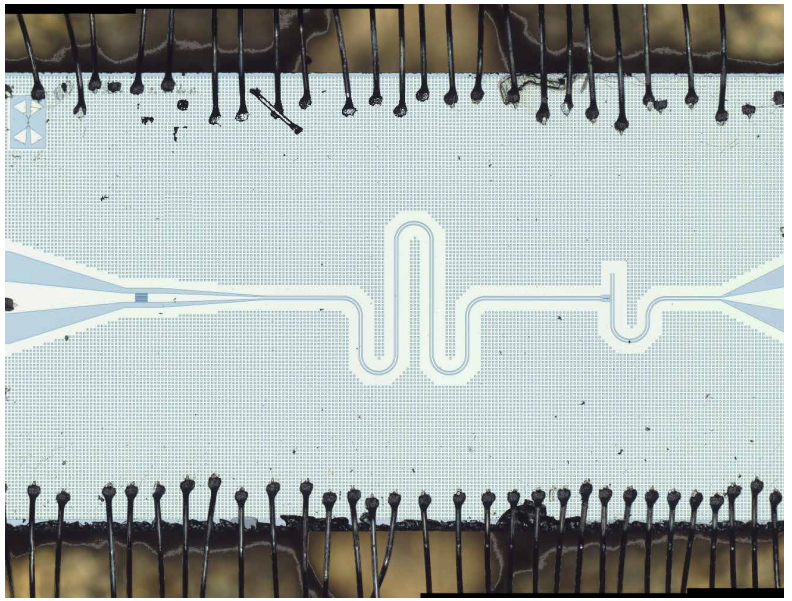
Expected quantum noise ½ hν/k_B T=0.174 K

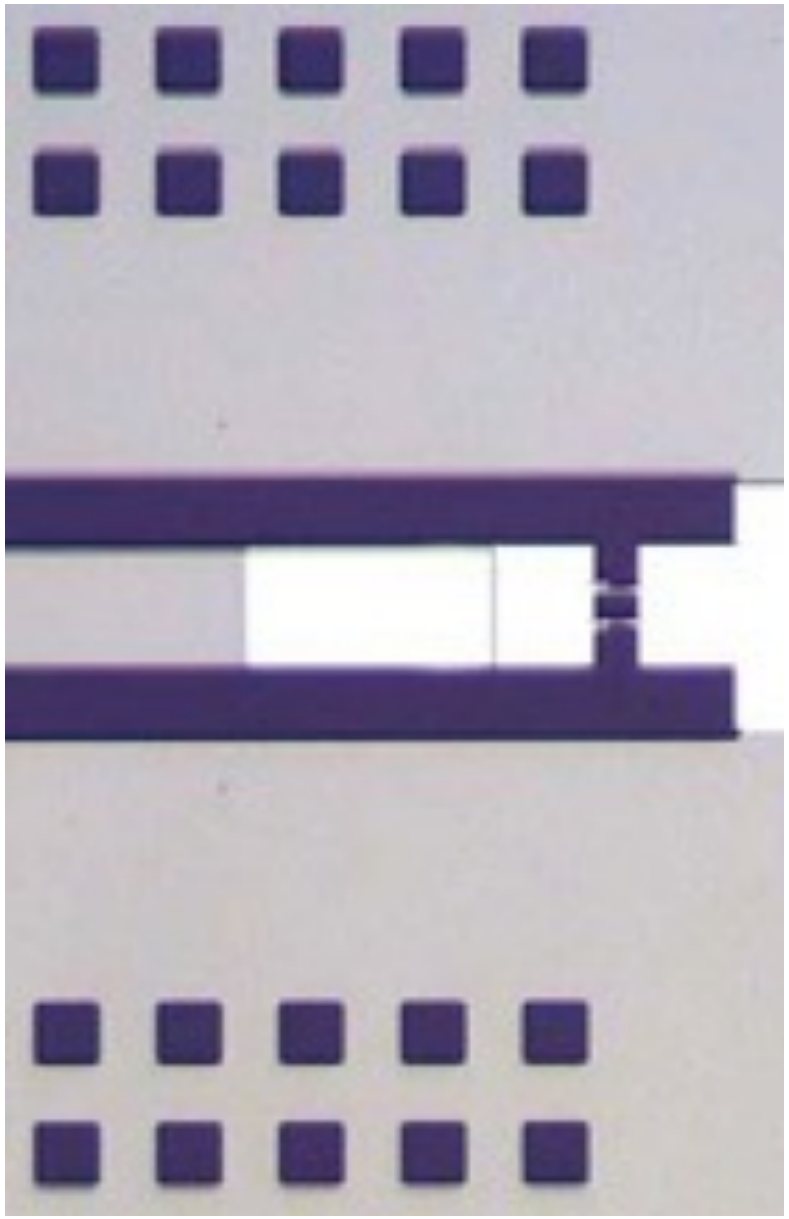
- Details are important!

Fortgeschrittenenpraktikum: The Josephson Parametric Amplifier Philipp Kruger, Kirill G. Fedorov

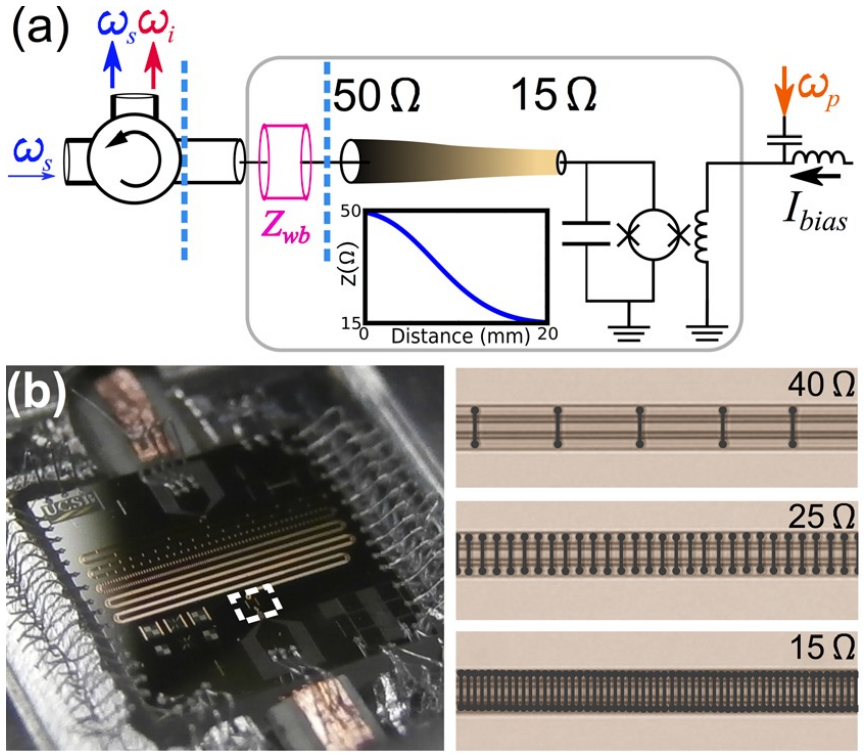
L Zhong et al 2013 New J. Phys. 15 125013







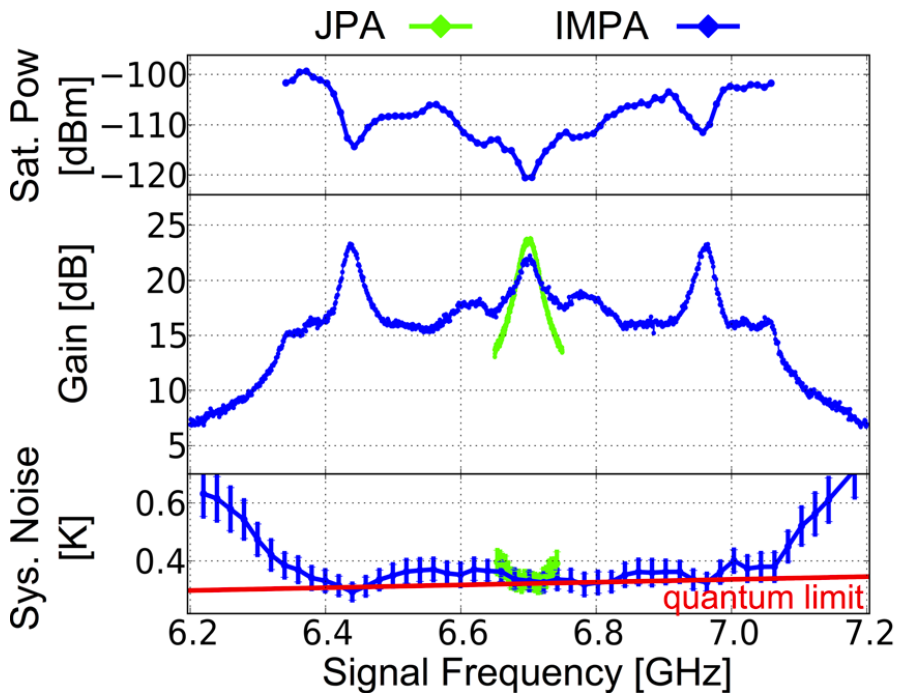
Broadband JPA I: IMPA impedance-transformed parametric amplifier



$$\omega_j = \frac{1}{\sqrt{LC}}$$

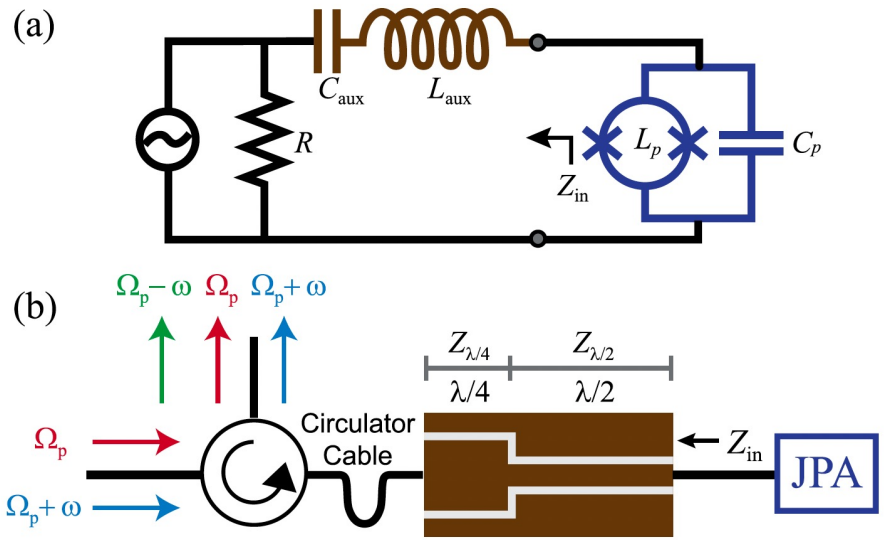
$$\gamma = \frac{1}{Z_0 C} = \frac{\omega_j Z_j}{Z_0}$$

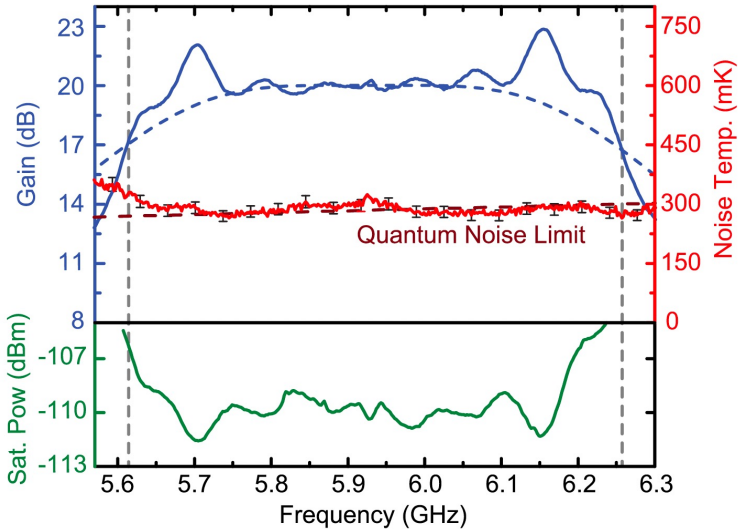
$$Q = \frac{1}{\sqrt{LC}} C Z_0 = \frac{Z_0}{Z_j}$$



Appl. Phys. Lett. 104, 263513 (2014)

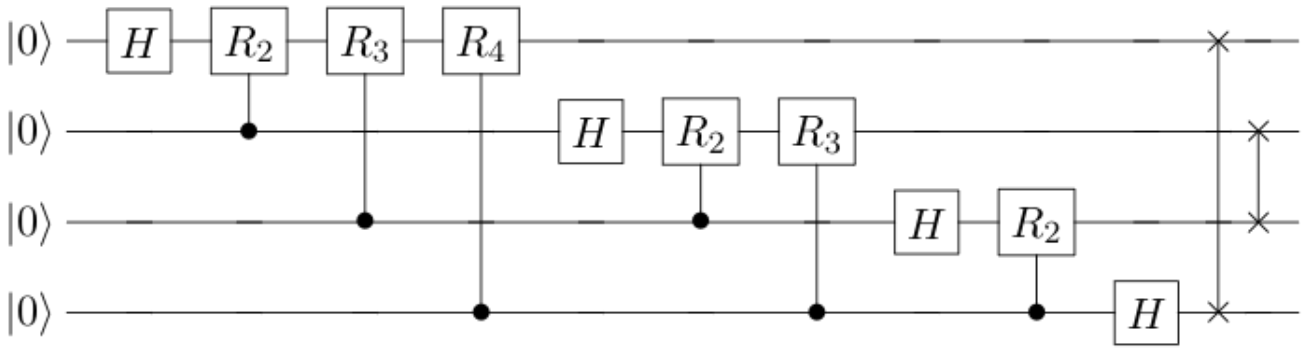
Broadband JPA II: Impedance Transformers

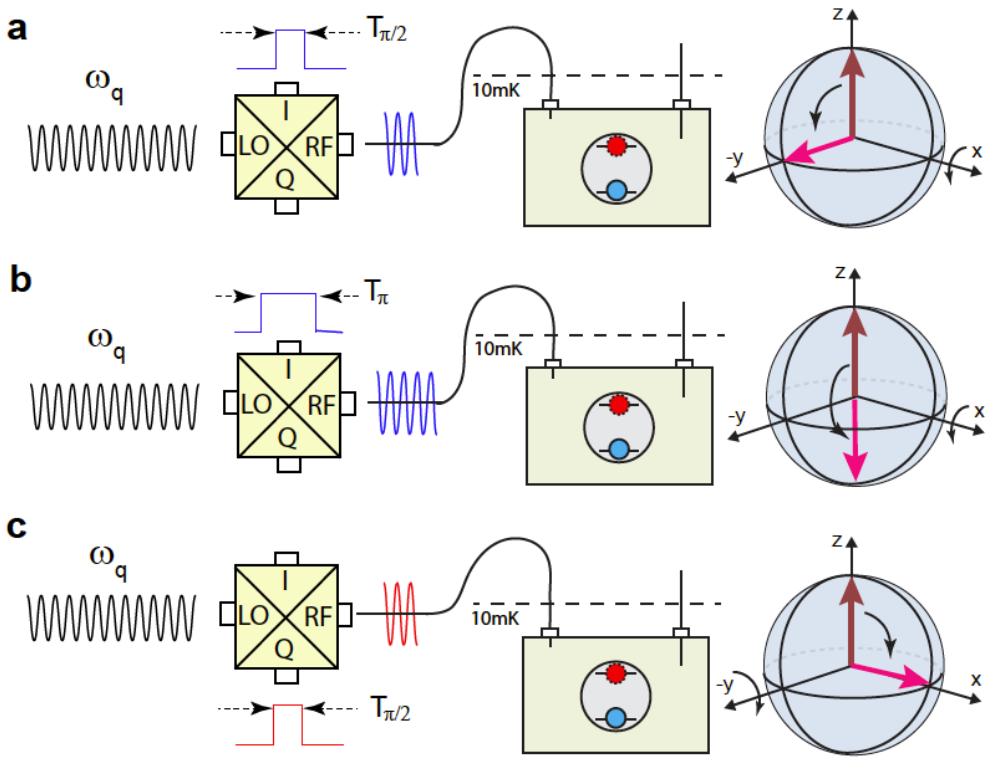


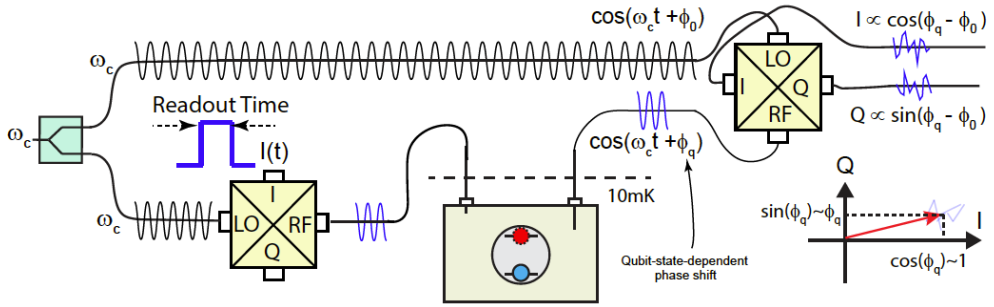


Appl. Phys. Lett. 107, 262601 (2015)

- Qubit Control

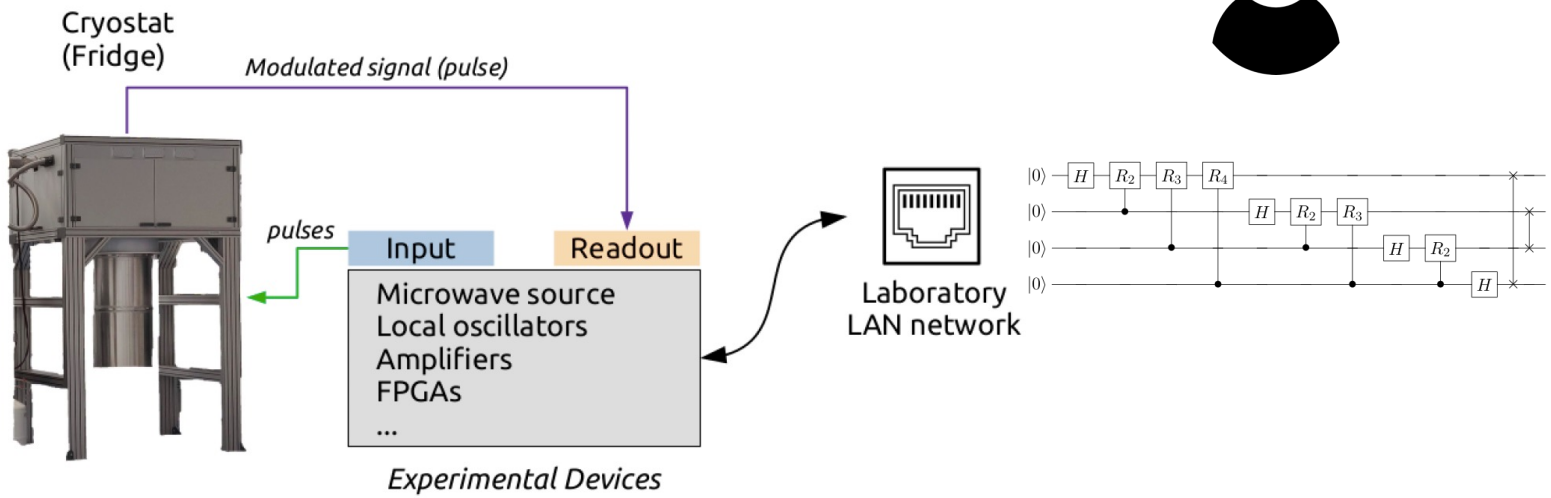






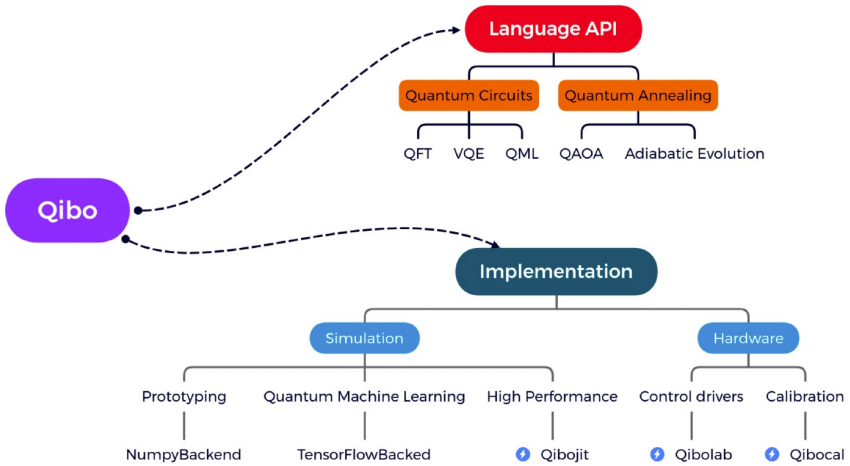
arXiv:1904.09291

Qubit Control



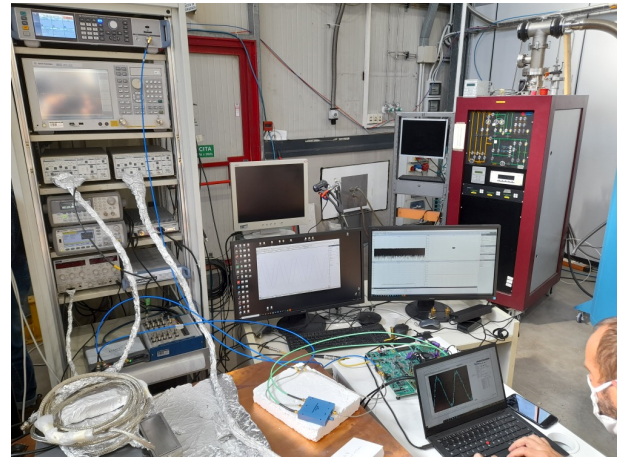
1) QIBO software for hardware control

https://github.com/qiboteam/qibo



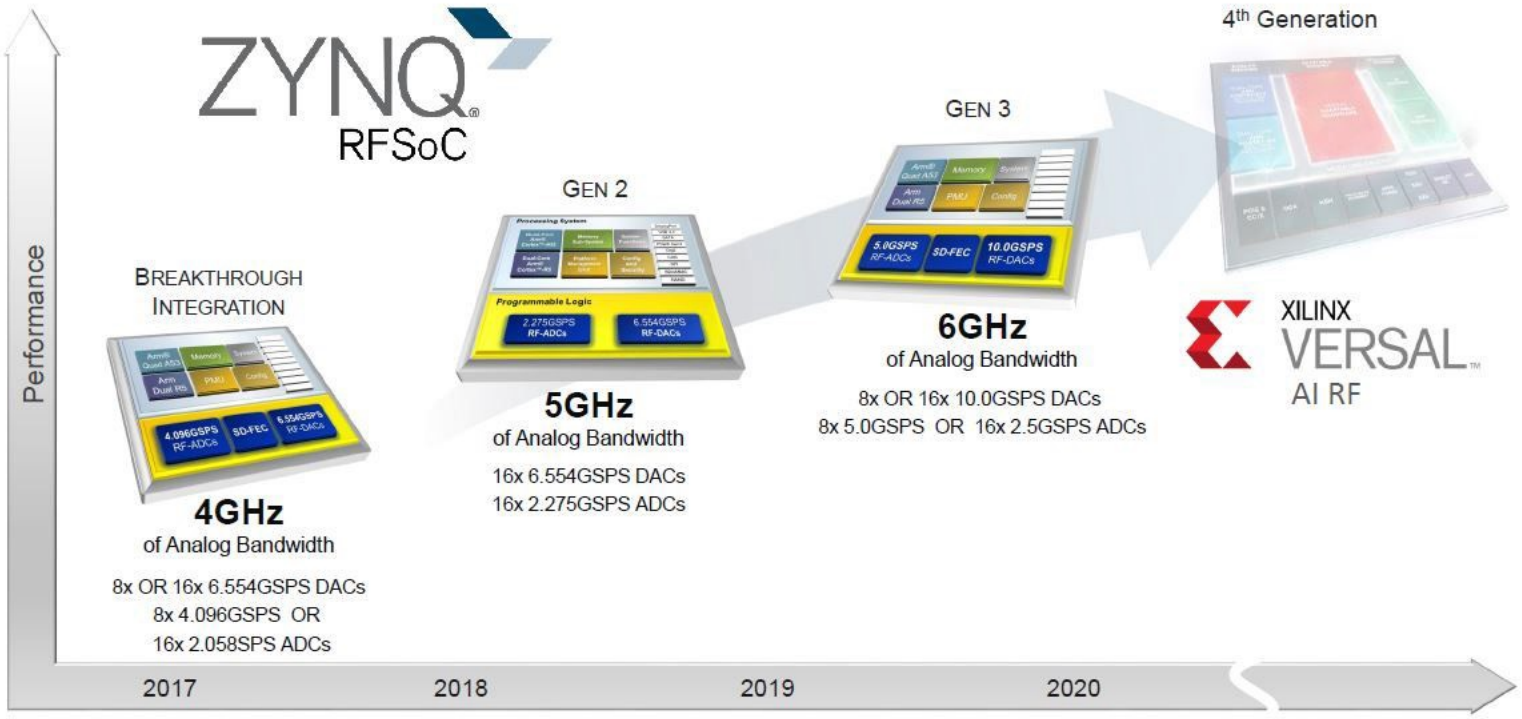
2) FPGA for direct microwave synthesis of qubit control pulses

arXiv:2203.01523
Digital Object Identifier 10.1109/TQE.2020.3042895



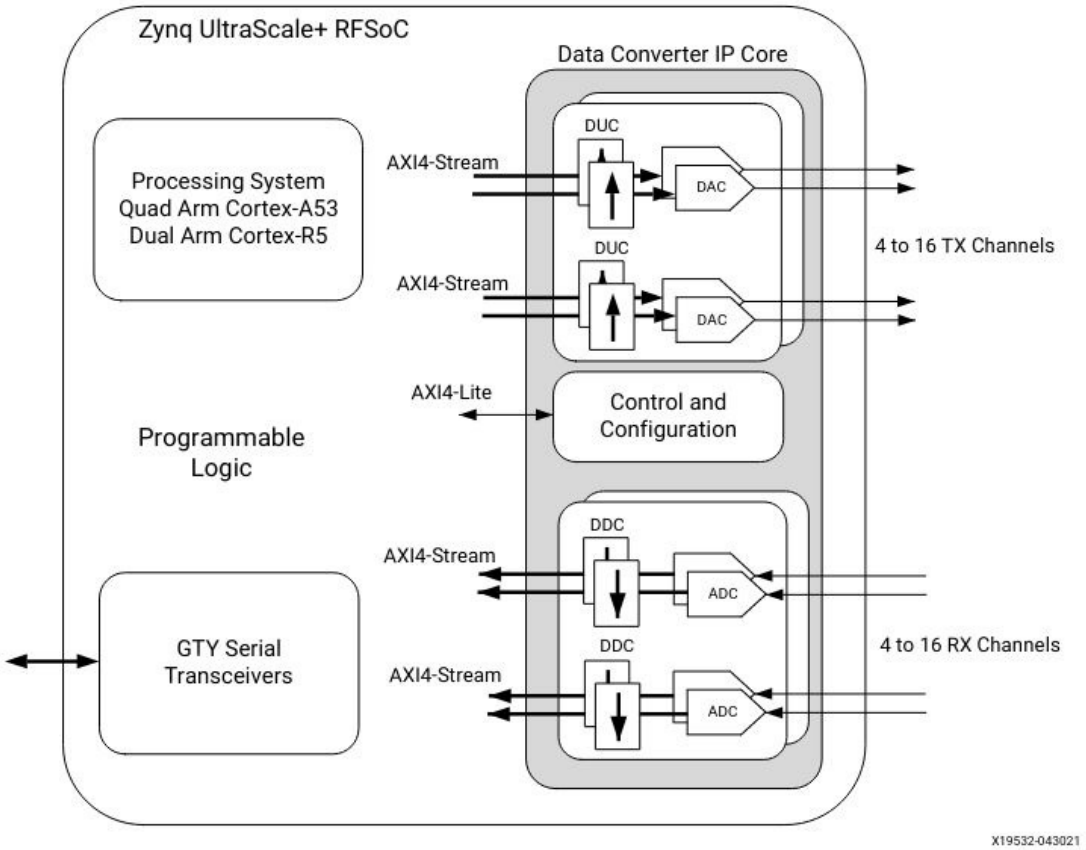
Xilinx RFSoCs

Roadmap to Meet Current and Future Market Needs

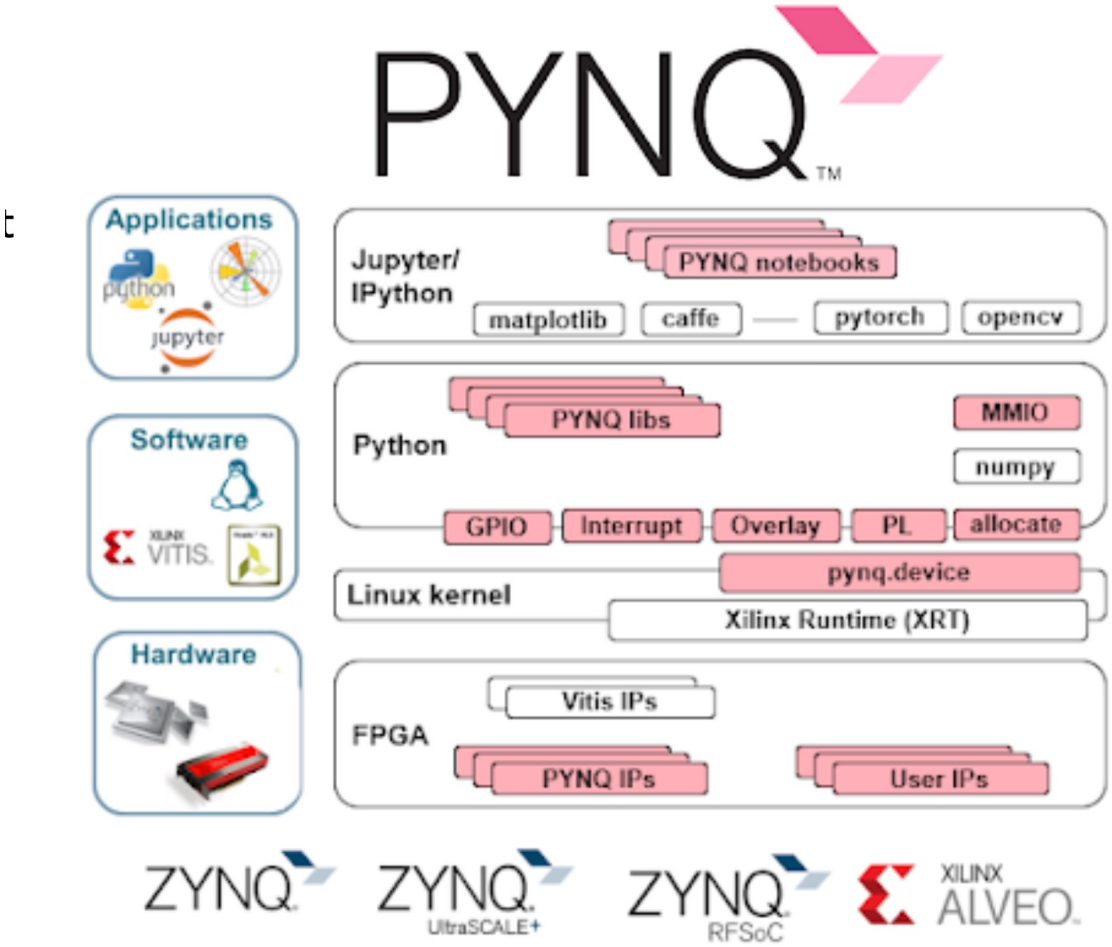


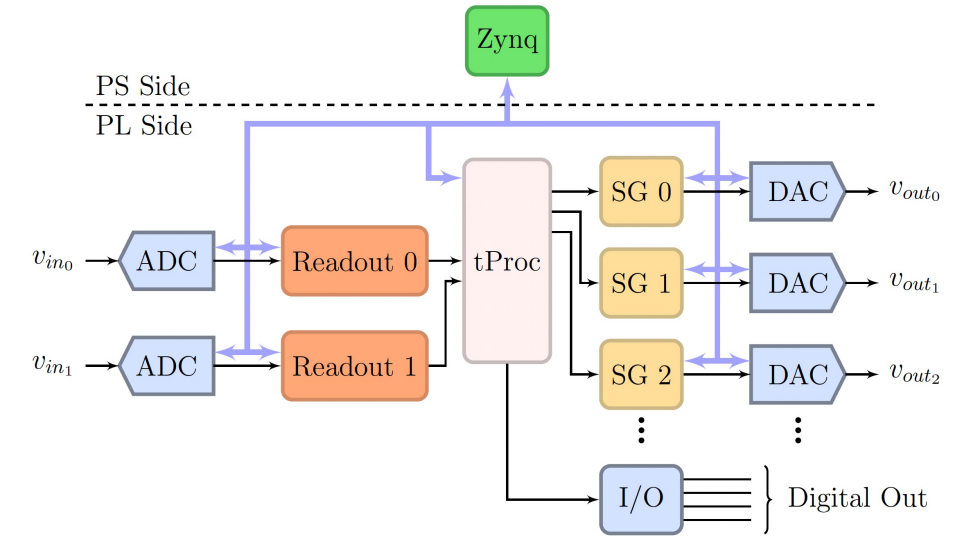
RFSoC Diagram

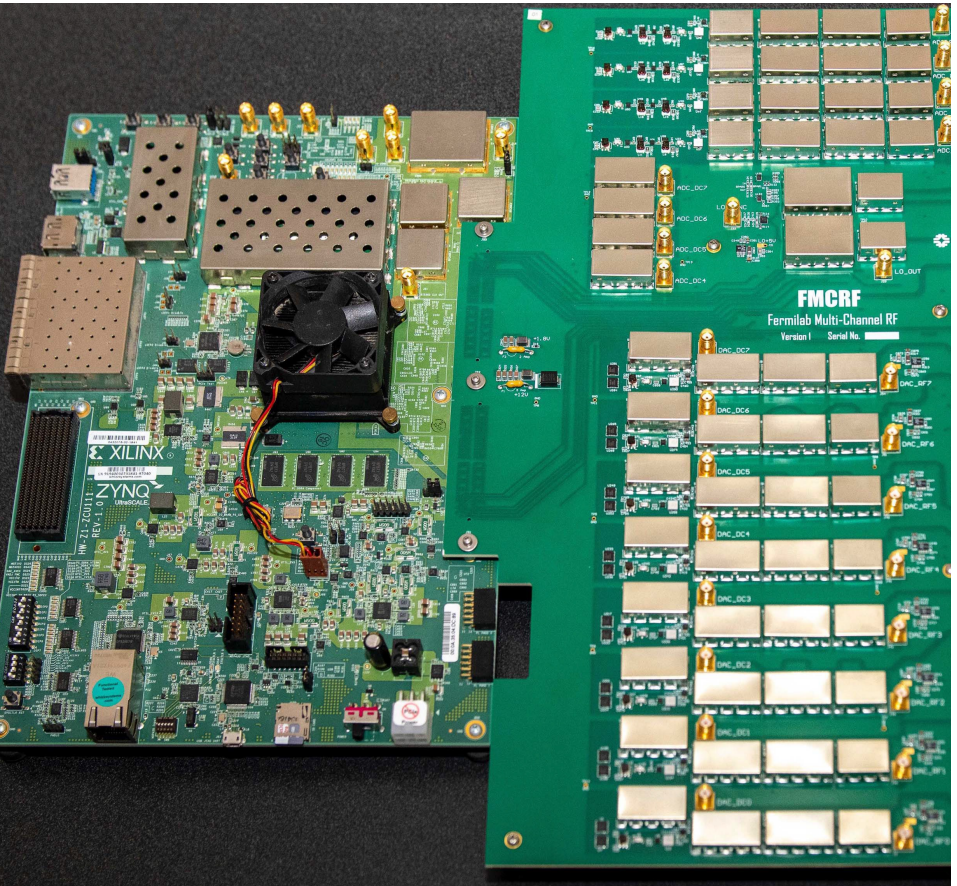
Figure 1: **Zynq UltraScale+ RFSoC RF Data Converter IP Core in Zynq UltraScale+ RFSoC (Gen 1/Gen 2/Gen 3)**



- PYNQ is an open-source project from Xilinx that makes it easier to use Xilinx platforms.
- Using the Python language and libraries, designers can exploit the benefits of programmable logic and microprocessors to build electronic systems.
- A PYNQ enabled board can be easily programmed in Jupyter Notebook using Python.
- http://www.pynq.io





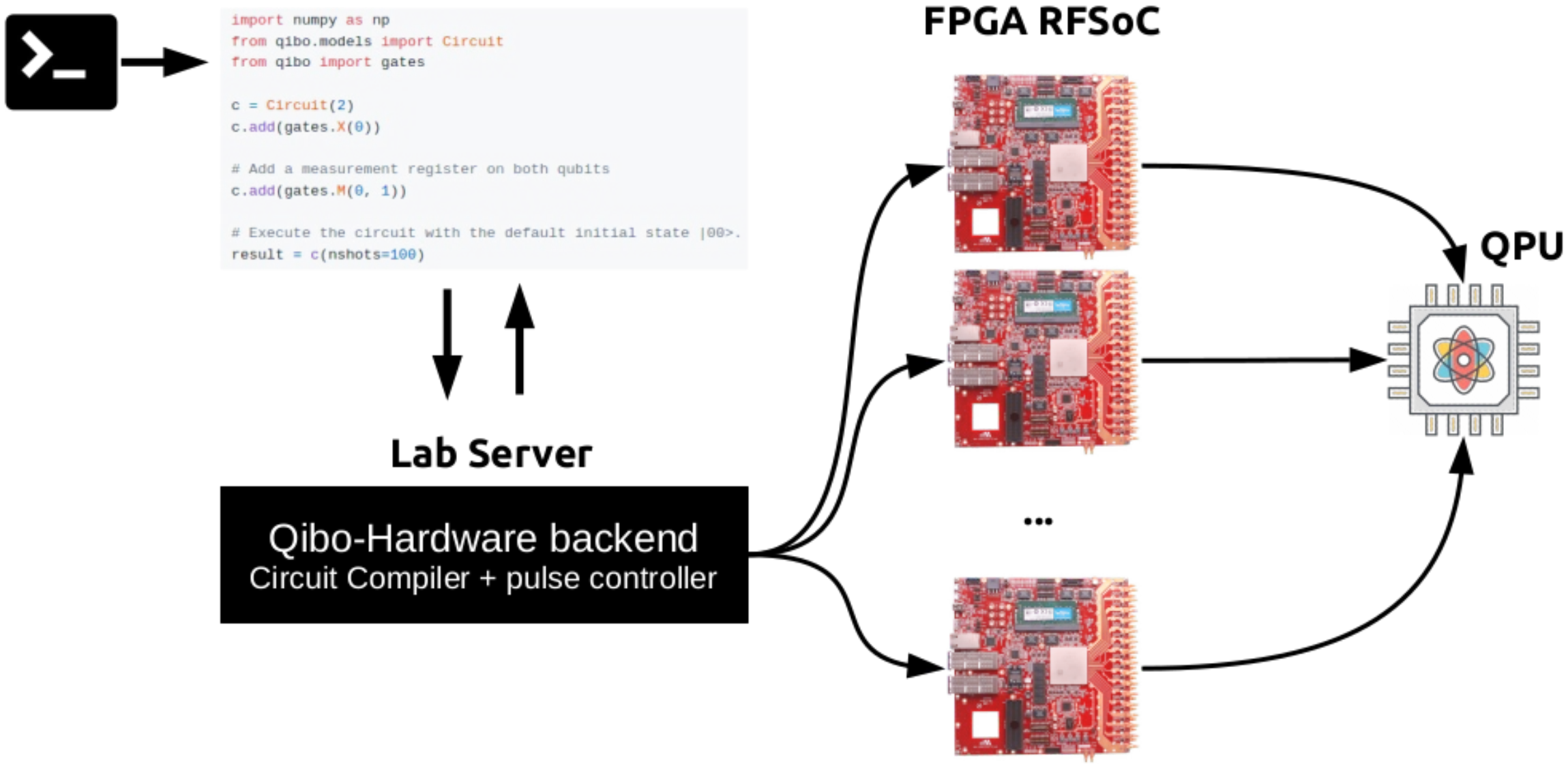


The QICK (Quantum Instrumentation Control Kit):

Readout and control for qubits and detectors

1. The Quantum Instrumentation Control Kit (QICK) is an open-source RFSOC-based platform which combines FPGA firmware for real-time processing and a Python interface running the PYNQ operating system. The initial implementation of the QICK uses the ZCU111 evaluation board with eight DACs and ADCs. Now available for ZCU216. Testing it now on ZCU208 at LNF.
2. The functionality of the QICK system is divided between the Processing System (PS) and Programmable Logic (PL).
3. The PS uses PYNQ libraries and drivers to enable direct memory access to the PL.
4. The user interface is typically via Jupyter notebooks accessed from a remote web browser.
5. Firmware in the PL includes signal generator blocks and readout blocks controlled by a timed-processor (tProcessor) block to implement time-critical functions.
6. The core of the QICK system is the tProcessor. This block implements a custom processor, with the addition of timed instructions to ensure events are executed at proper times.

arXiv:2110.00557


import numpy as np
from qibo.models import Circuit
from qibo import gates
c = Circuit(2)
c.add(gates.X(0))
# Add a measurement register on both qubits
c.add(gates.M(0, 1))
# Execute the circuit with the default initial state |00>.
result = c(nshots=100)
Lab Server
Qibo-Hardware backend
Circuit Compiler + pulse controller
FPGA RFSoC
QPU

S. Carrazza

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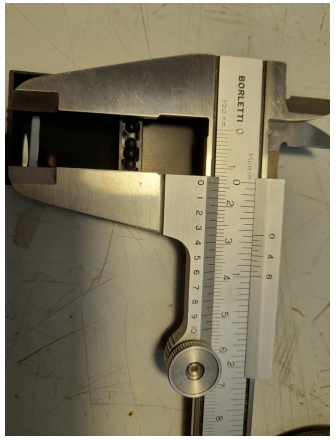
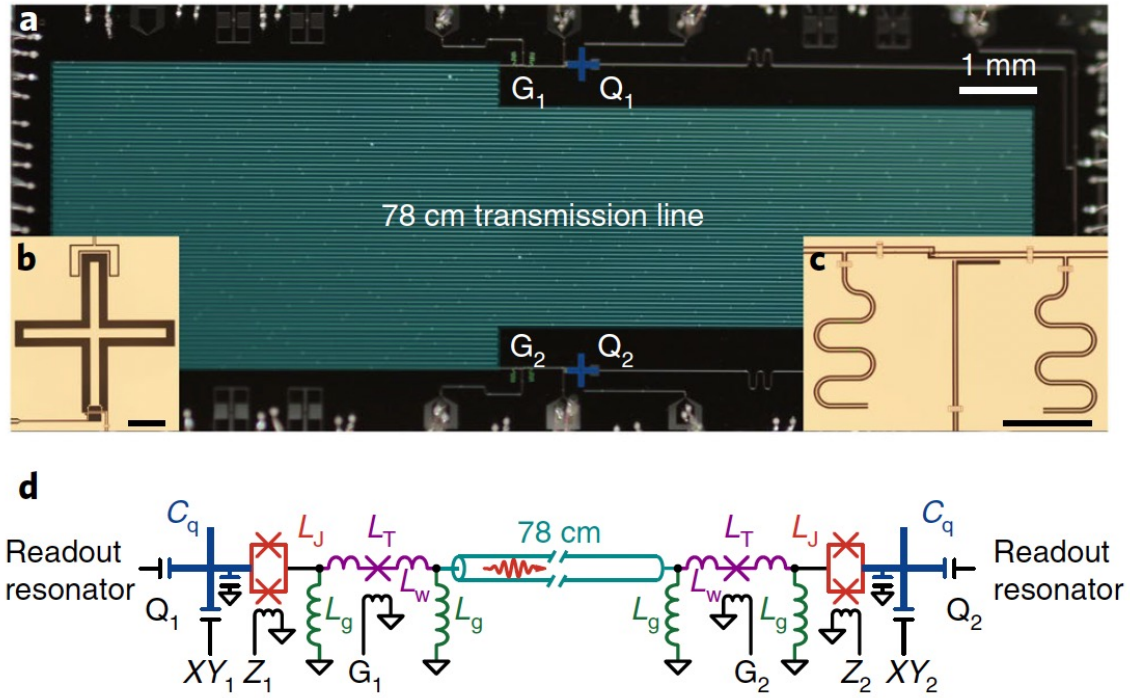


Test with 3D qubit + QIBO + QICK in preparation at LNF

Conclusion

1. The National Centre for HPC is a great opportunity to renew our labs and catch up on the accumulated delay in this field.
2. We will have to harmonize the activities and projects already in progress with those foreseen by the HPC
3. Define the collaboration and activities with our partners, Università di Napoli, CNR-IFN and MiB, contributing to the realization of a prototype quantum processor based on superconducting qubits.
4. Università di Napoli is already running a lab with SC qubits (in collaboration with SEEQC).
5. With MiB and CNR-IFN we will establish the entire development and production chain of key components for a superconducting qubit quantum computer including design, optimization, fabrication and testing with the goal of fabricating a 2 (few) qubits system, and test Bell inequalities …



https://doi.org/10.1038/s41567-019-0507-7