Quick update on DAQ

Note: DAQ WG meeting every Thursday at 2:00 PM (CET)

- inconclusive discussions for many months
- eRD109 project "boundaries" pretty unclear (ASIC or electronics chain?)
- answer: ROB should stay on detector side
- lack of specifications so far, lack of feedback from detectors (and proper managing of from the WG

Two main news:

1. something finally moving...
2. DAQ meeting 9 December

Recent proposals (Tonko Ljubic, BNL)

- RDO model (our "ROB")

RDO Model

- a PCB, specific to every detector in shape/size/form but with expected common features
  - FPGA acting as the SERDES to/from DAQ and control of the ASICs
    - and source of the recovered main EIC clock
    - and some algorithms e.g. zero-suppression or something “simple”
  - PROM for the FPGA configuration (omitted if we use flash-based FPGAs)
  - JTAG connector for PROM programming
  - SFP+ module for electrical-optical interfaces and fiber (1 at least)
    - perhaps some other form factor?
  - clock/jitter cleaner chip (optional for some detectors, e.g. TOF)
  - low jitter clock fanout chips to the ASICs
  - DC/DC converters and/or regulators for LV power to the RDO (e.g. FPGA, etc)
    - but possibly also for the ASICs
  - connection/connector for a number (e.g. N=2-32) of ASICs
    - or none if the ASICs are directly connected to the RDO PCB
  - connector to LV cable (e.g. incoming 10V)
  - ID chip (e.g. I2C or 1wire to uniquely id the board), temperature chip (I2C or 1wire; can be within the ID chip)
  - debugging port (e.g. USB or serial; can be omitted for production versions)
  - LEDs (power, clock received & locked, other activity)
  - jumpers/switches (always put jumpers :-))
  - test pins (lots), some high speed (SMA); don’t need to be populated in production version
- more on RDOs in later slides…

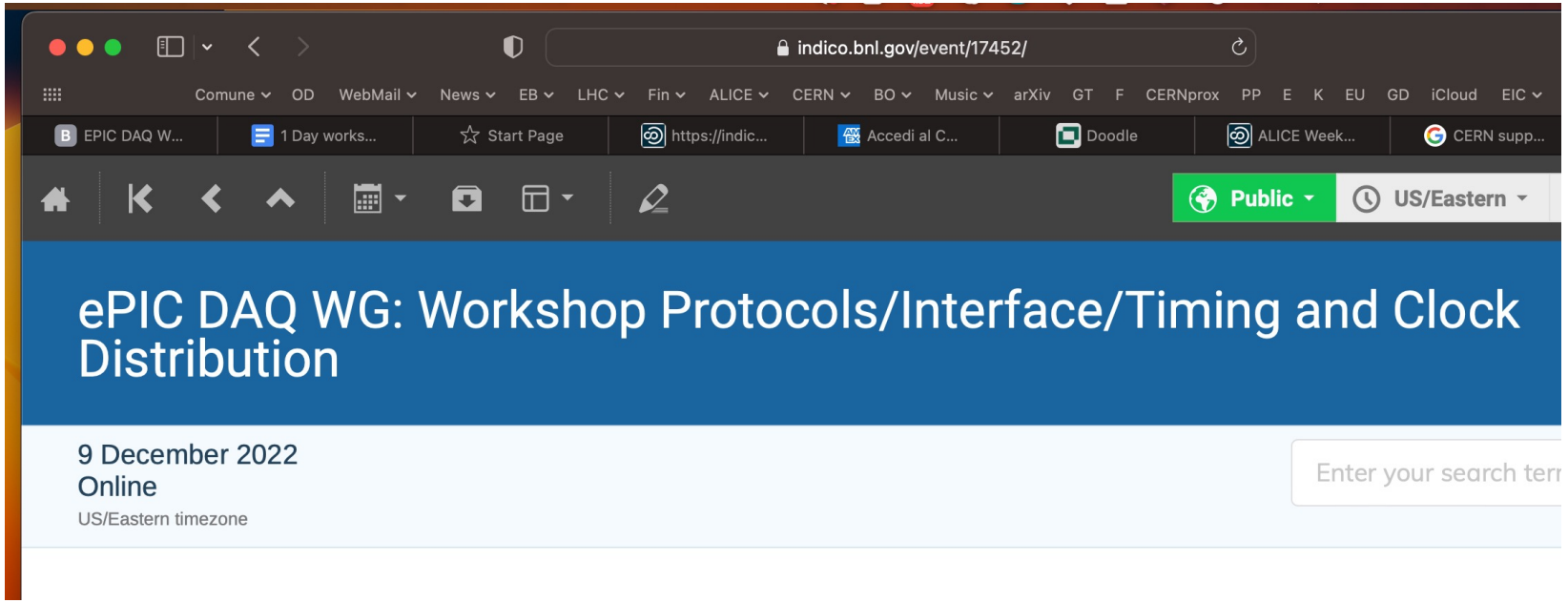
In our current design this
matches our ROB
(reading 16 AlcorV3 64 channels)

Target FPGAs:
- Xilinx Artix Ultrascale+
- Xilinx Kintex Ultrascale+
- Microchip Polarfire

Xilinx ZCU106 as eval board for prototyping in FY23/FY24
RDO boards in FY25

For us it could be very useful to plan FY24 when ALCORv3 available

Plus:
- WG for clock protocol/clock recovery à la lpGBTX
- WG for "DAQ receiver card" (no PHELIX hopefully...)



My takehome

- so far DAQ group quite improductive, finally moving somewhere
- important to remain attached for our ROB design/planning
- be present at 9/XII workshop
- depending on decisions next week we might invest on development kit indicated as target (still to be studied)