UNIVERSITÉ
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T2K

Challenges in read-out electronics for ν physics: the Super-FGD

XX Workshop on Neutrino Telescopes, Venice

26th October 2023

University of Geneva
Department of nuclear and particle physics

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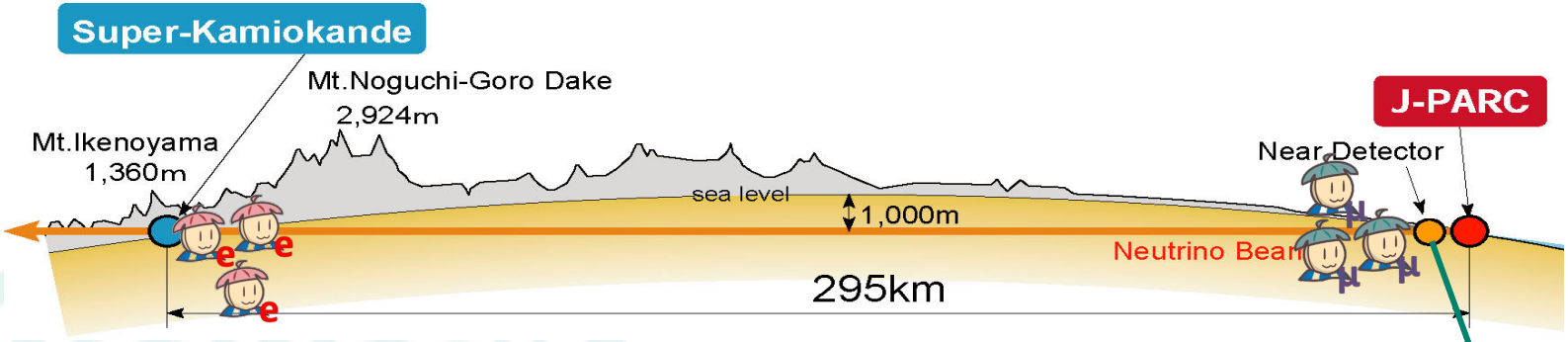
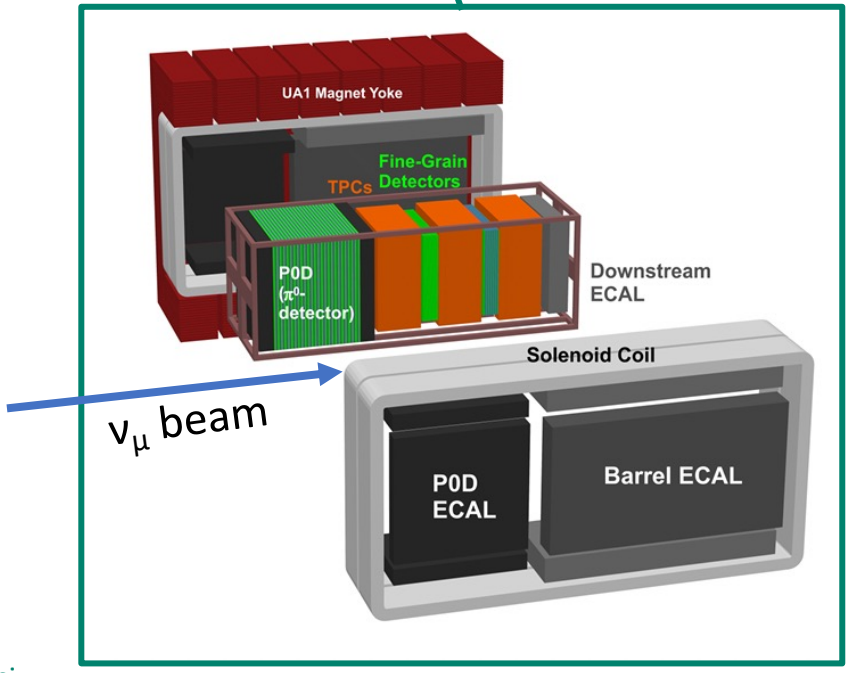
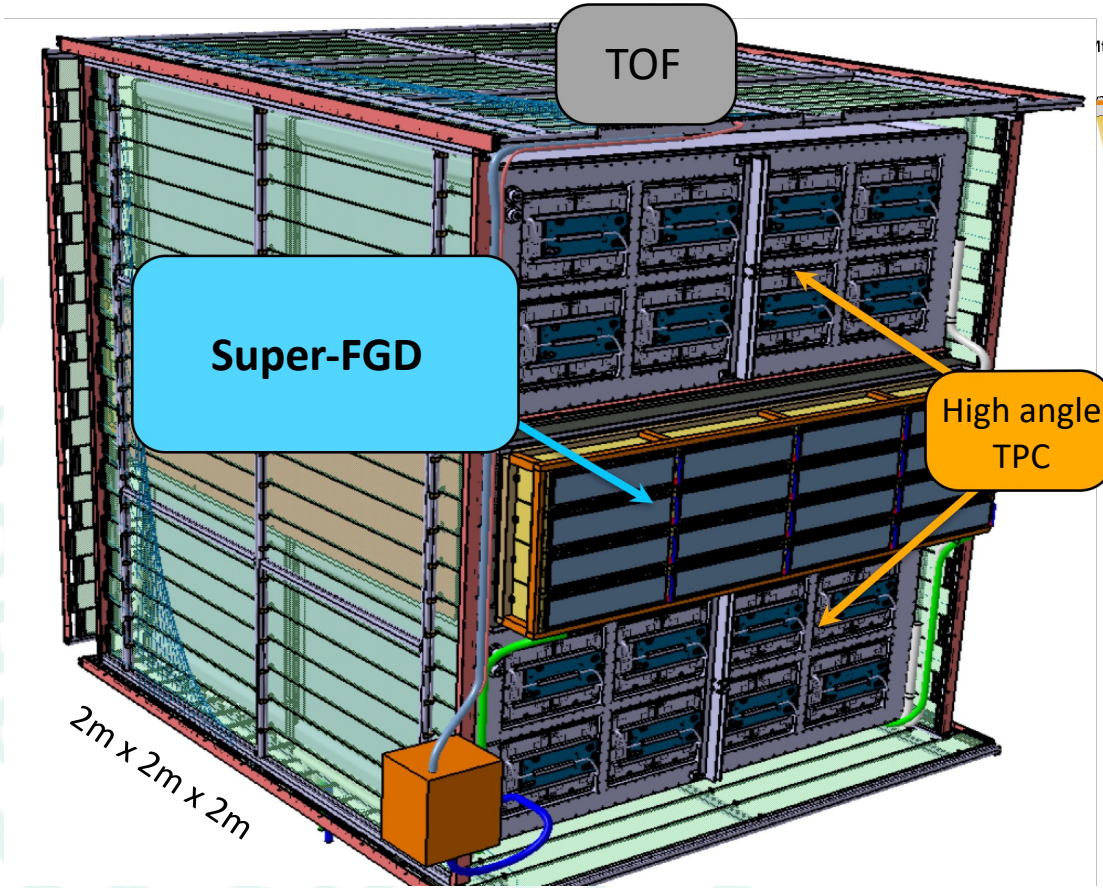
The T2K experiment

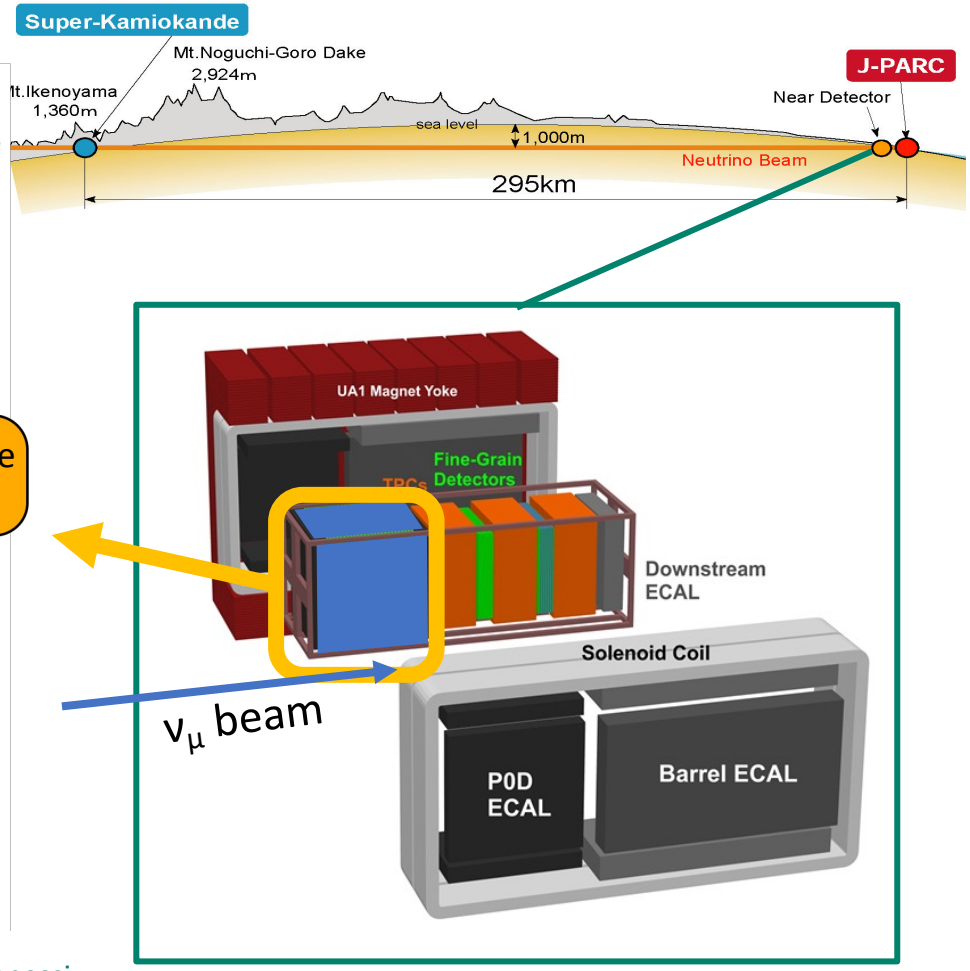


- T2K: Long baseline: Near + Far Detector
- **Neutrino flux** and **neutrino cross section** uncertainties can be constrained using the near detector
- Technology: active scintillator target + tracking gas detectors + ECAL in a 0.2 T magnetic field

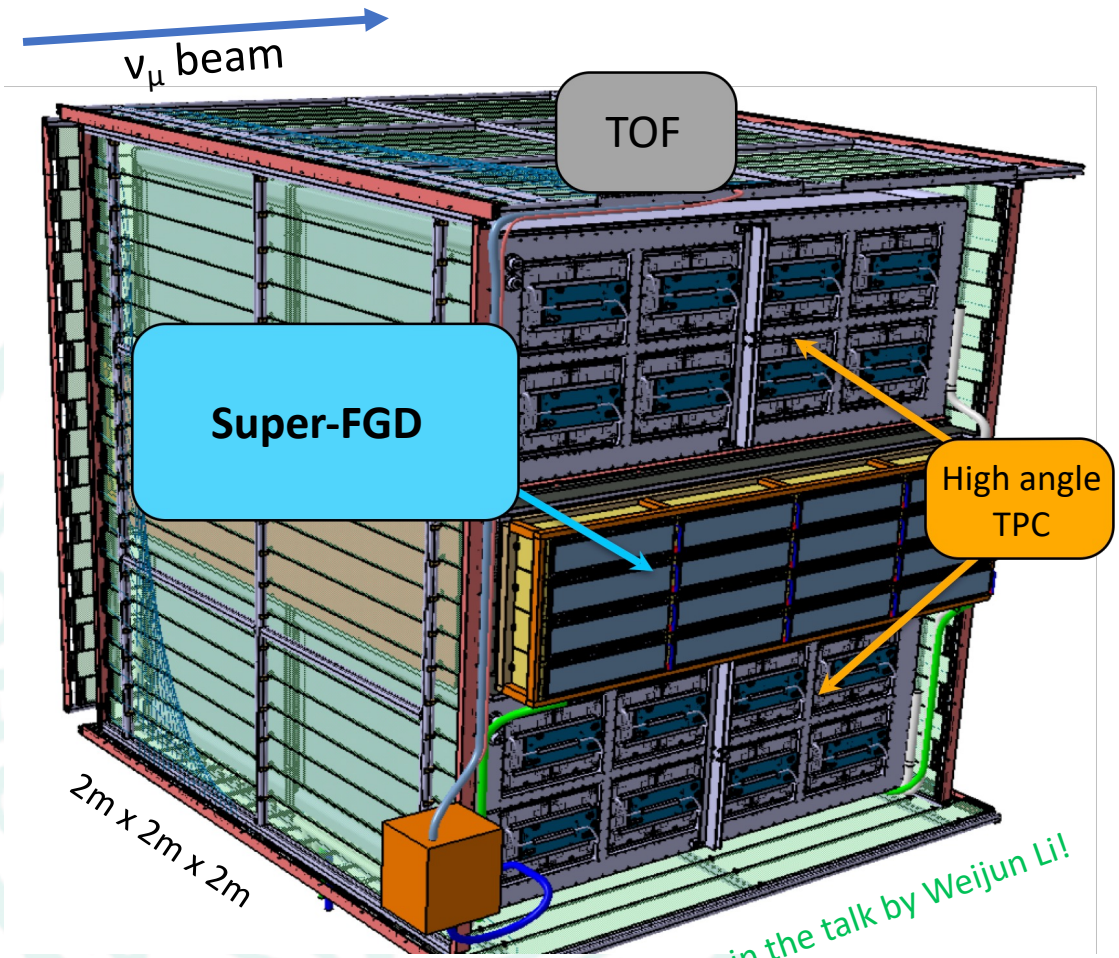


T2K ND upgrade

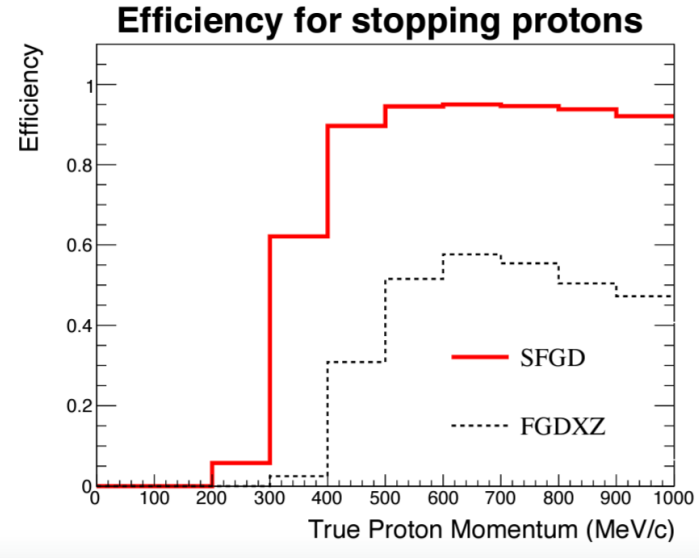




T2K ND upgrade

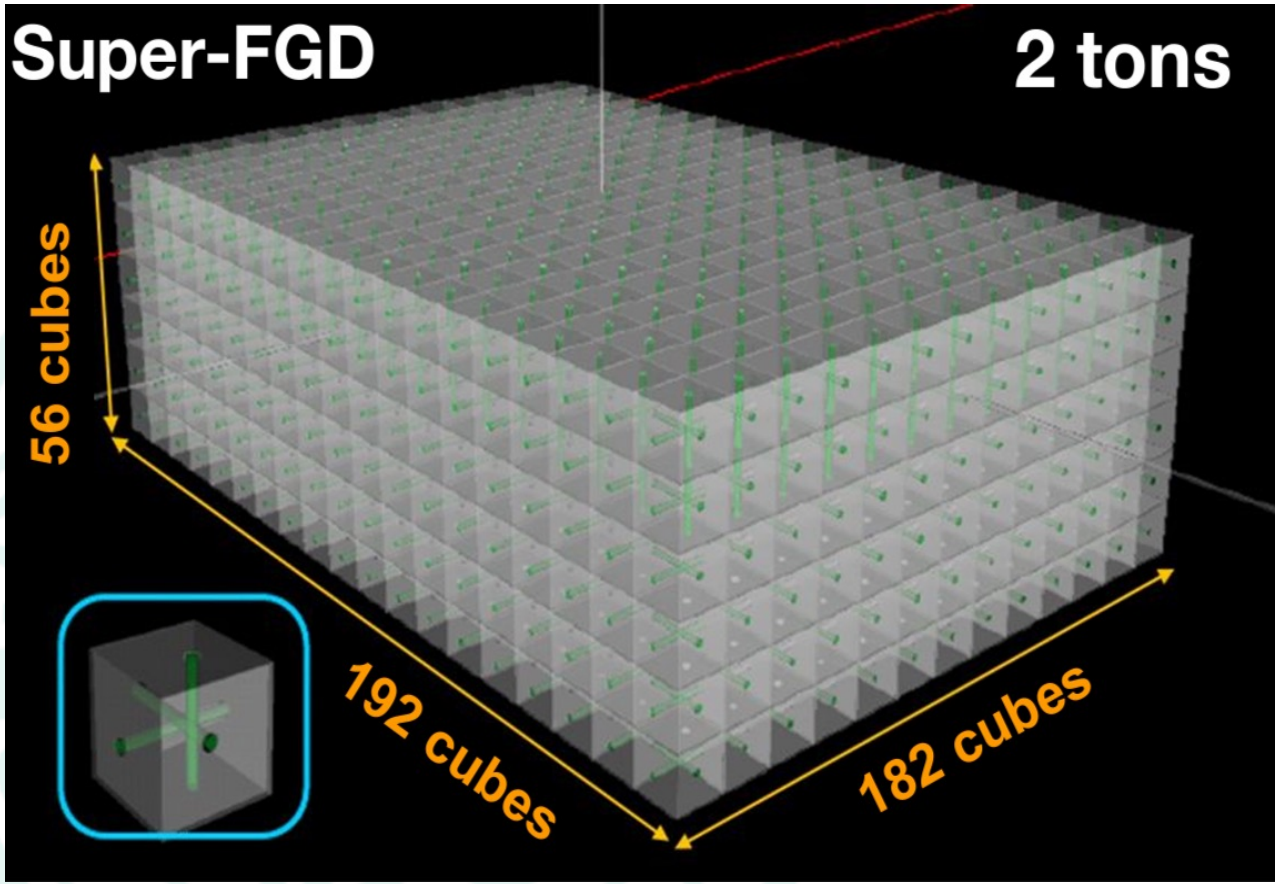


- 2 tons active target with 3D tracking
- Improved angular acceptance
- Neutron detection capabilities
- Low proton momentum threshold

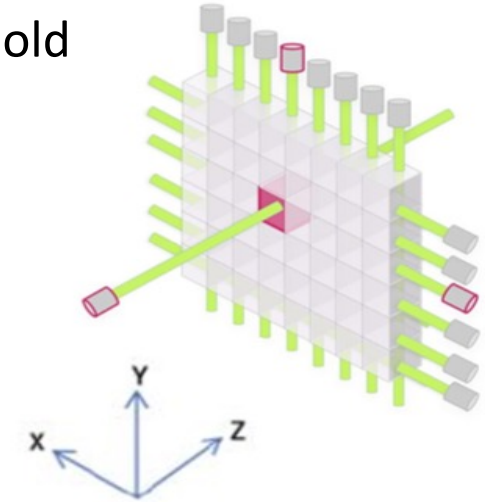


The Super-FGD

The Super-FGD



- 2 millions polystyrene cubes
  - 3D tracking
- WLS fibers + MPPCs light read-out
  - Read 2 millions optical units with "only" **60'000 electronics channels**
- Wide dynamic range
- <1 ns timing resolution
- Low threshold

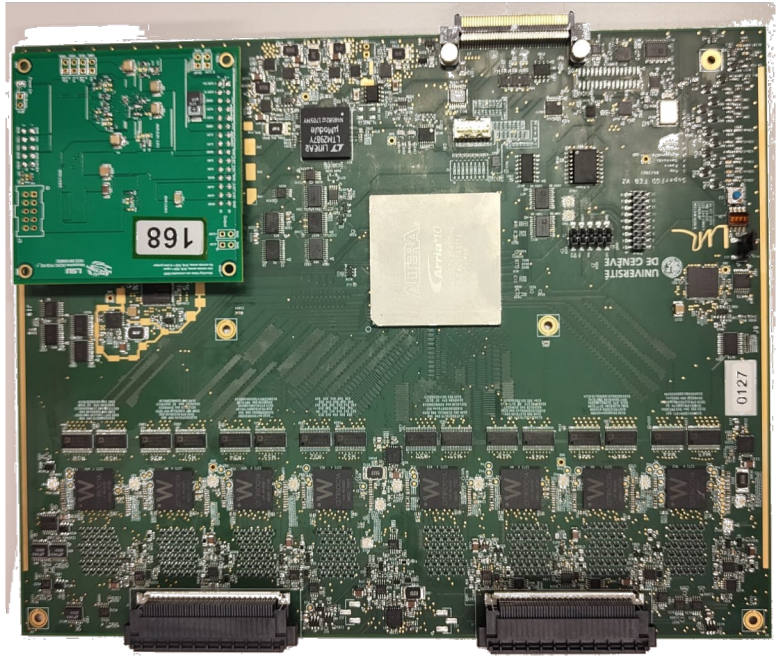


sFGD electronics

Front-End board (FEB)

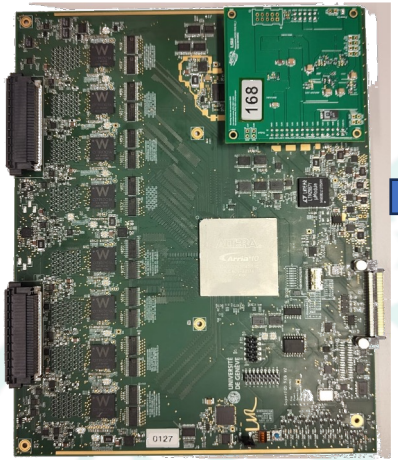
- Univ. of Geneva and LLR Paris
- FPGA ARRIA10 by Intel: DAQ and Slow Control
  - Time stamp: 1.25 ns or 2.5 ns
- 8 CITIROC read-out chips
  - **32 channels each -> 256 ch**
- Per channel: **2** analog paths with peak detection technology
  - High gain and low gain
- Timing information
  - Trigger
  - Time over Threshold

Back: DAQ/SC, sync and power



Front: MPPC signals and HV/T sensors

sFGD electronics



- A total of **222** FEBs employed in the detector
  - to read 56’800 SiPMS

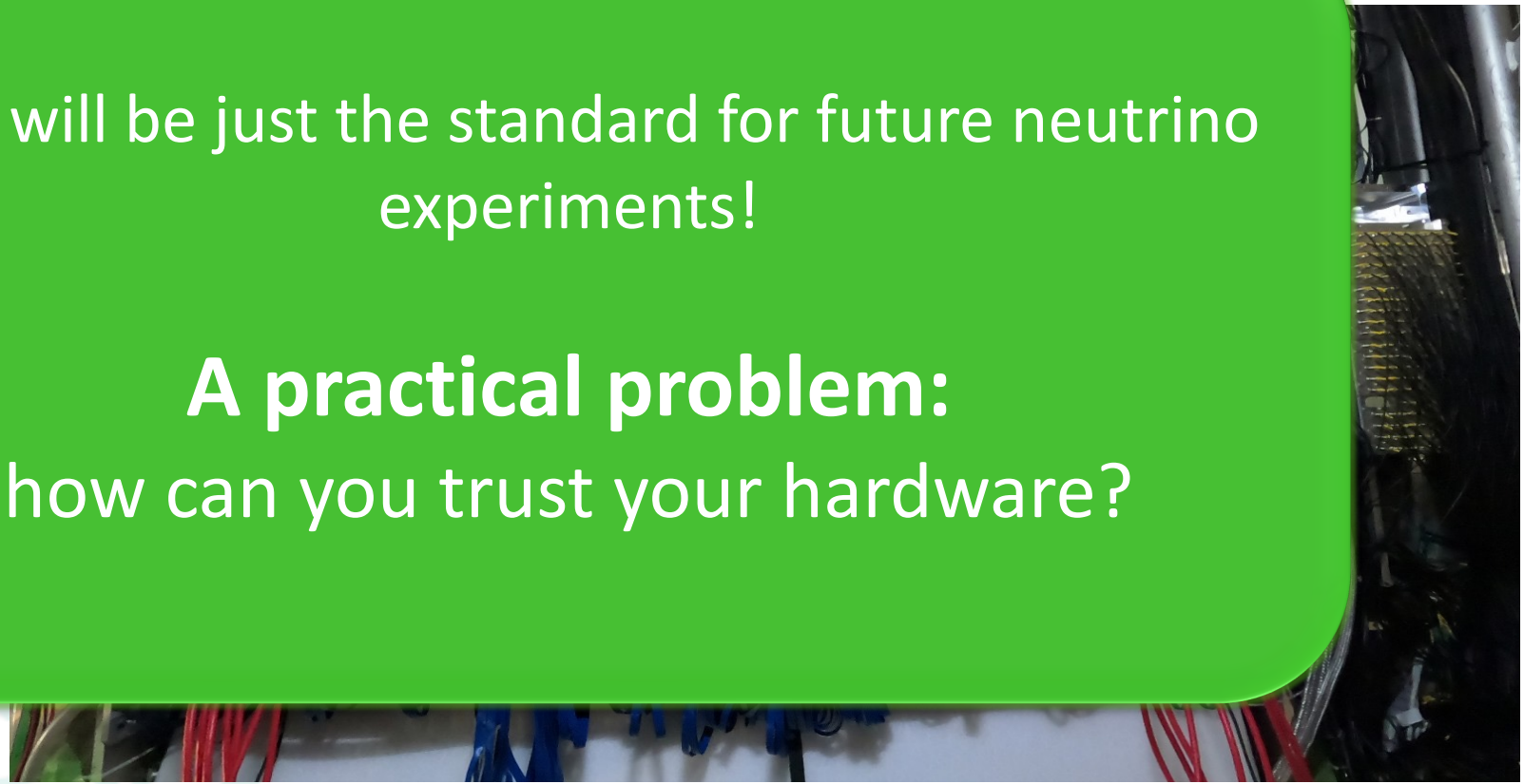
sFGD electronics

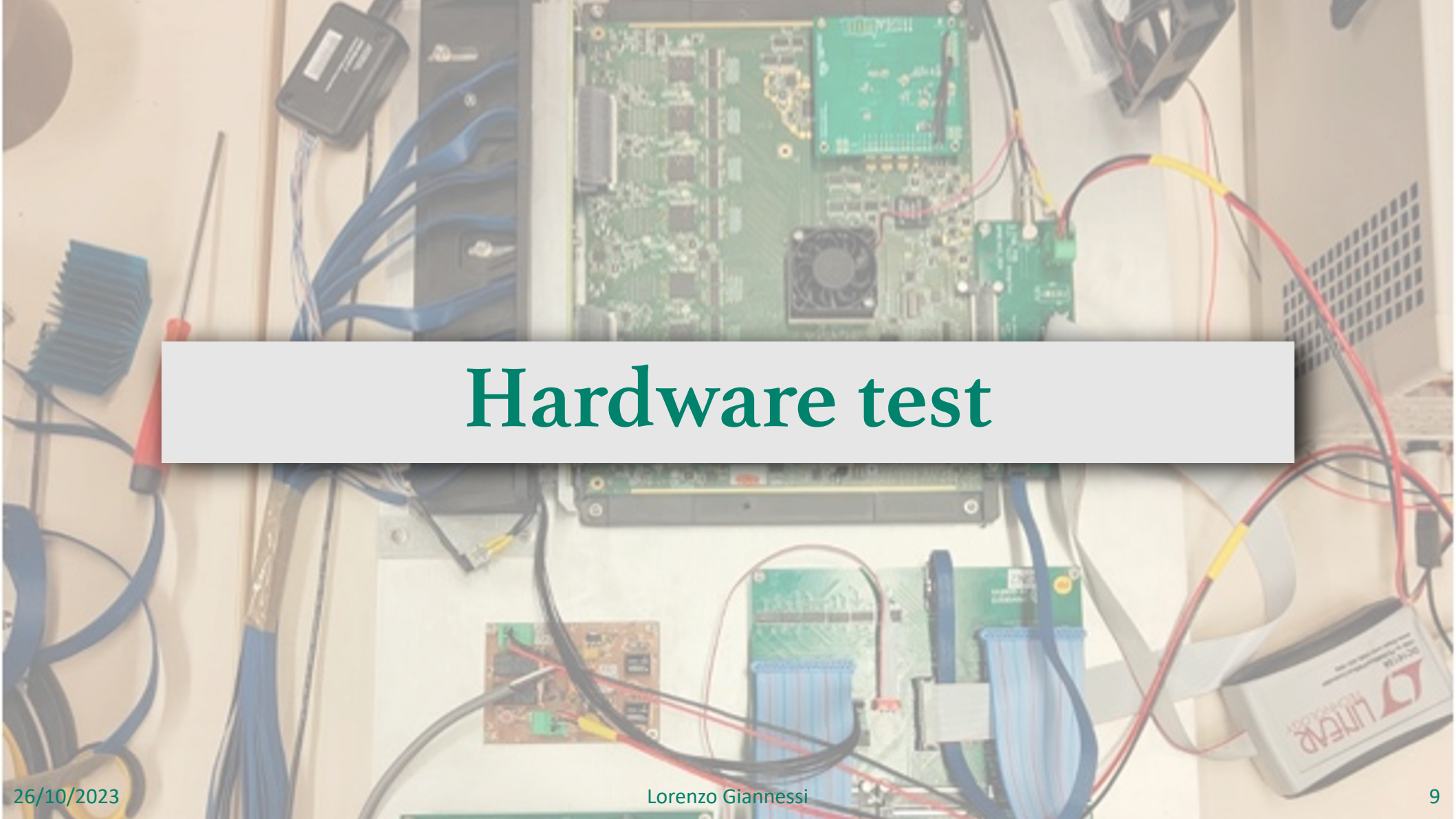
- A total of **222** FEBs employed in the detector

This will be just the standard for future neutrino experiments!

A practical problem:

how can you trust your hardware?

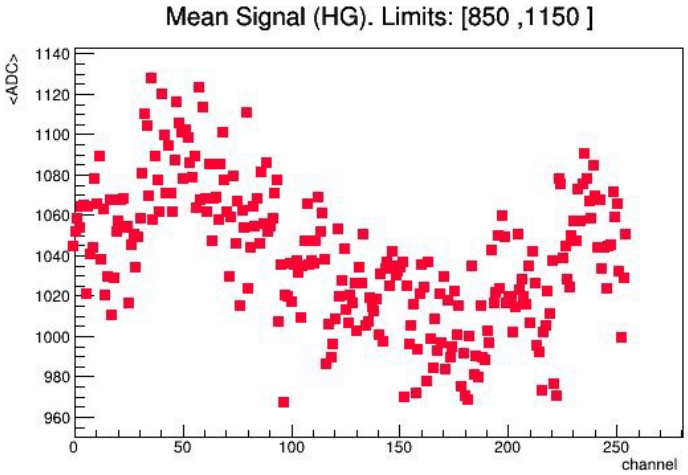


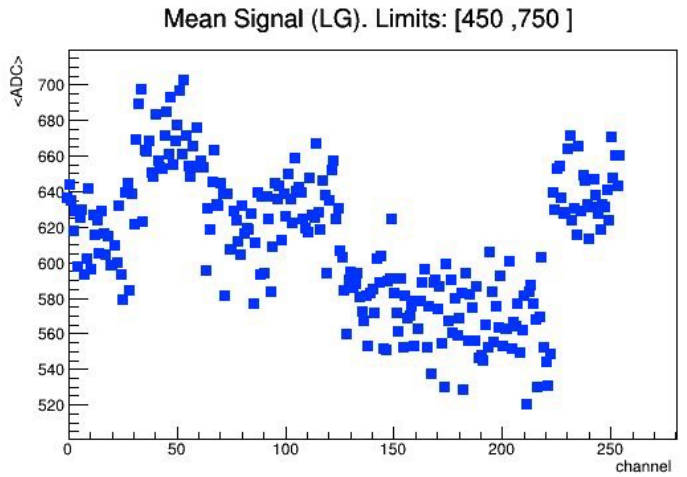


Hardware test

Hardware test

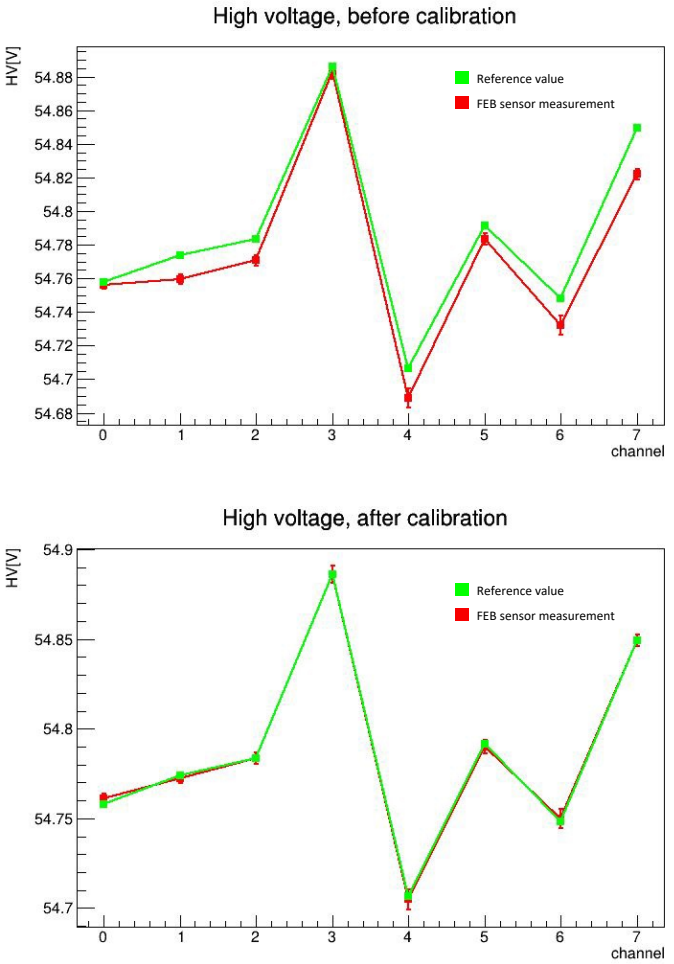
- FEB injected with a known signal in each channel
  - Test of **timing** and **ADC** output





Hardware test

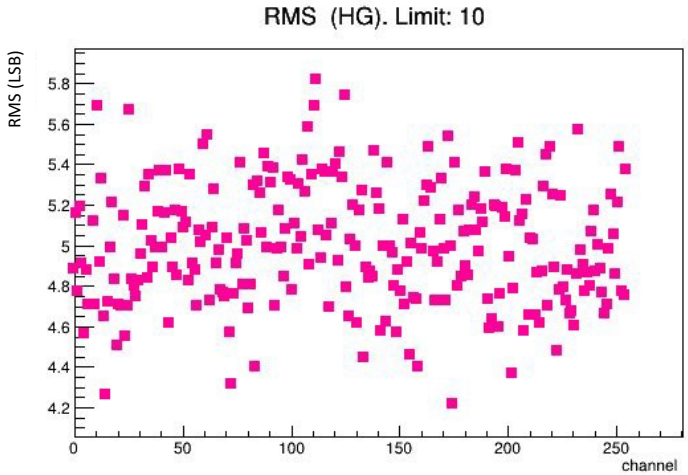
- FEB injected with a known signal in each channel
  - Test of **timing** and **ADC** output
- Test all Slow control lines
- Test and **calibration** of HV and NTC sensors
- Test of safety circuitry exploiting voltage-activated components

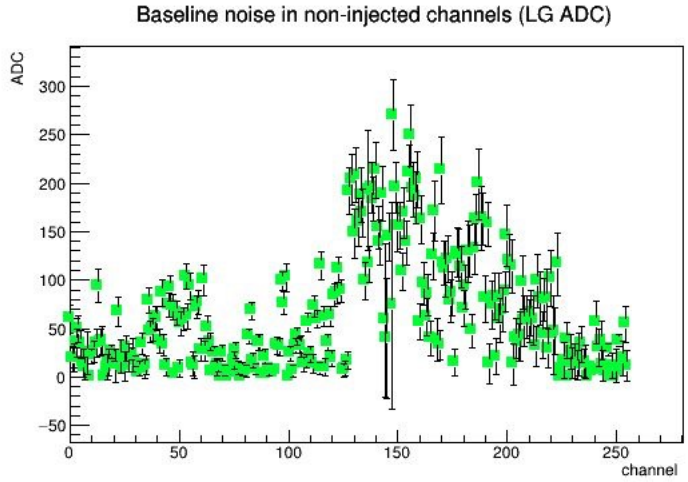


More in the backup!

Hardware test

- FEB injected with a known signal in each channel
  - Test of **timing** and **ADC** output
- Test all Slow control lines
- Test and **calibration** of HV and NTC sensors
- Test of safety circuitry exploiting voltage-activated components
- First order channel-by-channel **noise** assessment
- Produce database with the "*hardware fingerprint*" of each FEB





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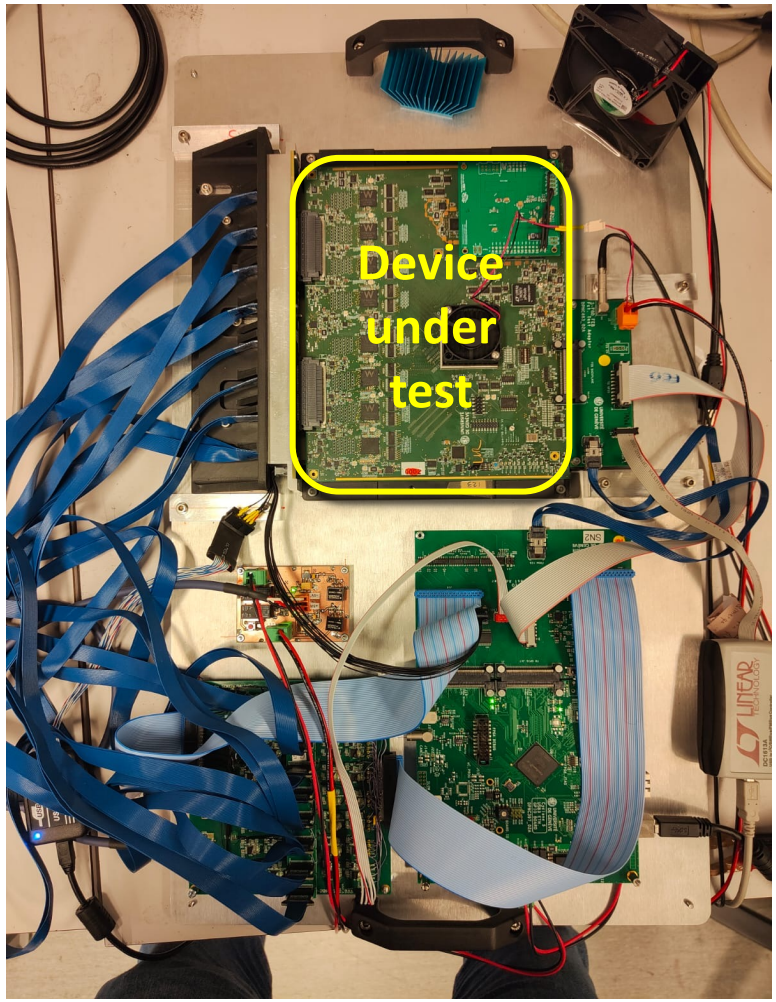
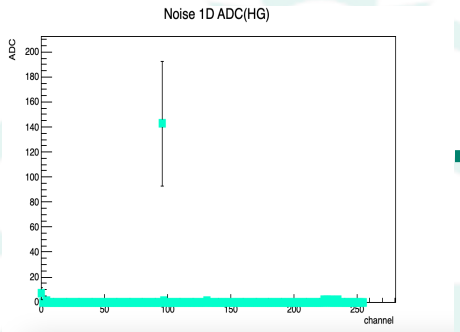
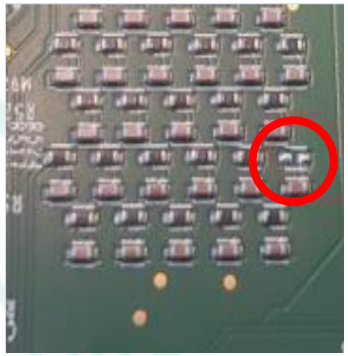
  - Test of **timing** and **ADC** output
- Test all Slow control lines
- Test and **calibration** of HV and NTC sensors
- Test of safety circuitry exploiting voltage-activated components
- First order channel-by-channel **noise** assessment
- Produce database with the "*hardware fingerprint*" of each FEB
- **Table-top, 6 minutes long, plug-and-play**
  - ~ 240 FEBs tested!



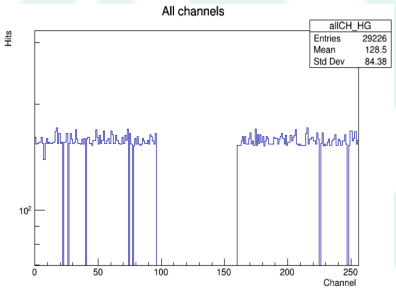
Examples of HW problems detected and **located**

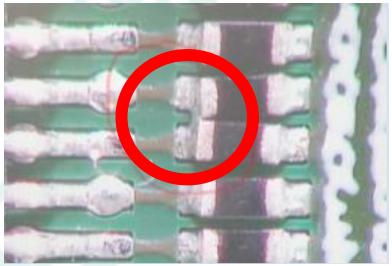
Missing resistor



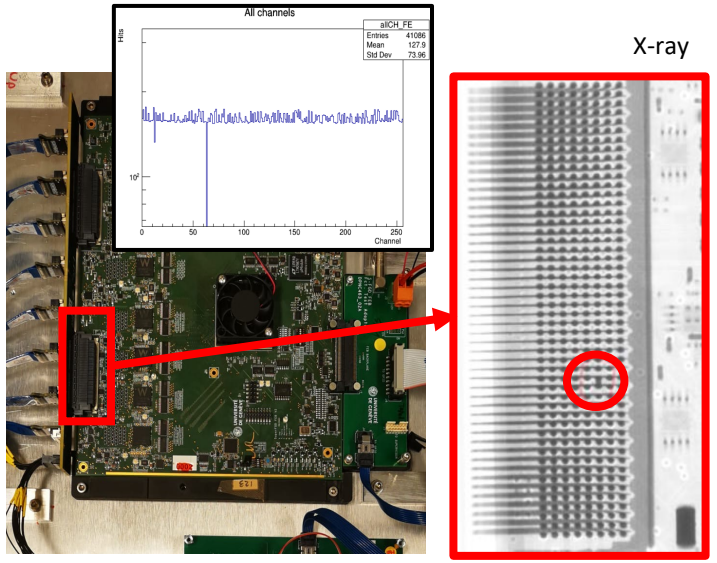


Shorted components





Short circuit in connector



+ Revealed important design improvements from pre-series to final FEB version

Conclusions

- Production of +222 FEBs designed by University of Geneva and LLR
- Tested the hardware of **all** the FEBs, locating and fixing HW problems
- Hardware test setup shipped on-site.
- The Super-FGD (with its electronics) is installed, waiting for new exciting neutrino physics!

Thanks for your attention!

Additional information

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Work performed within the T2K collaboration.

Keywords: neutrino detectors R&D, Super-FGD, T2K, electronics, read-out

Abstract:

The T2K collaboration[1] is upgrading the near detector (*ND280*)[2] with four additional subdetectors: a *time of flight* detector (*TOF*), two *high-angle TPCs (HATPC)*, and the *super fine-grained detector (Super-FGD*). The Super-FGD is the most ambitious project, consisting of 2 million of scintillator cubes read by optic fibers along three directions, allowing three-dimensional track reconstruction in a 2-tons fiducial mass detector. The remarkable advantages are low proton detection momentum threshold, neutron detection ability, and 4π angular acceptance. A crucial element for the success of this detector is the Front-End electronics, comprising more than 200 Front-End Boards (FEB) based on the CITIROC chips, reading almost 60'000 thousands SiPM channels.

When dealing with such complex electronic devices, the producing companies do not have the knowledge to test the hardware in what is relevant from a physics standpoint, thus it is the job of the physicist to design a test bench that proves the reliability of the read-out electronics.

This talk presents a novel, custom-made test bench, entirely developed at the University of Geneva, to reliably test the hardware of the 243 FEBs produced for the Super-FGD, and locate any hardware problem. This setup allowed us to test the quality of the Front-End boards in all their features: connection of readout channels, slow control lines, voltage and temperature sensors, and safety circuitry in a very short time (6 minutes per FEB), with a table-top setup and user-friendly software. Furthermore, this setup will be used during the detector run for on-site diagnostics of the electronics.

Funds:

This work was funded by Swiss national fund (SNSF) grant number #200020_204609 and #20FL20_201477

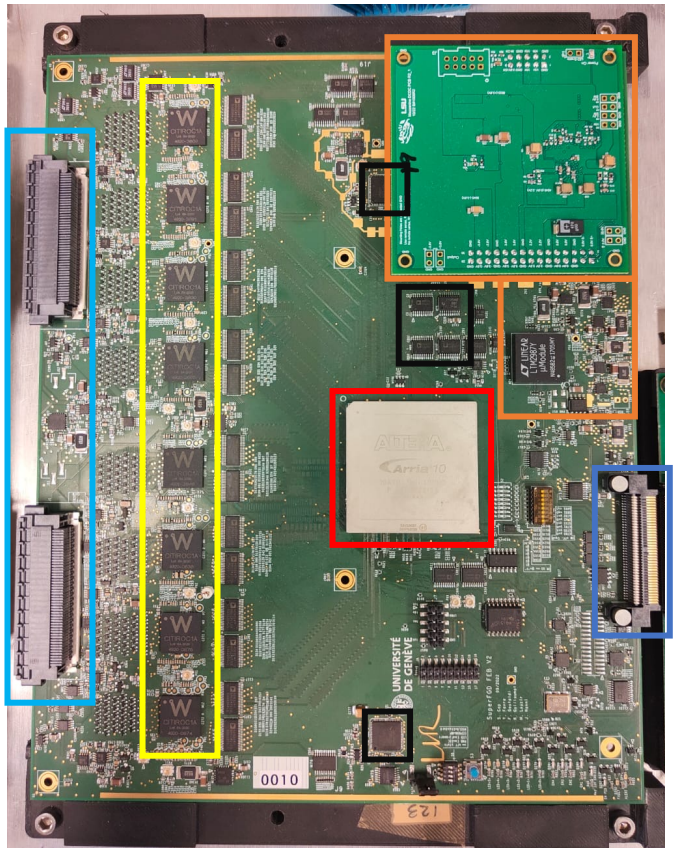
References:

[1] The T2K Experiment, NIM A, 659, 1, 2011, 106-135, https://doi.org/10.1016/j.nima.2011.06.067

[2] T2K ND280 Upgrade -- Technical Design Report, the T2K Collaboration, 2020, arXiv: 1901.03750

Back up

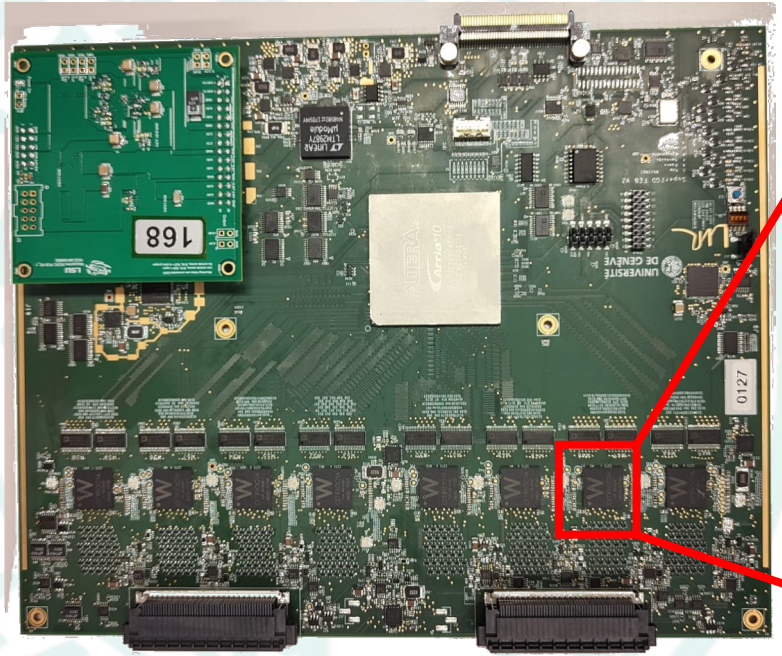
- Power mezza and “power region”: The chip in the power region is the supervisor chip that checks if all the DC-DC converters are working as expected
- FPGA: the core of the FEB that handles slow control functions (CITIROC and ADC config), passes data from CITIROC to DAQ, …
- CITIROC chips: 8 32channes chip that perform triggering, amplification and shaping of the signal. The output analog signal goes to external ADC placed on the FEB
- Connectors to MIB: (MPPC Interface Boards) to which the MPPC are connected via “blue ribbon” cables
- Backplane connector
- **ADC**s



sFGD electronics: the FEB

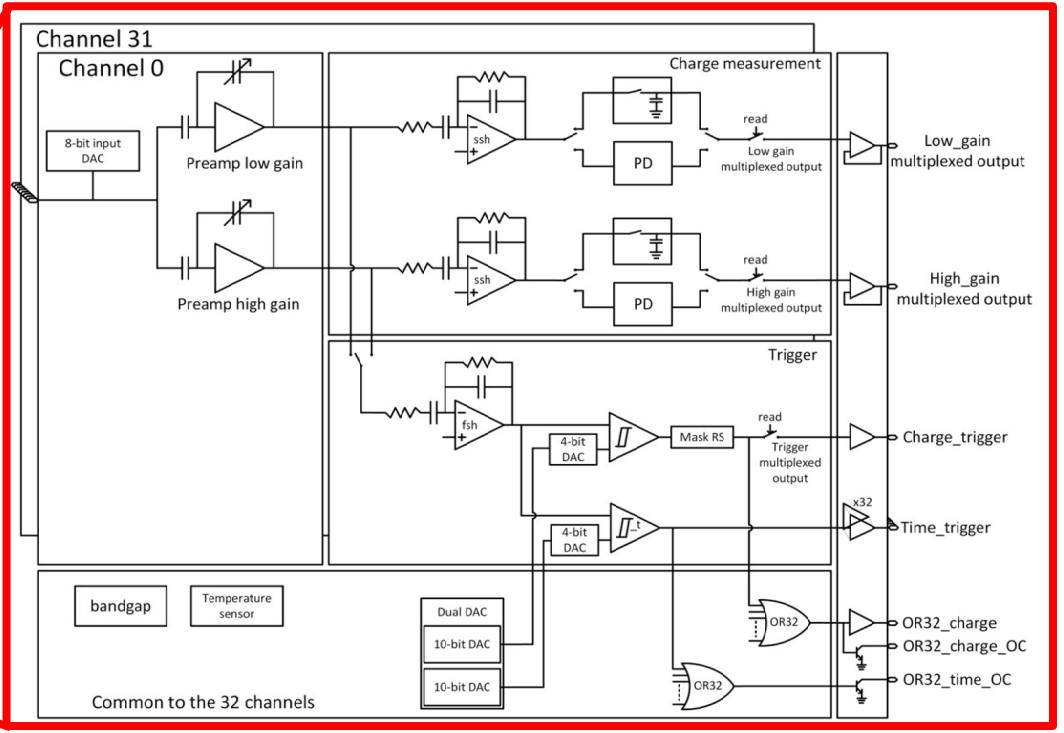
- FPGA ARRIA10 by Intel controls DAQ and SC
  - Time stamp: 1.25 ns
- 8 CITIROC[2] read-out chips -> **256 ch**

Back: DAQ/SC, sync and power



Front: MPPC signals and HV/T sensors

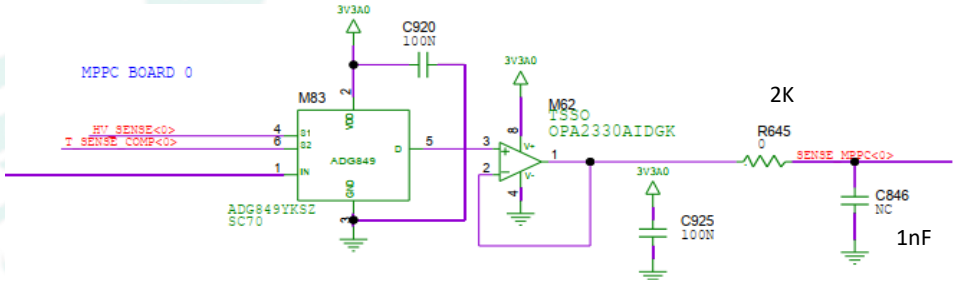
- 2 analog paths per channel with peak detector
  - High gain and low gain
- Timing information (trigger and ToT)



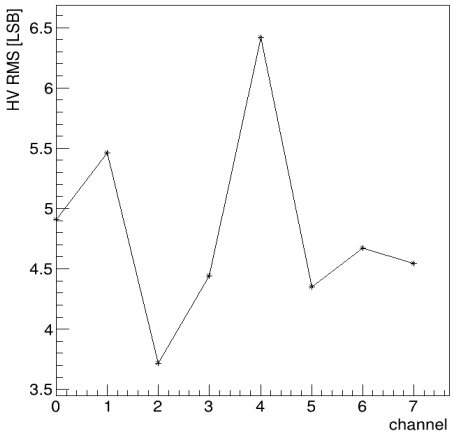
CITIROC chip schematics

Hardware test: RC filter

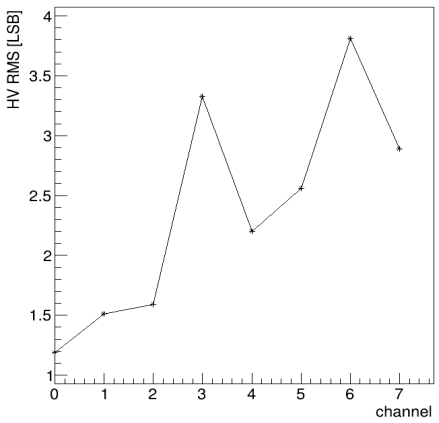
- **Calibration** of HV and NTC sensors
  - **Check presence of RC filters**

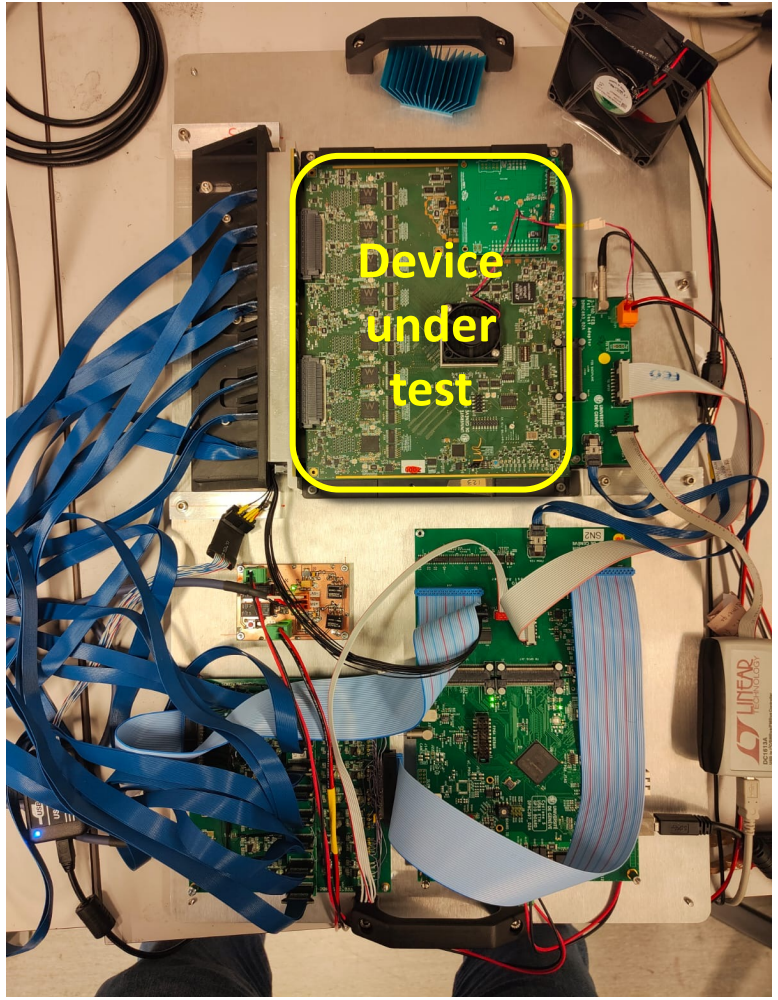


HV RMS (no RC)



HV RMS (with RC)



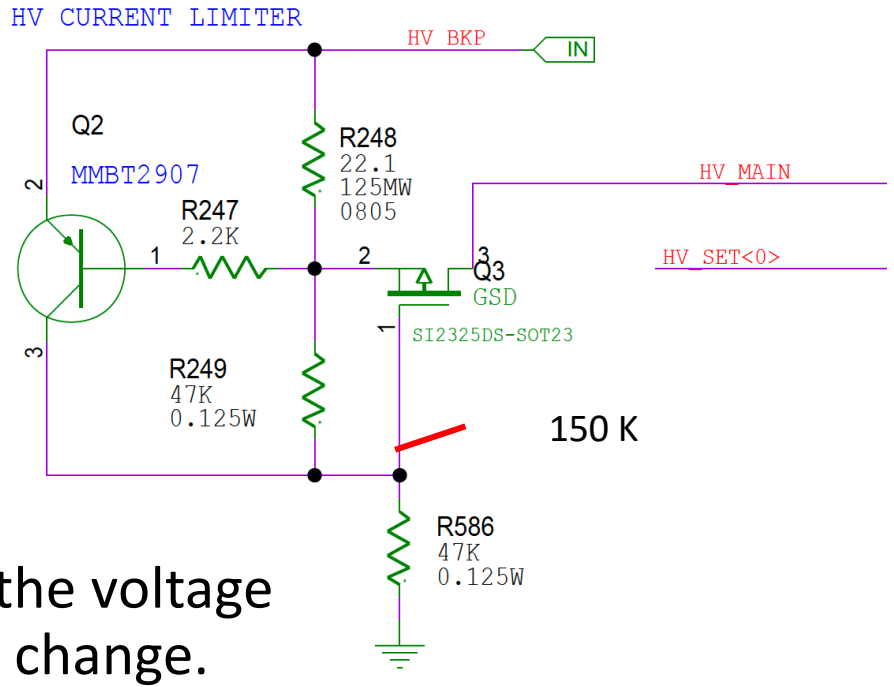


Hardware test: safety circuit

- We want to make sure that the resistor in the current limiter circuit is 150KΩ.
- The GS threshold voltage is between -2.5 and -4.5 V
- V_{GS} is computed as (given R=R586):

$$V_{GS}=V_{PS}\cdot\left(\frac{R}{(47+R+0.022)}\right)-\left(V_{PS}\cdot\frac{(47+R)}{(47+R+0.022)}\right)$$

V_{PS}: voltage set on Power supply



- For the same V_{PS} , if the resistance changes, the voltage applied on the GS terminals of the transistor change.
- With higher R, the V_{PS} necessary to enable the transistor is higher

SPECIFICATIONS T_J = 25 °C, unless otherwise noted

Parameter	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = - 250 µA	- 150			V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 2.5		- 4.5	