CMS - CdG T1

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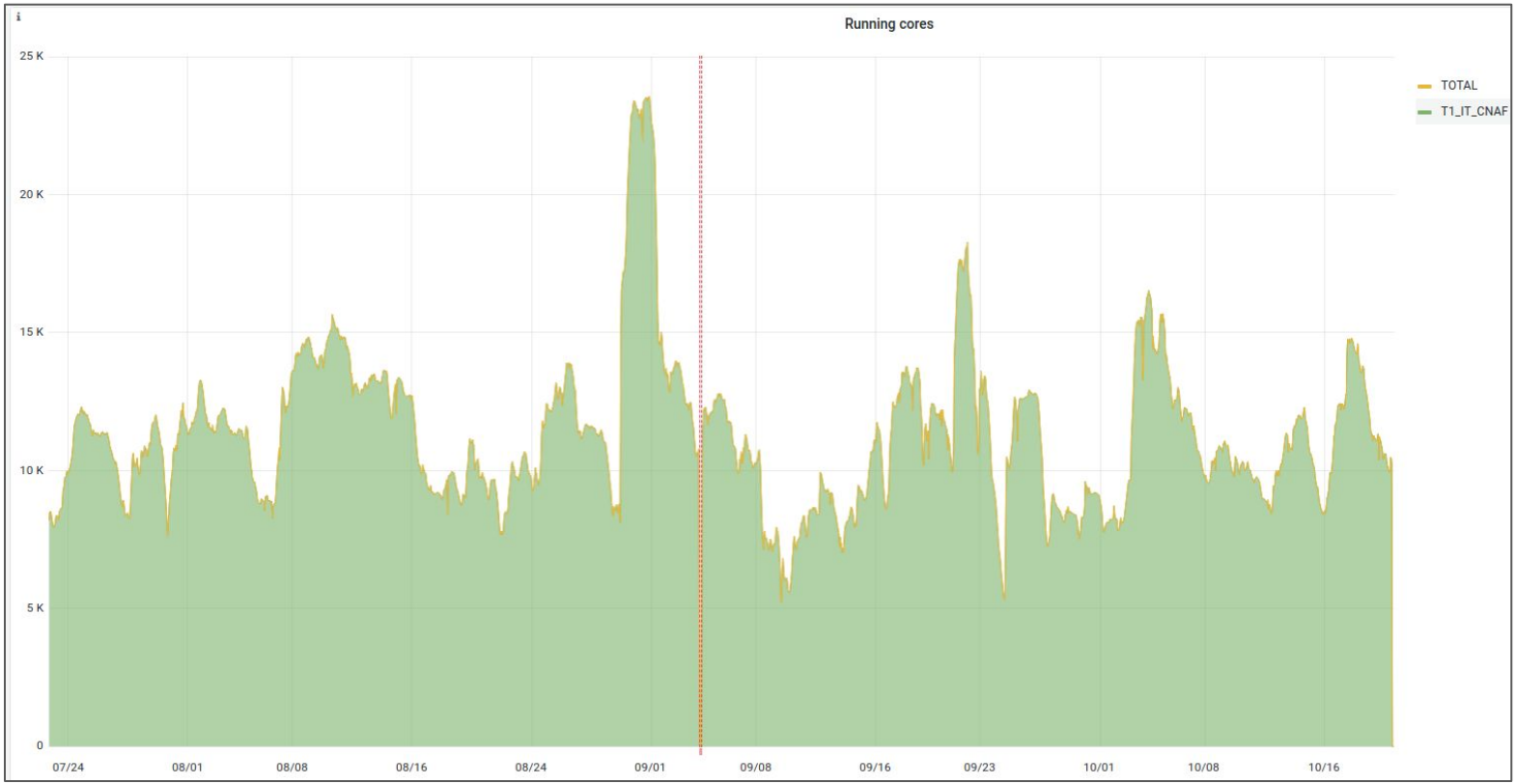
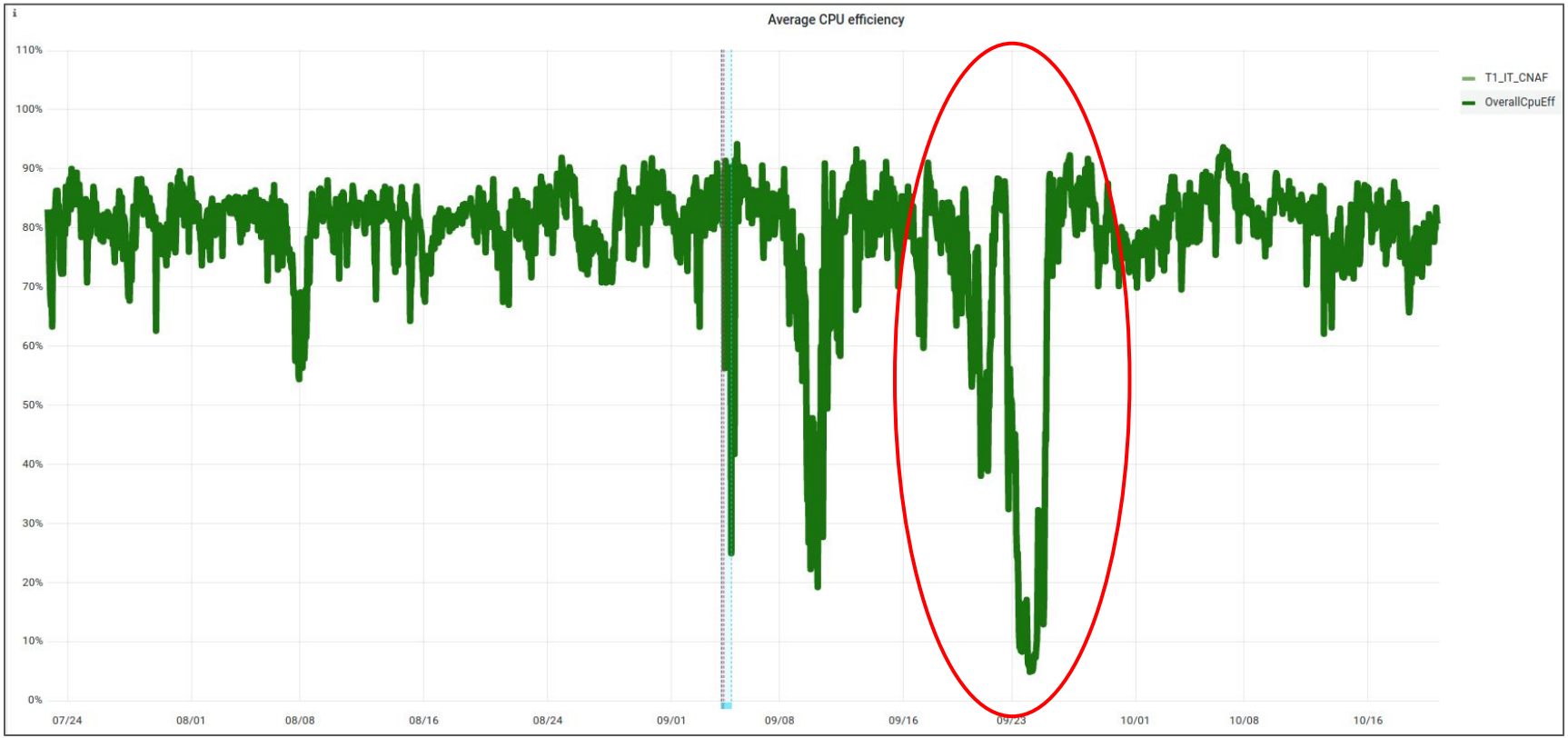
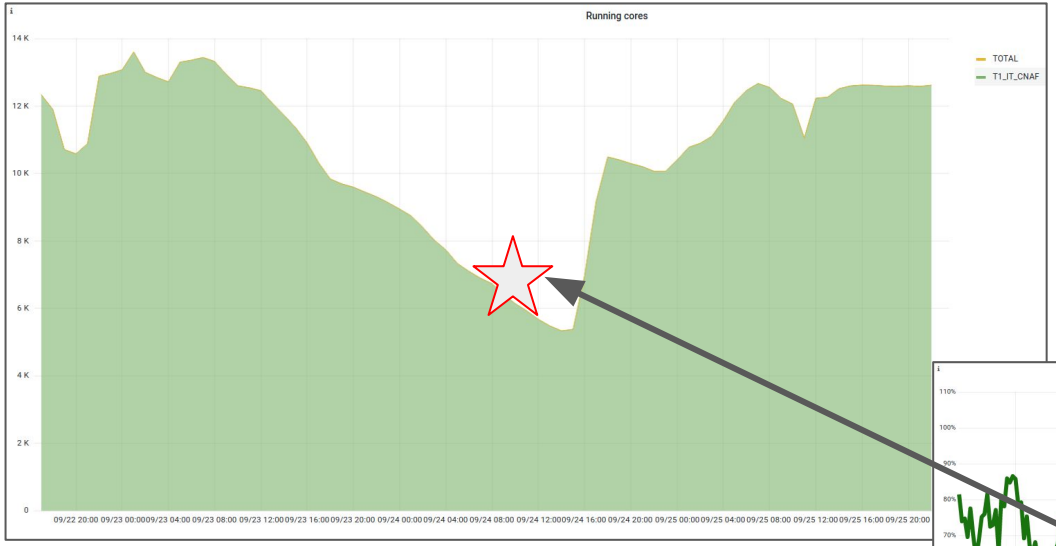
Utilizzo Risorse Tier1



Efficienza di CPU @CNAF

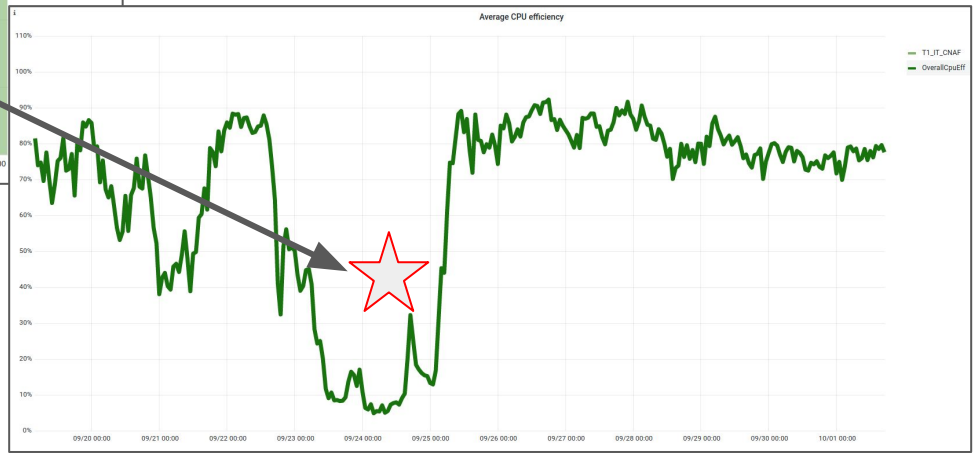


Debugging del problema..



In estrema sintesi il sito è andato in drain per il fallimento dei sam test di cui ci ha parlato Lucia

- **Failing SAM tests in tape storage area, cleaned by garbage collector (GGUS)**



R&D AF: validazione dell'infrastruttura

Ad oggi abbiamo dimostrato che l'infrastruttura distribuita e' pronta ad essere usata per analisi interattiva attraverso framework nuovi (RDataFrame, Coffea)

- Il focus è **raccogliere misure ed informazioni per avviare discussioni e ricevere nuovi input**

- L'obiettivo e' quello di contribuire in CMS alla definizione della direzione da seguire

Preselection		
	Legacy	**RDF (O2)**
Overall time	3h 40min	25min
Overall rate	1095 Hz	7306 Hz
Event-loop rate	1192 Hz	8473 Hz
Overall network read	488 GB	371 GB
Average RSS per-node	Ca. 13 GB	Ca. 17 GB
Postselection - 1st scenario		
	Legacy	**RDF**
Overall time	0.25h	0.08h
Overall rate	306 Hz	855 Hz
Event-loop rate	412 Hz	1976 Hz
Overall network read	11 GB	10 GB
Average RSS per-node	Ca. 1 GB	Ca. 15 GB

Power architecture validation è completa

FullSim

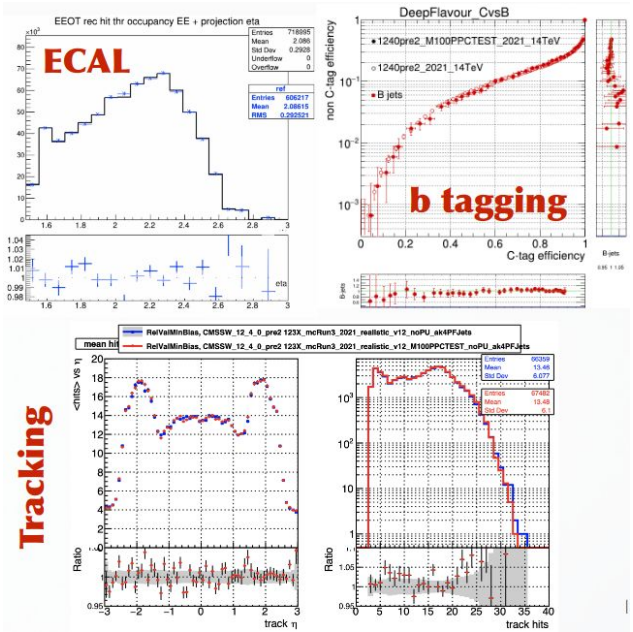
Release Name	Tracker	Ecal	HGcal	Hcal	CASTOR	DT	CSC	RPC	GEM	MTD	PPS	L1	Tracking	Electron	Photon	Muon	Jet	MET	bTag	Tau	PF	Info	RelMon
12_4_0_pre2_M100PPC	✓	✓	–	✓	–	✓	✓	✓	–	–	–	–	✓	✓	✓	✓	✓	✓	✓	✓	✓	i	⛶

L'architettura Power CPU può ora essere utilizzata per la generazione e l'elaborazione di dati

- Validazione tecnica **OK.** Validazione della fisica **OK**
- Ora possiamo utilizzare M100 (e in US -> OLFC Summit) in produzione

Inoltre:

- **Tutto il sistema di computing è pronto ad usare qualunque architettura. CMS ha software compilato per x86, Power e ARM**



Quali sono i prossimi passi

We plan to use M100 to extends T1_IT_CNAF for production activities, following the transparent extension approach

- Need to cope with the 10GB GPN “constraint”

Currently we are restarting with backfilling (thanks Hasan !)

- New workflow defined with PdMV and managing the backfill thanks to the CompOps recipe

Few options as next step

- Uses TaskChain targeting T1_IT_CNAF and then we run GEN/SIM @M100 Digi/Reco at regular CNAF.
- Thanks to the multiarch support enabled we can do this transparently using the “custom match rules” to apply proper “filtering”
  - We did such a test
  - We might need some support from SI to define correctly the matching rules
- How much: (the INFN allocation is of the **Order of 3M CoreHrs per year)**
- **Uses StepChain but at lower scale**
  - **Need to better evaluate what it could be actually achievable.**

Excerpt of a CMS Workflow description


```
{
  "_id": "spiga_TC_SLC7_Marconi_TB_CMS_Marconi_220729_194721_8502",
  "PrepID": "TEST-CMSSW_11_2_0__fullsim_noPU_2021_14TeV-1608392371-ZMM_14",
  "RequestString": "TC_SLC7_Marconi_TB_CMS_Marconi",
  "Comments": {
    "CheckList": "",
    "WorkFlowDesc": ""
  },
  "ProcessingString": {
    "Digi_2021": "Digi_2021_TC_SLC7_Marconi_CMS_Marconi_TBv20210430_test",
    "Reco_2021": "Reco_2021_TC_SLC7_Marconi_CMS_Marconi_TBv20210430_test",
    "ALCA_2021": "ALCA_2021_TC_SLC7_Marconi_CMS_Marconi_TBv20210430_test",
    "ZMM_14TeV_TuneCP5_2021_GenSim": "ZMM_14TeV_TuneCP5_2021_GenSim_TC_SLC7_Marconi_CMS_Marconi_TBv20210430_test"
  },
  "ScramArch": [
    "slc7_ppc64le_gcc9",
    "slc7_amd64_gcc900"
  ],
  "SizePerEvent": 1234,
  "Memory": 3000,
```


Requirements = **(stringListMember(TARGET.Arch,"ppc64le,X86_64"))** && (TARGET.OpSys == "LINUX") && (TARGET.Disk >= RequestDisk) && (TARGET.Memory >= RequestMemory) && (TARGET.Cpus >= RequestCpus) && (TARGET.HasFileTransfer)