# FPGA-based Hadron Fluence Sensors

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# Outline

- Motivation
- SRAM-based Field Programmable Gate Arrays
- Sensor and Interface Boards
- Use Case at Belle II
- Conclusion

# Motivation

- Hadrons with energy>few MeV may indirectly induce SEUs in SRAMs
  - thermal neutrons (~25 meV) can also be detected if the fabrication includes Boron ($^{10}B + n \rightarrow \alpha + {}^{7}Li$)

hadron fluence

cross section per bit

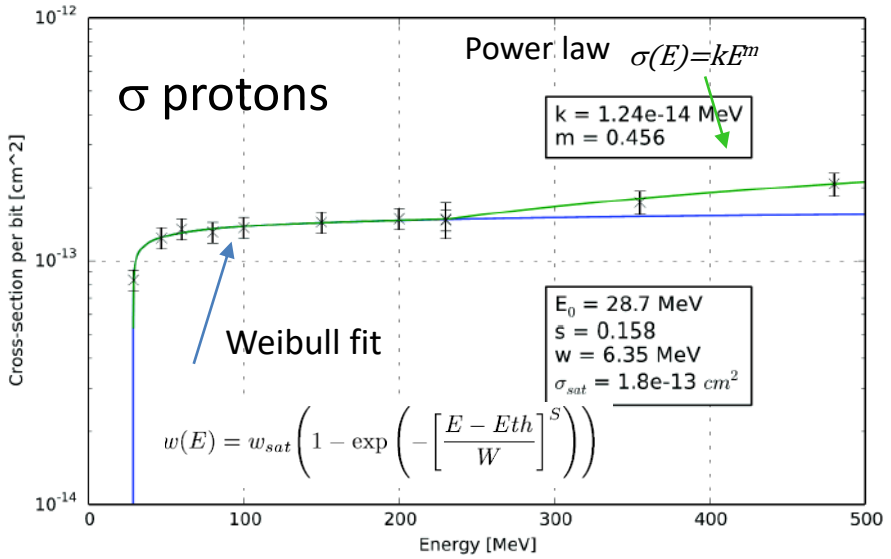
$$\Phi = \frac{N_{upsets}}{\sigma\, N_{bits}}$$

upset count

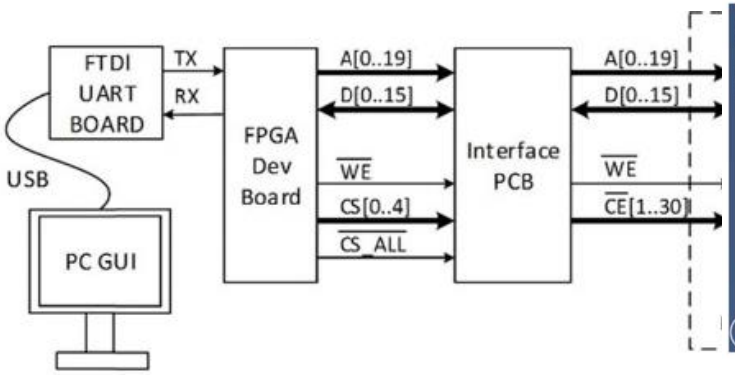
memory size

- $\sigma = \sigma(\text{device}, V_{DD}, \text{hadron}, E)$
- device must be latch-up free and TD-tolerant
- State-of-art solutions [1,2,3]: sensor SRAM + readout FPGA

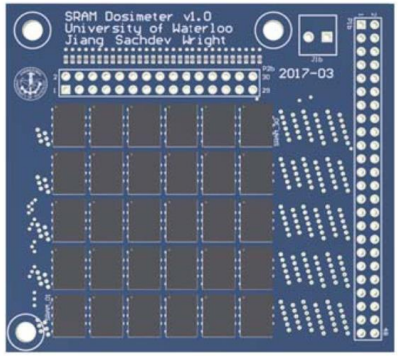
SRAM Cypress CY62157EV30 8Mb (90nm) [1]




SRAM readout chain [3]




SRAM array

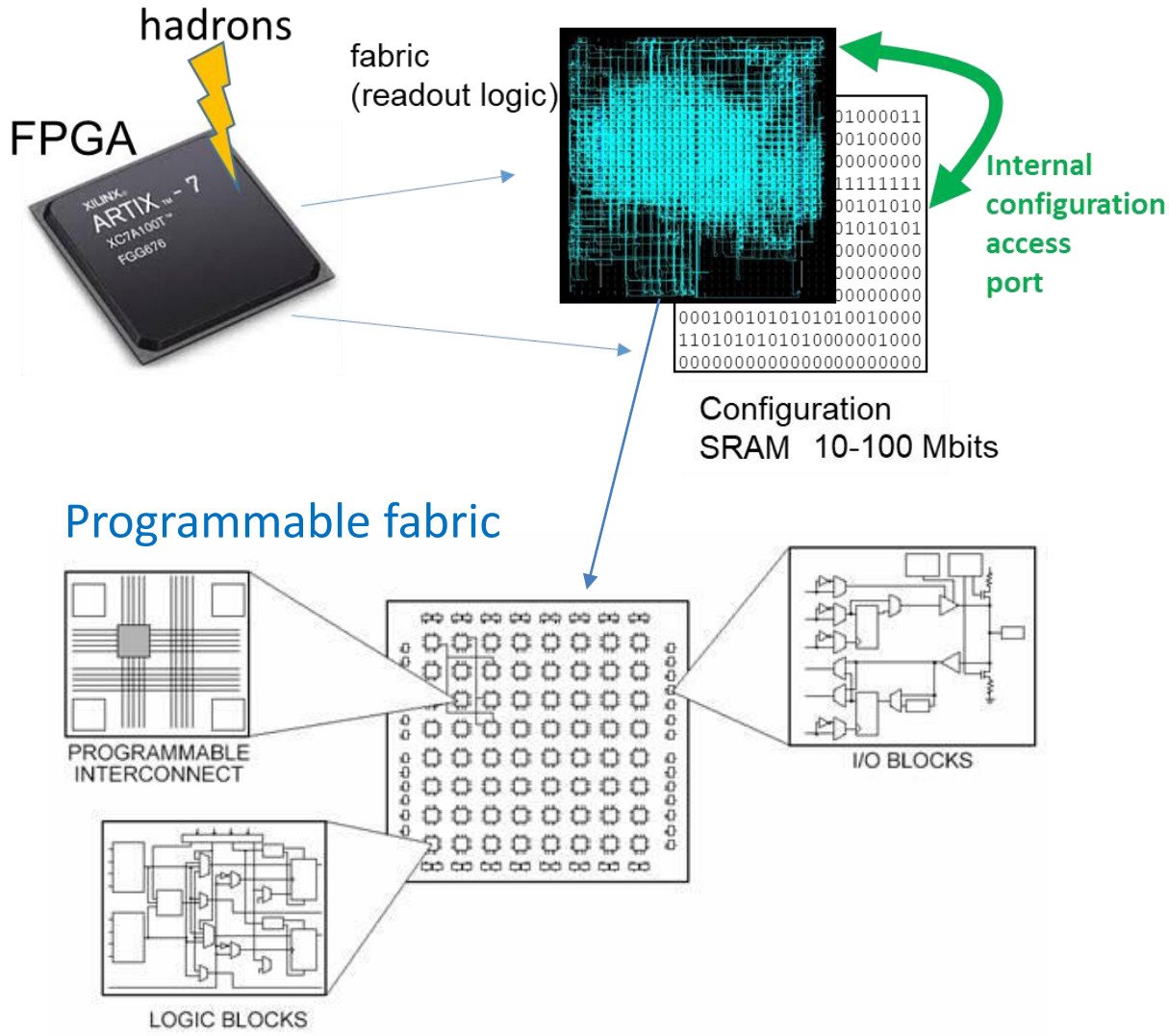



Radiation beam


[1] S. Danzeca et al., 2014, doi: 10.1109/TNS.2014.2365042
[2] K. S. Ytre-Hauge et al., 2019, doi: 10.1016/j.radmeas.2019.01.001
[3] E. Blackmore et al., 2019, doi: 10.1109/TNS.2018.2884148

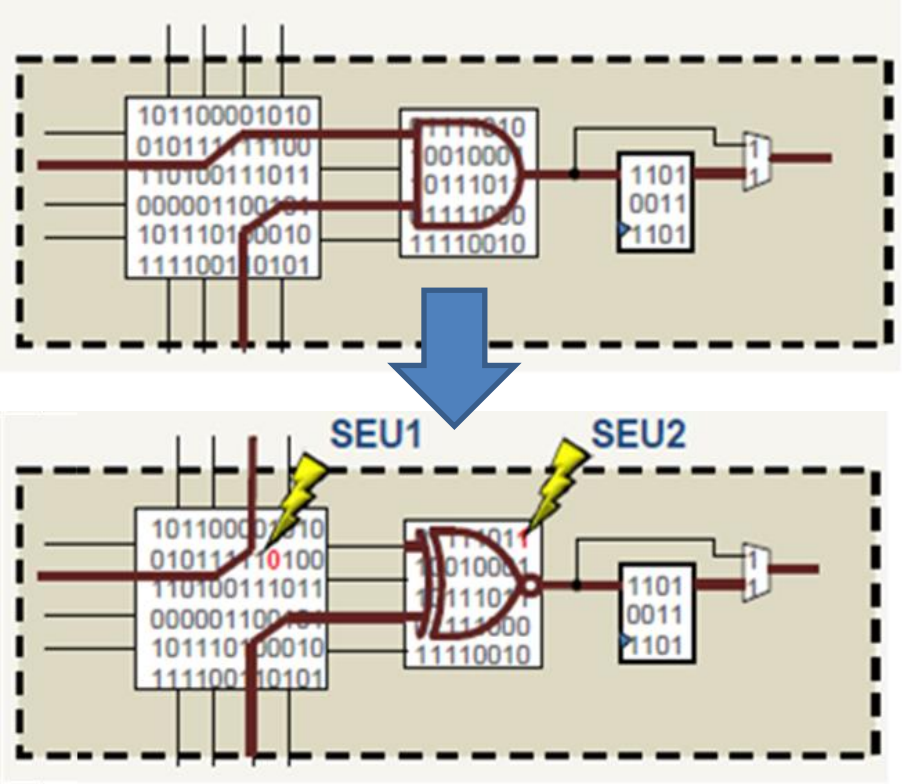
# SRAM-based Field Programmable Gate Arrays

- FPGAs embed programmable fabric and configuration SRAM (CRAM)
- Programmable fabric can access CRAM via dedicated internal port (ICAP for Xilinx)
- Many devices are TD-tolerant (>few kGy) and latch-up free
- FPGA as compact hadron fluence counter
  - CRAM as sensitive element + fabric programmed as readout
- PHI R&D funded by INFN CSNV (2021-2022)



# Upsets Vs Configuration

- Challenge: upsets (*what we want to measure*) may disrupt the readout logic (*our transducer*)

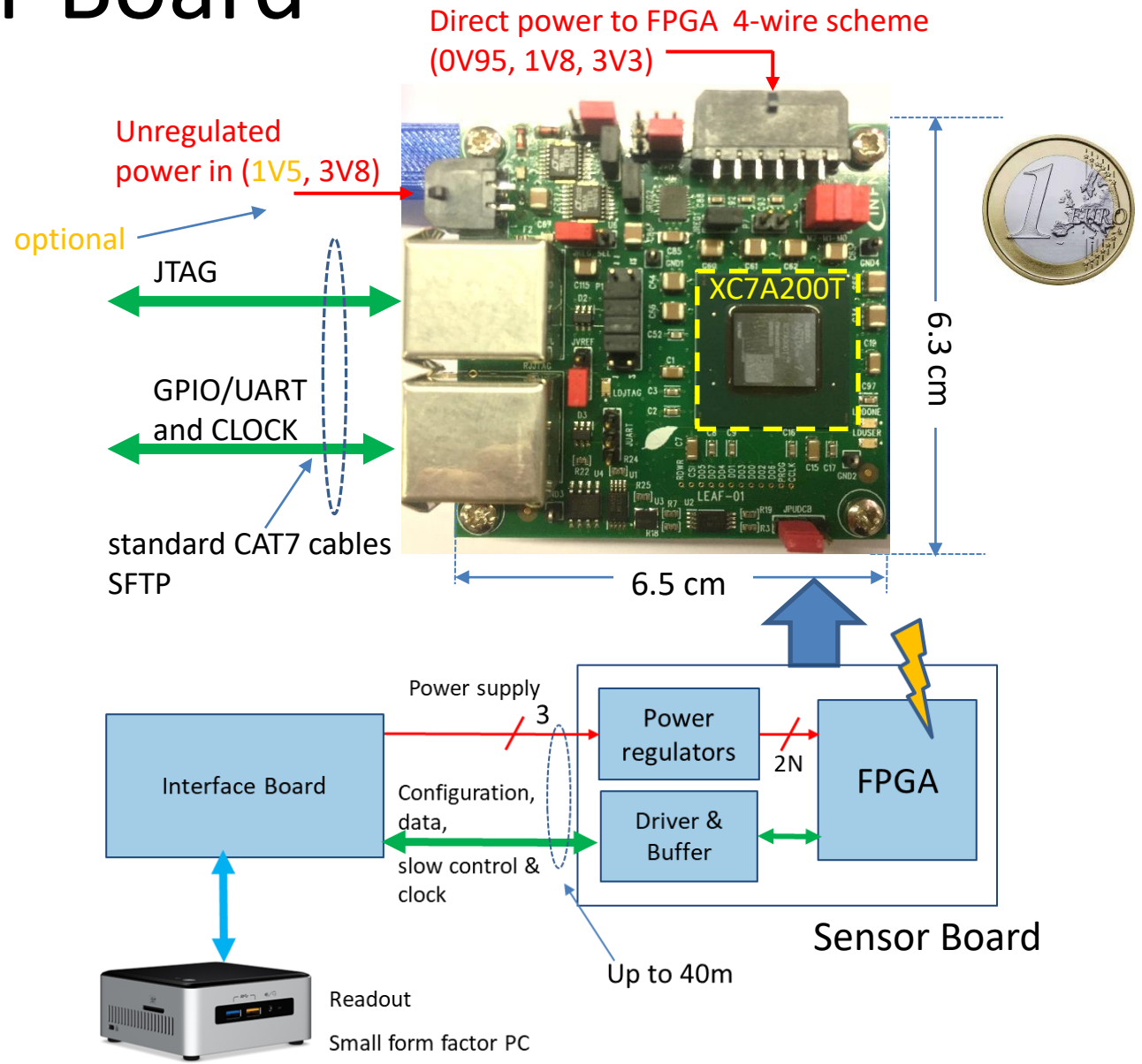



- Readout logic main features
  - detect and correct upsets in CRAM => self-correct functionality
  - self-contained (no external memories for reference bitstream)
  - provide details about upsets (timestamp, memory address, bit offset, polarity)

- Radiation Hardening By Design
  - PCB, firmware, redundant CRAM content

# Sensor Board

- Compact board (6.3cm x 6.5cm)
  - Only COTS components, radiation tolerance studies in [1,2]
  - Dual power input mode: direct or via-regulators
  - Low power consumption (~0.7 W)
- Xilinx Artix-7 200T
  - 28nm CMOS
  - 59 Mb CRAM + 18 Mb BRAM
  - Expected proton-SEU $\sigma = 9.4 \cdot 10^{-15}$ cm$^2$, sensitivity = 1.4 $10^6$ pp/cm$^2$

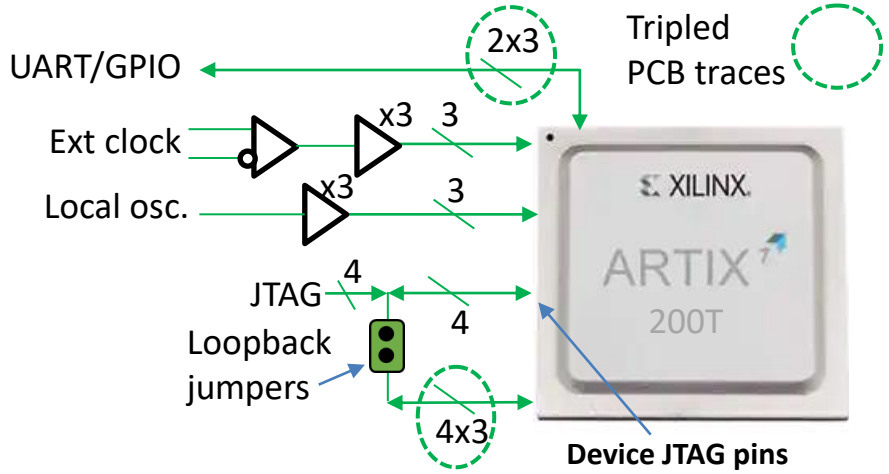


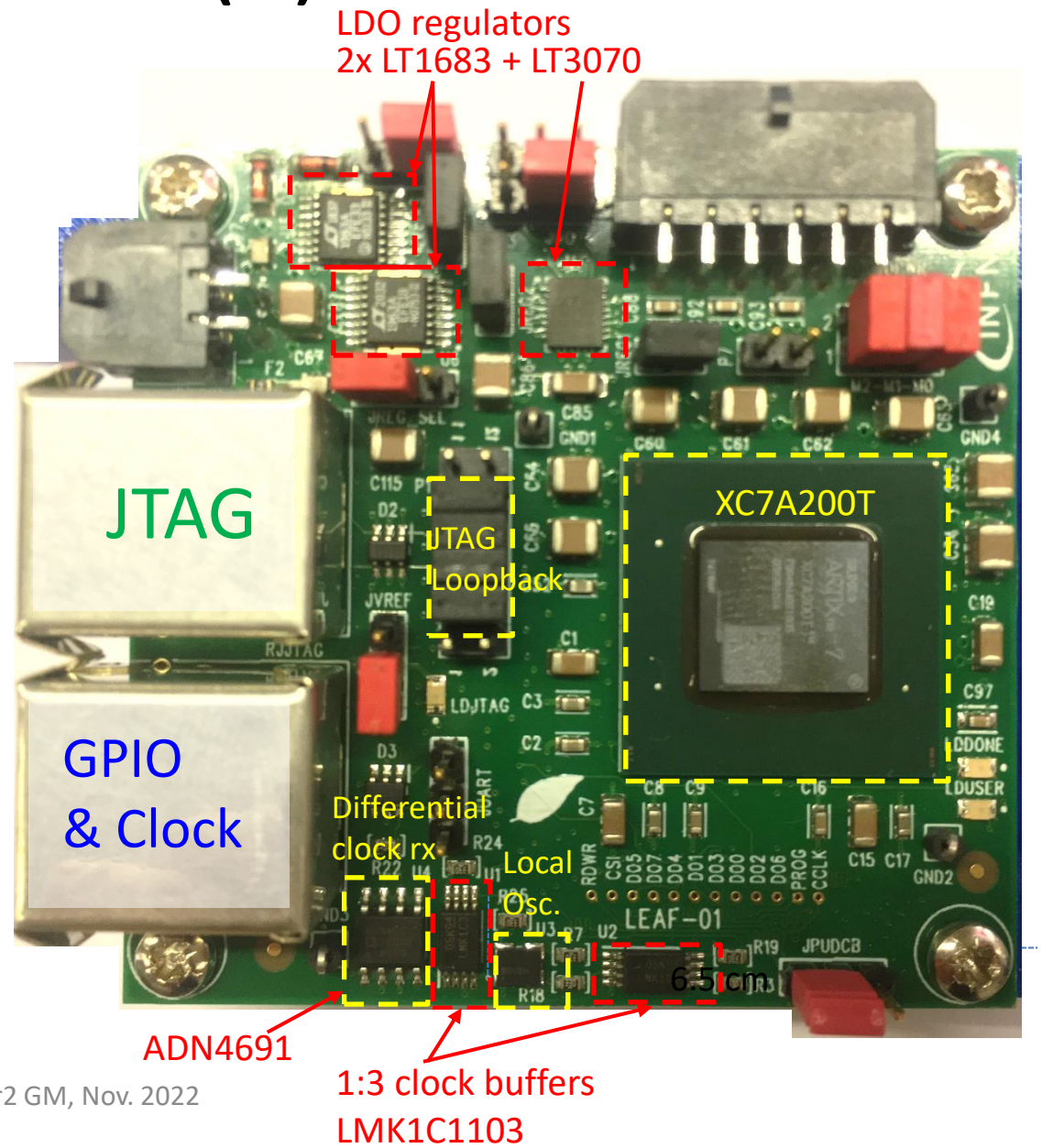


[1] T. Higuchi et al., 2012, doi: 10.1088/1748-0221/7/02/C02022
[2] Y. Yu Nakazawa et al., 2020, doi: 10.1016/j.nima.2019.163247

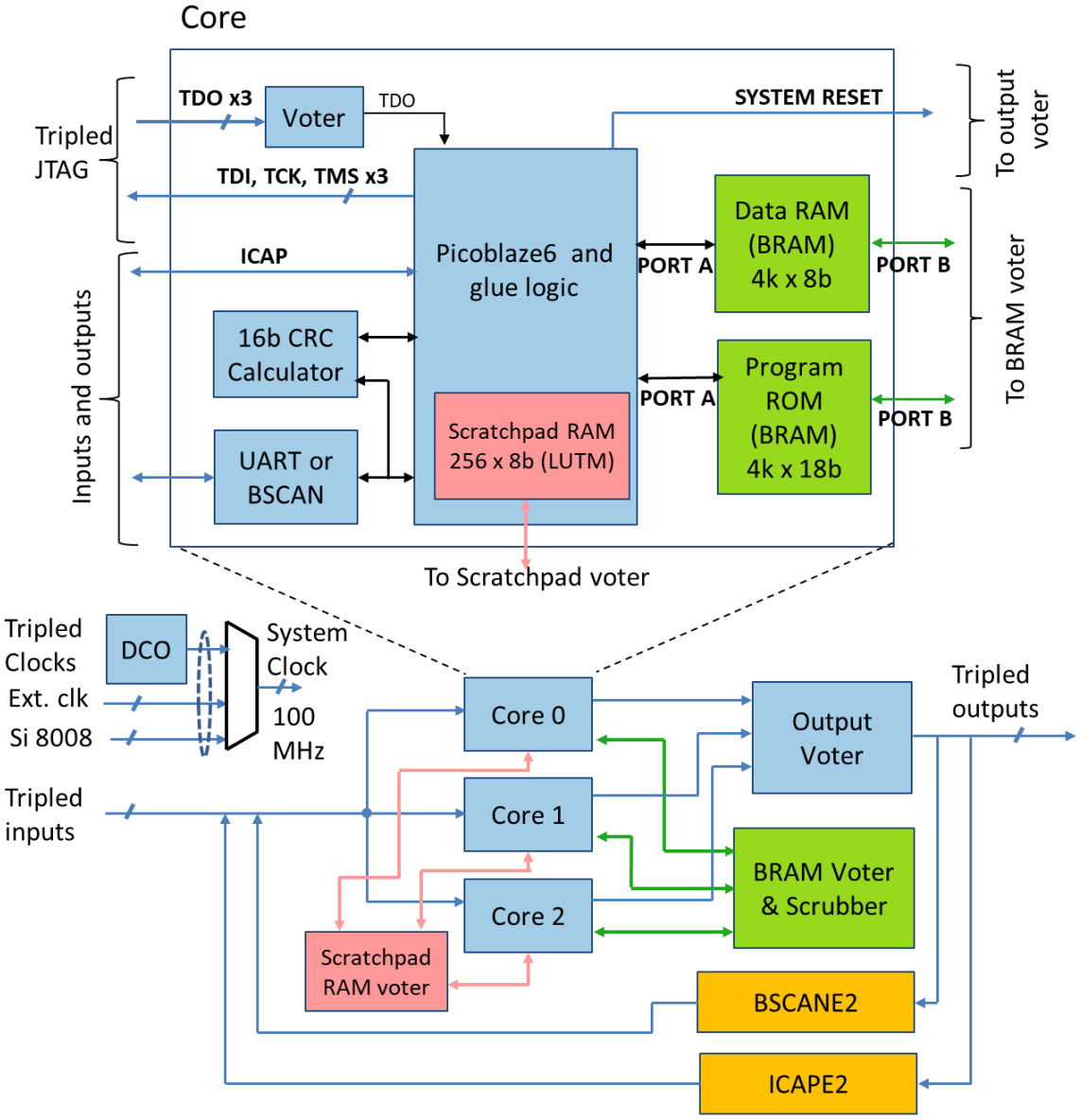
# Sensor Board (2)

- Components: FPGA, power regulators, oscillator, buffers, passives, connectors
- Triple traces for clock, UART, JTAG self-scrubbing (loopback)
- Dual clock input support
  - external and local oscillator (100 MHz)

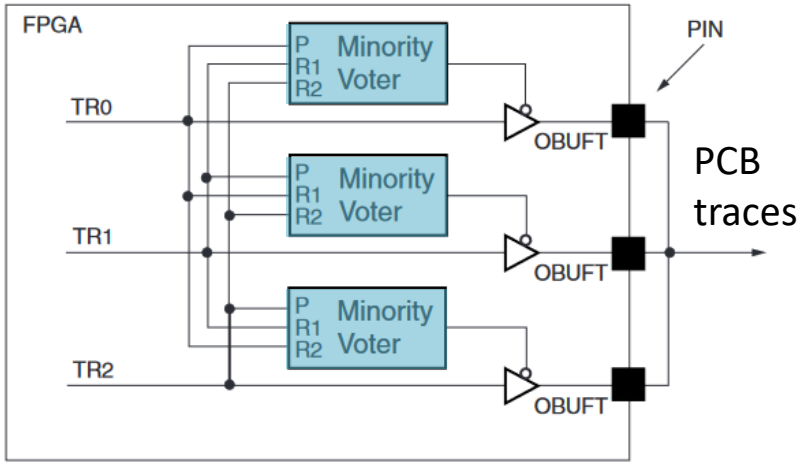


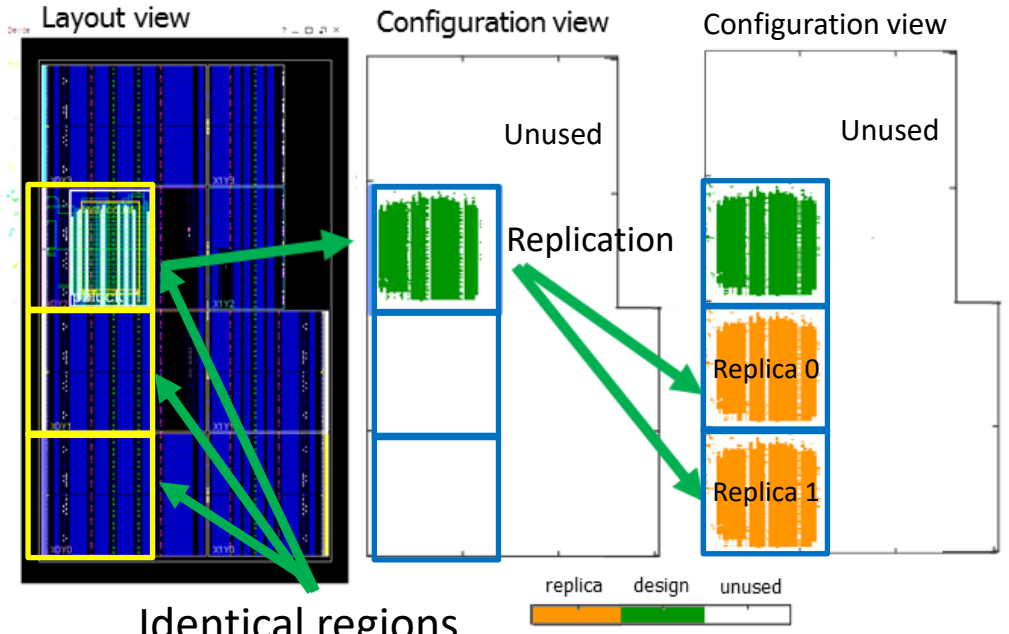
# Readout Logic




- Minimize single point of failures
  - Triple modular redundancy, triple IOs
  - Multiple configuration access ports: on-the-fly switch between ICAP and JTAG
  - Multiple clock sources
  - Majority voting of redundant configuration for firmware self-repair



# Majority Voting Configuration for Self-Repair




1. Generate FPGA bitstream and identify used configuration memory locations (i.e. frames)
2. Replicate used frames and keep track of redundant and remaining empty frames
3. During FPGA operation, **majority vote** redundant frames for error detection and correction and **check** empty frames

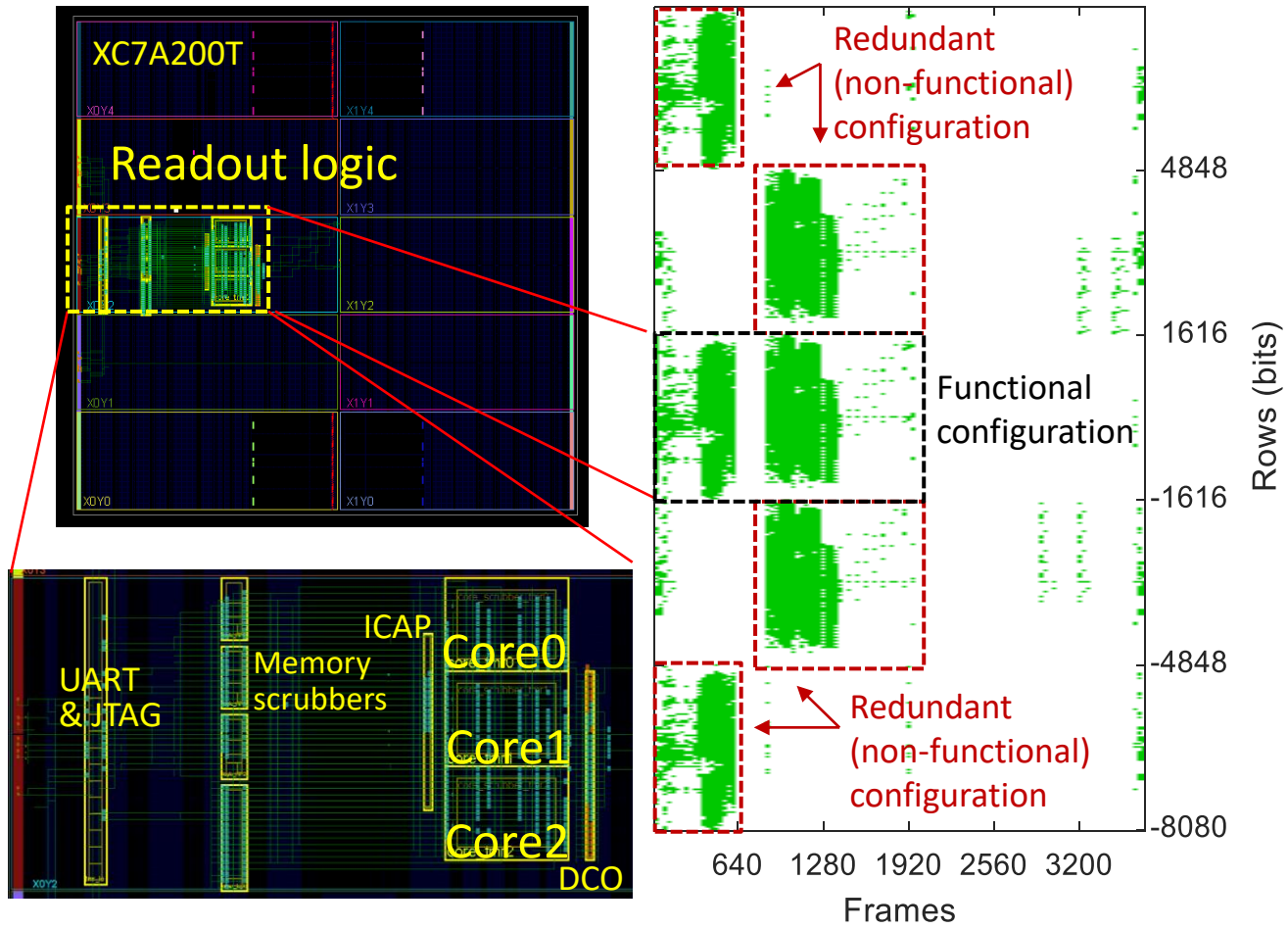

- Can correct all the bits in a frame
  - Assuming no errors in homologous redundant bits (physical separation of redundant copies)
- Based on ICAP, portable on several FPGA families
- No additional power dissipation related to redundant configuration

[1] R. Giordano et al. “Configuration Self-repair in Xilinx FPGAs," in IEEE Trans. on Nucl. Sci., vol. 65, no. 10, pp. 2691-2698, Sept. 2017. **Open Access**
https://ieeexplore.ieee.org/document/8456573

# Layout and Configuration View

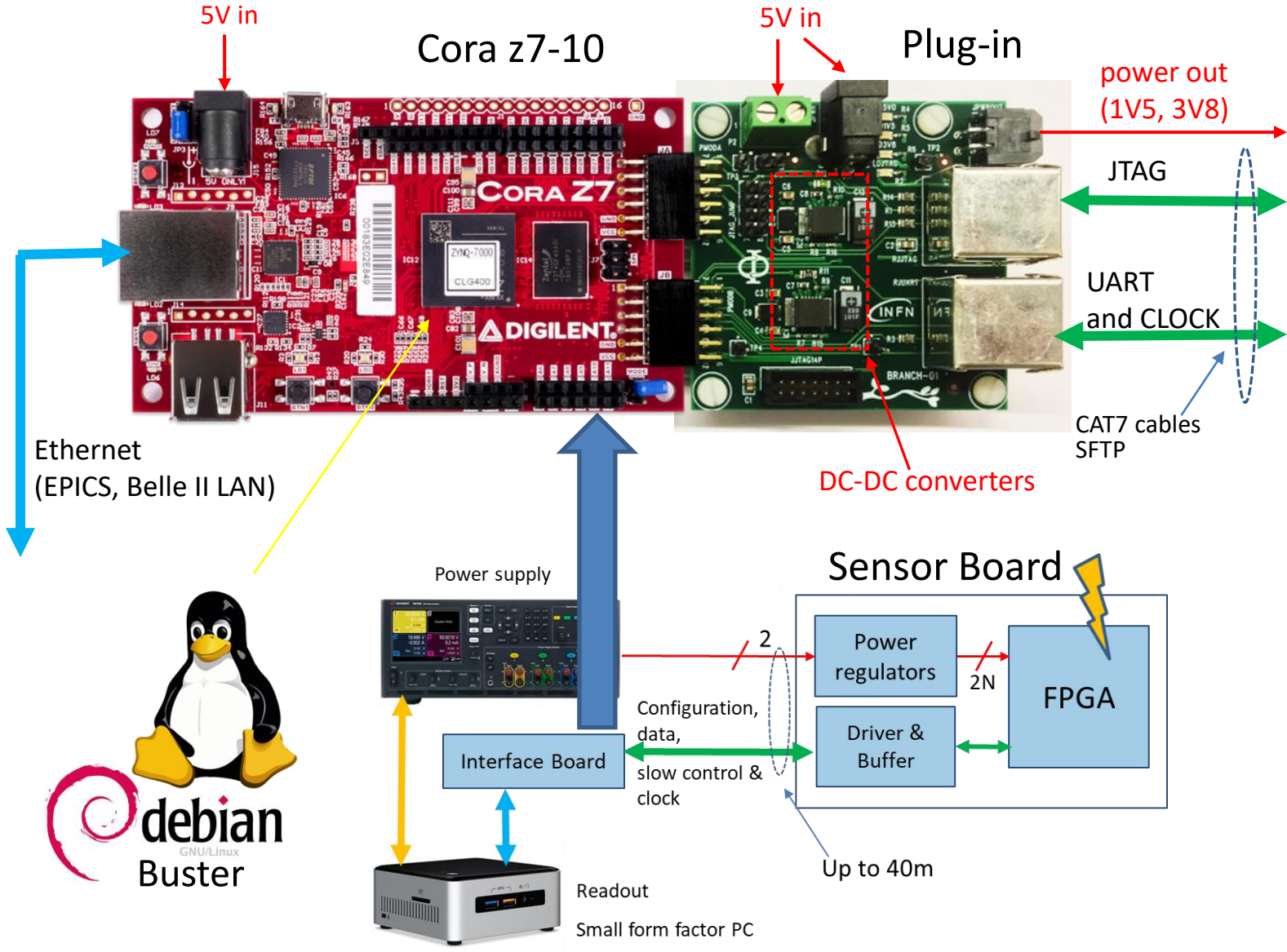
- Redundant modules placed and routed in distinct areas “pblocks”
- Minimal resource utilization (2.5% slices and BRAMs)
- Fully triple redundant configuration [1], CRAM utilization 22.0%
- Full CRAM readout time 1.5s

| Logic Resources | Used | Available | % |
|---|---|---|---|
| Slices: FFs | 1813 | 267600 | 0.7 |
| Slices: LUTs | 2174 | 133800 | 1.6 |
| Slices: overall | 823 | 33450 | 2.5 |
| BRAM 36k | 9 | 365 | 2.5 |
| BUFG | 4 | 32 | 12.5 |
| BSCAN | 1 | 4 | 25.0 |
| ICAP | 1 | 2 | 50.0 |



# Interface Board

- Interface board for configuration and serial readout
  - Digilent Cora z7-10 based on Zynq-7000 (FPGA+ARM uP) + custom plug-in board
- Plug-in board (custom)
  - Provides JTAG, clock, UART to the sensor board
  - Hosts two DC-DC converters for supplying power to the sensor
- Automatic Cable Delay Compensation for fast JTAG over distances up to 40 m

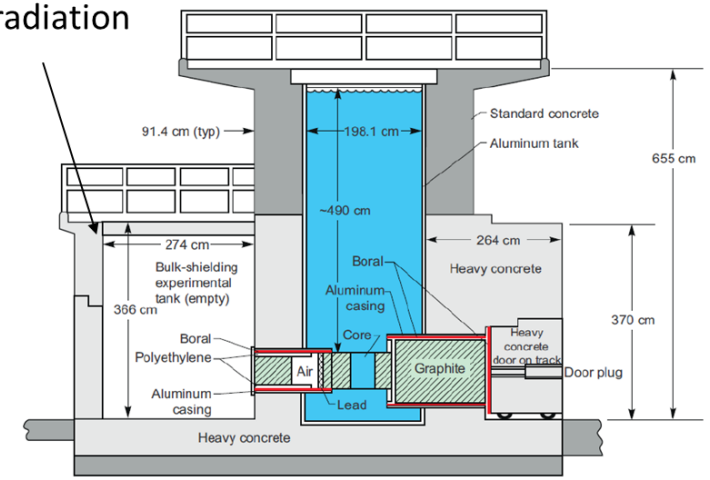


# Radiation Tests Status

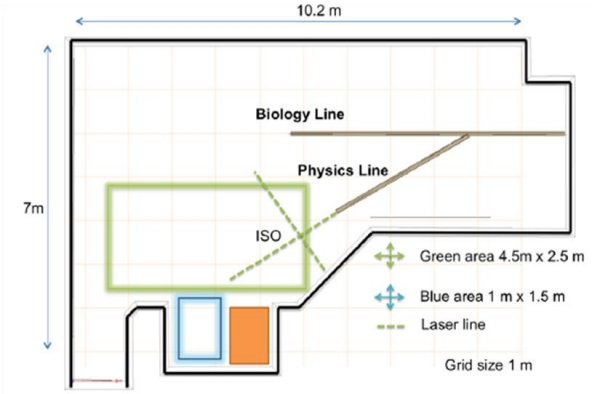
- Radiation tolerance tests at the TRIGA reactor of Jožef Stefan Institute (Ljubljana, Slovenia)
  - Dry chamber for irradiation w/ flux ~ $10^7$ $n_{eq}$/($cm^2$·s) at full power
  - HEP-experiment-like radiation environment (Belle II spectrometer)
  - Results: neutron fluence tolerance > $10^{12}$ $n_{eq}/cm^2$, readout logic failure cross section $5.1 \cdot 10^{-12}$ $cm^2$ (thermal n)
- Measurement of σ(E) at Trento Institute for Fundamental Physics and Applications (Trento, Italy)
  - monoenergetic protons from 70MeV to 226 MeV
  - fluxes from $3 \cdot 10^6$ to $2 \cdot 10^8$ p/($cm^2$·s)
  - Testing in progress, will be completed in Nov-Dec 2022
- Interest of Belle II background community for single-event upset monitoring in on-detector FPGAs [1] and neutron-related background in general

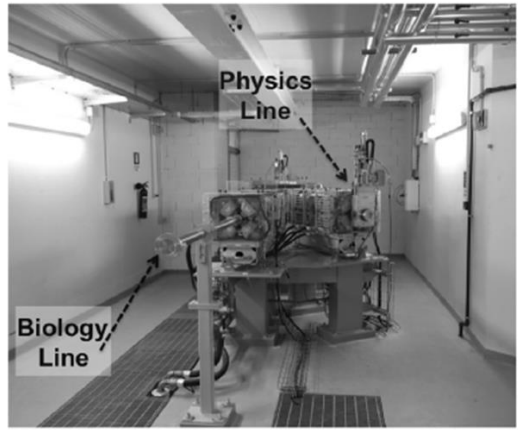
Dry room for irradiation

TRIGA layout




TIFPA Irradiation Room

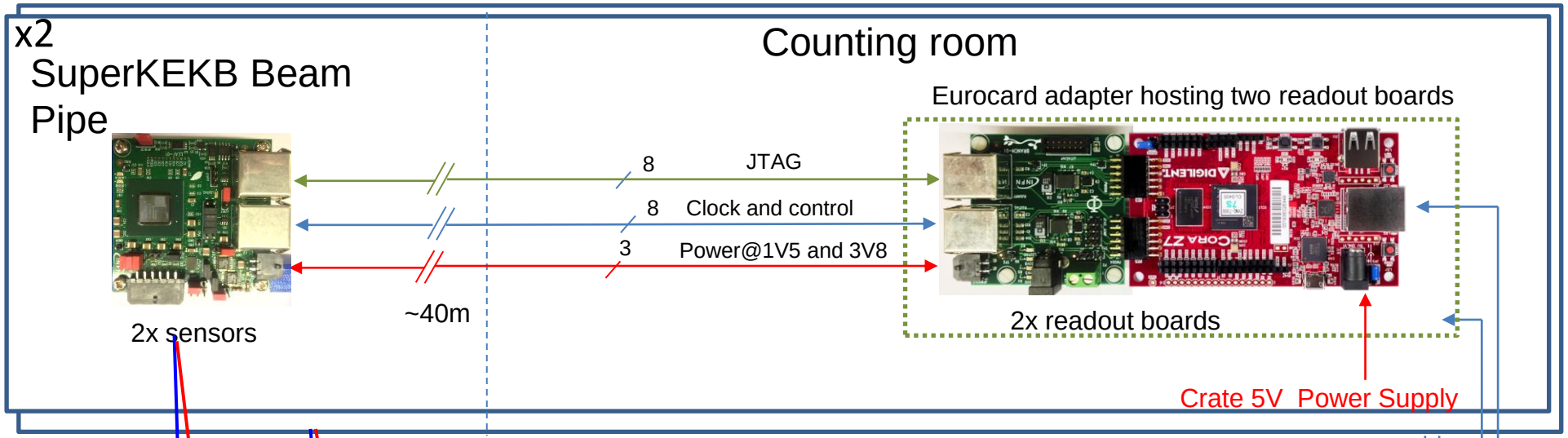


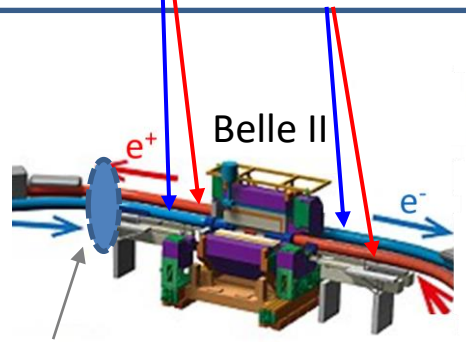




[1] Talk at biweekly beam background meeting

# Hadron Fluence Monitoring at Belle II

- To be installed in 2023
- Overall 4 sensors + 4 readout boards
  - Two at forward (e+/e-) and two at backward (e+/e-)
  - Will replace present FPGA test boards
- EPICS support for integration with other Belle II monitors
- Back-end server at INFN NA for data collection and web publication (Grafana)
- Overall system modularity makes it possible to add more measurement points over time

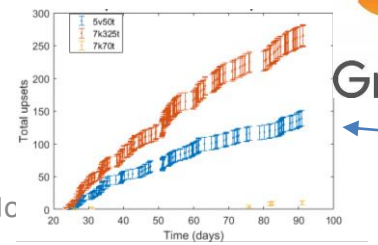





KEK local area network

Internet HTTP


Grafana


DELL PowerEdge R650 @ NA

# Conclusions and…

- Designed a compact, FPGA-based hadron fluence sensor
  - RHBD at PCB and firmware level exportable to other applications of FPGAs in radiation areas
- Interface board
  - Ethernet-enabled JTAG programmer and more!
- Promising results from radiation testing of two sensors
  - Tolerated neutron fluence better than requirements ($>10^{12}$ $n_{eq}/cm^2$)
  - $\sigma(E)$ characterization with proton beams in progress
- Outlook on foreseen readout system at Belle II

# …Acknowledgments


- This research has been funded by INFN in the framework of the PHI experiment (CSNV)
- We wish to thank
  - A. Boiano, A. Vanzanella, A. Pandalone, E. Masone from SER (Electronics and Detectors Service) of INFN Napoli for their technical support to this activity


  - JSI TRIGA staff for their technical support during the irradiation test