Readout system for a GRAIN Demo

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DUNE IT, LNF
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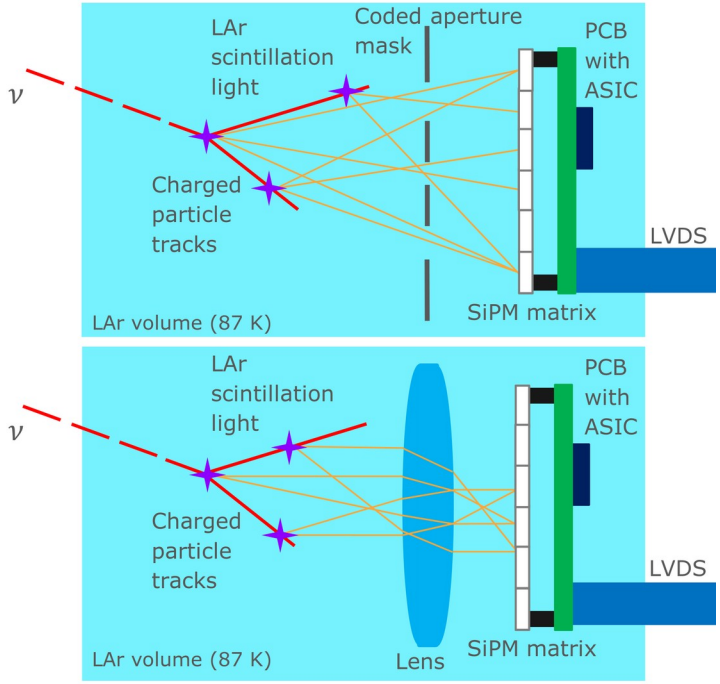
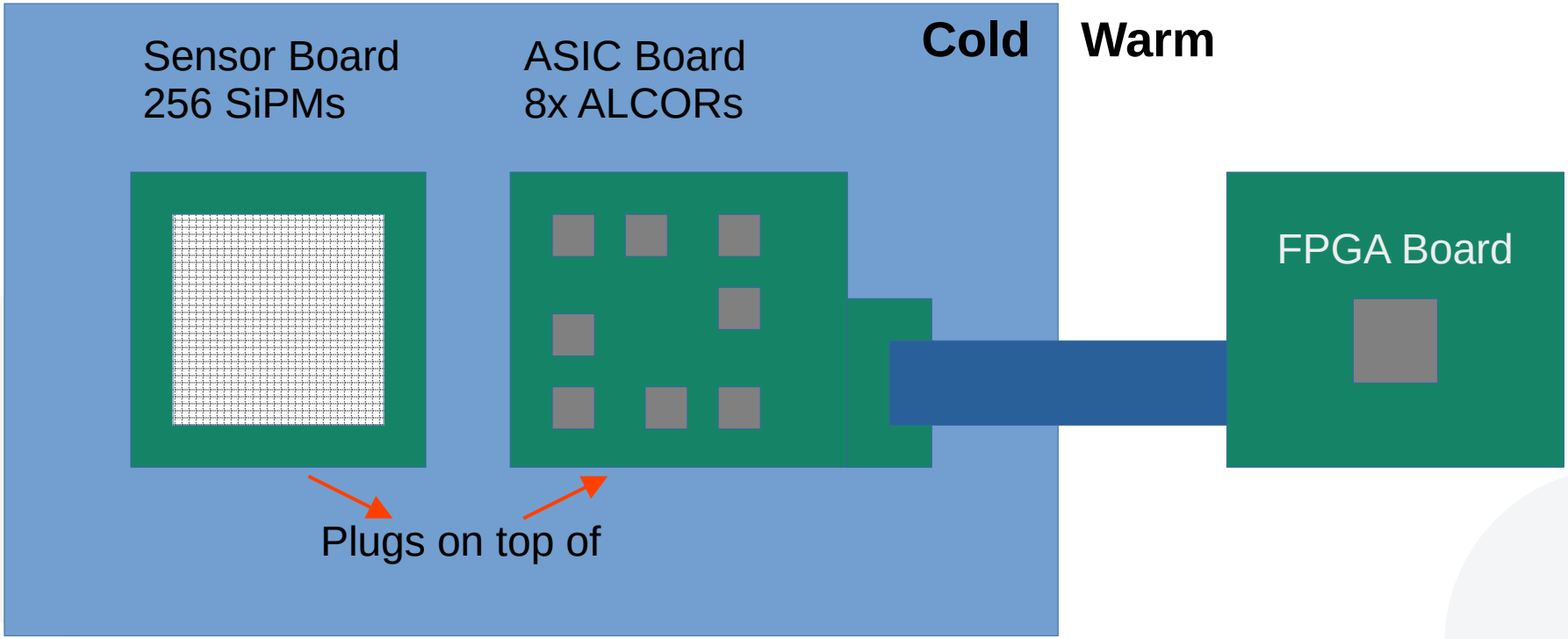
INFN
Istituto Nazionale di Fisica Nucleare

Readout System Overview



- same readout system for masks and lenses
- 256 ch. SiPM camera
- ALCOR cryogenic ASIC

Readout System Overview



Progress from last year

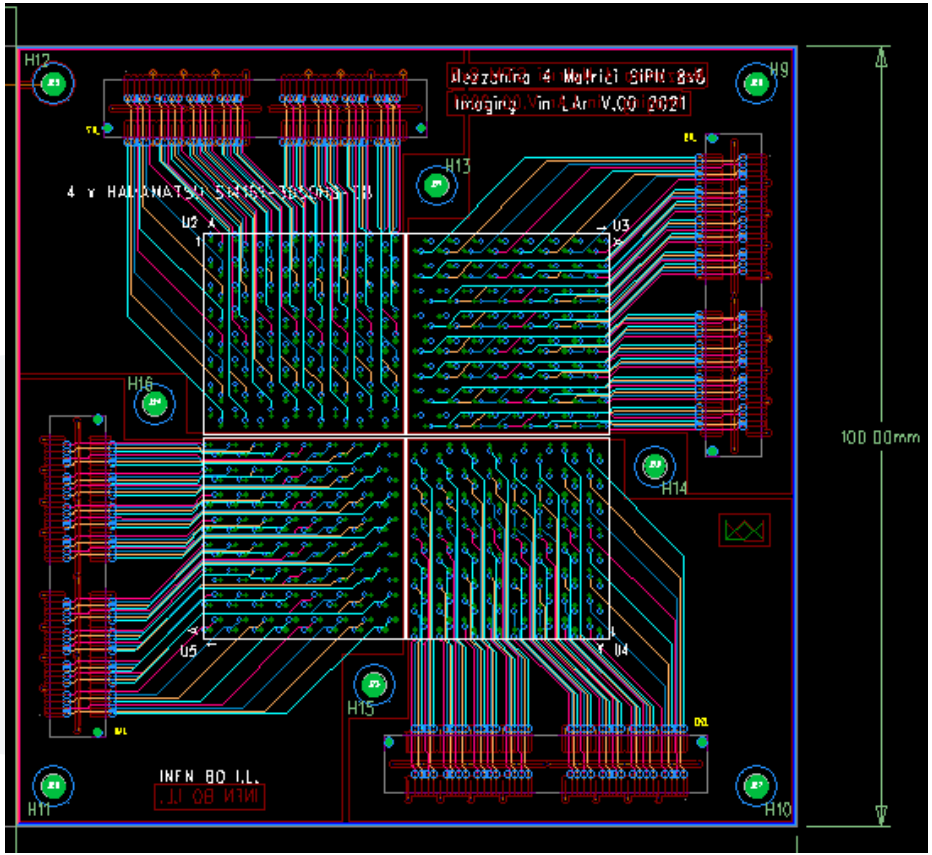
Nov ‘21

- Design of Sensor Board
- Design of ASIC Board
- FPGAs on order

Nov ‘22

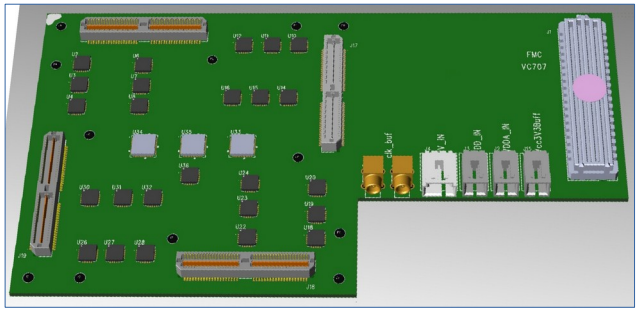
- 8 Sensor boards in hand
  - 4 with 3x3 and 4 with 1x1
- ASIC Board in hand
  - Only one ASIC bonded
- 3 FPGA Boards in hand
  - Seeking an extra

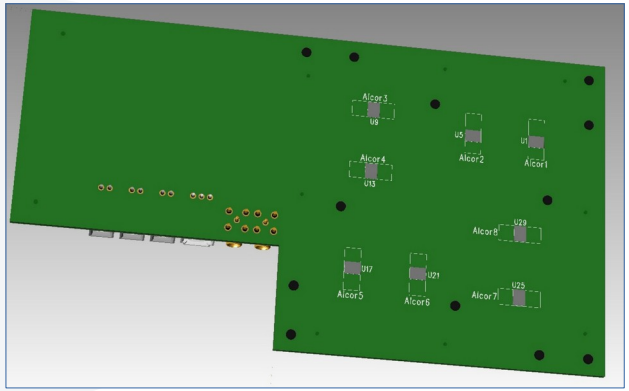
Sensor Board

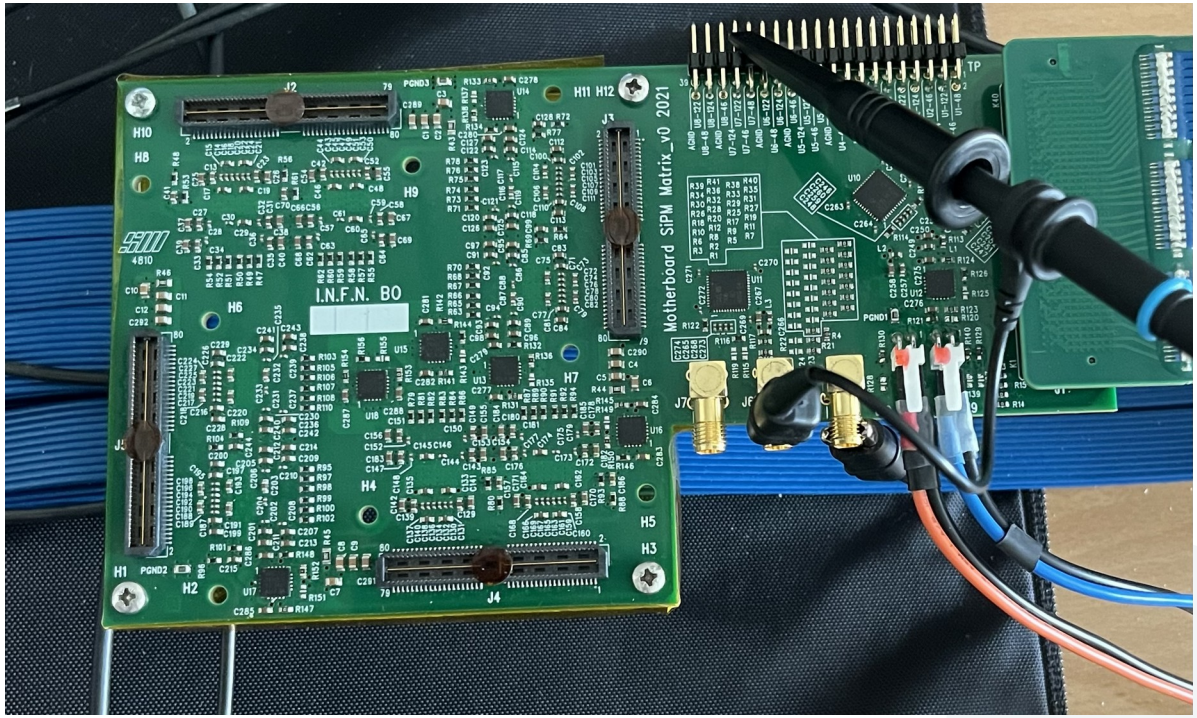


HPK S14161-3050-08

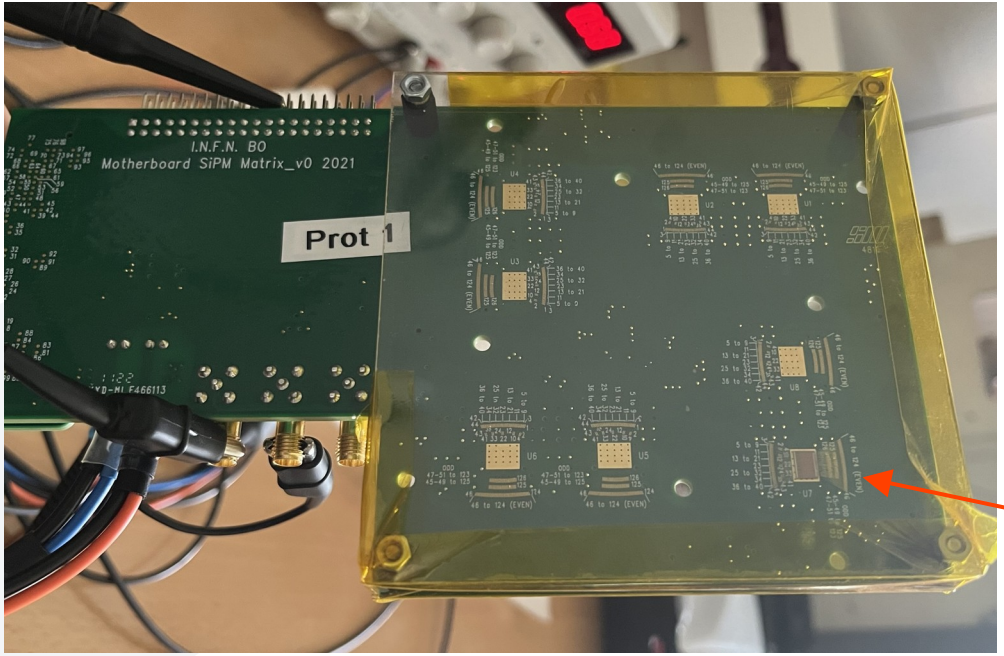
ASIC Board







ASIC Board

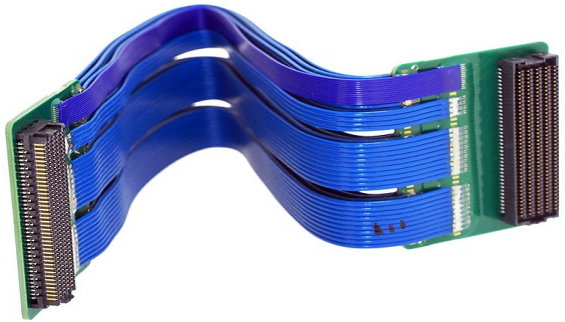


- Board is fully functional
- Auxiliary components working well in LN
  - LV regulators, LVDS buffers
  - No issues with connectors
- One ALCOR bonded

FPGA, Firmware & co.

- Xilinx VC707
  - one per camera
  - oversized, but needed for connectivity
- 1m FMC cable extension procured

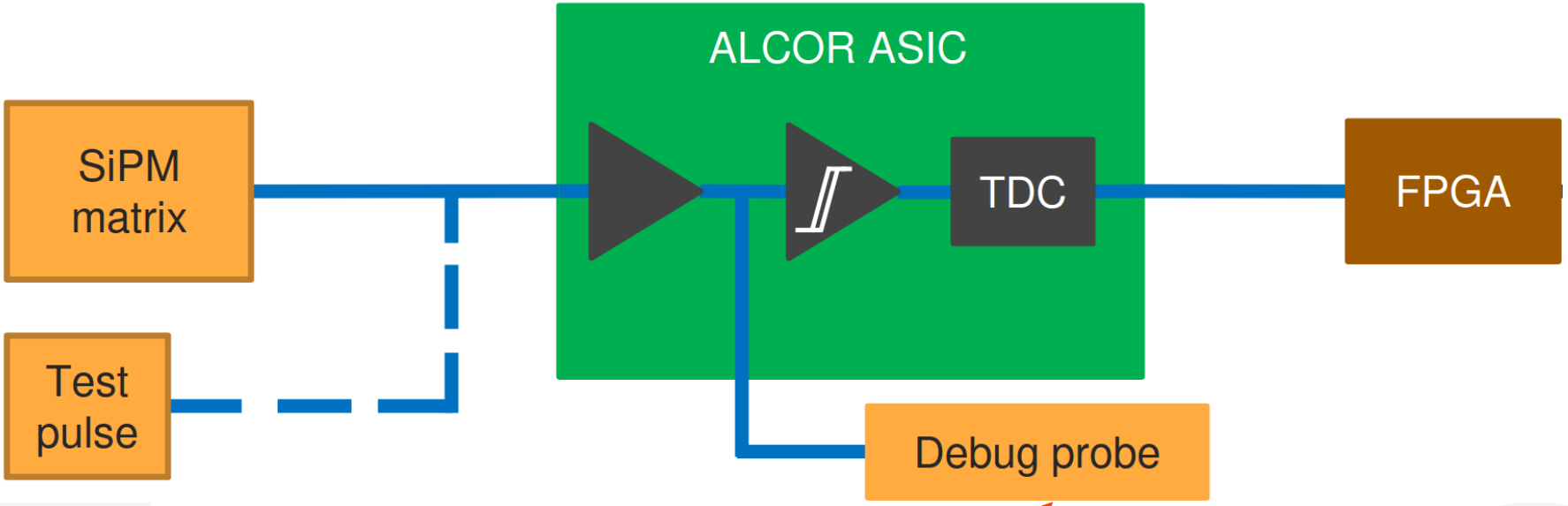
- Firmware and DAQ software in progress
  - Sufficient to talk to ASIC
  - Configuration and readout are working



CRYO Tests

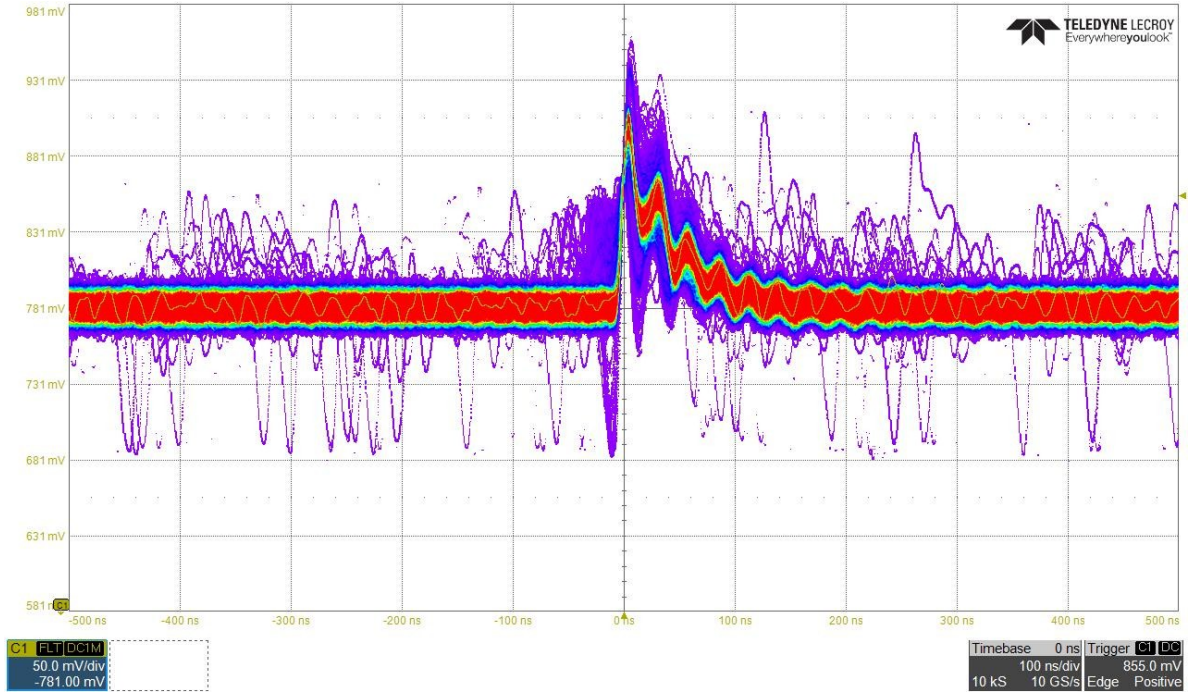
- Non trivial to procede step by step
  - Internal test pulse not working well
  - Complex connectorization
- Whole system tested warm and cold since Sept ‘22.

Test Setup

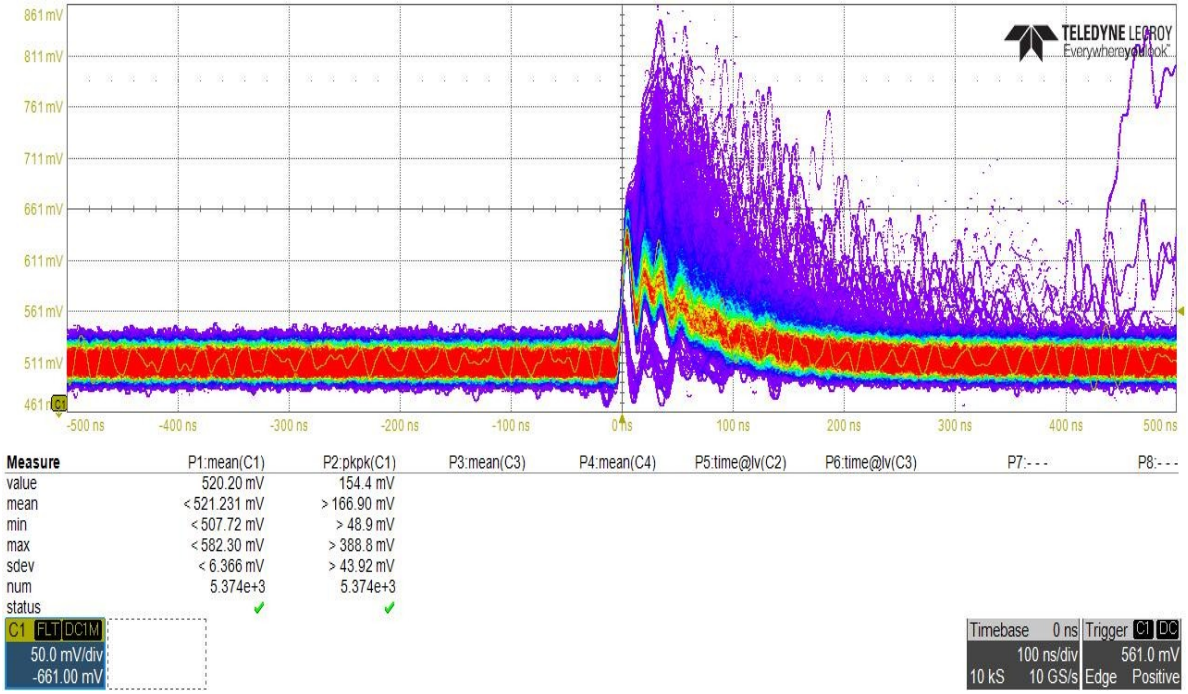


- Next slides show this signal on the scope

Test Results – WARM – 1mm



Test Results – CRYO – 1mm



Result Summary

- All digital functions that were exercised seem **OK**
- Gain **OK**
- Risetime **OK**
- Baseline noise **OK**

- Oscillation at ~30 MHz
  - Likely self induced
- Influenced, but not fully mitigated, with preamp bias current setting

Outlook

- Currently working on reducing this noise, but we may have to live with some of it
- Everything else is on track, ready by end of year
- No significant progress on finding alternative ASICs that meet our needs