Cold electronics and DAPHNE for FD1-HD and FD2-VD

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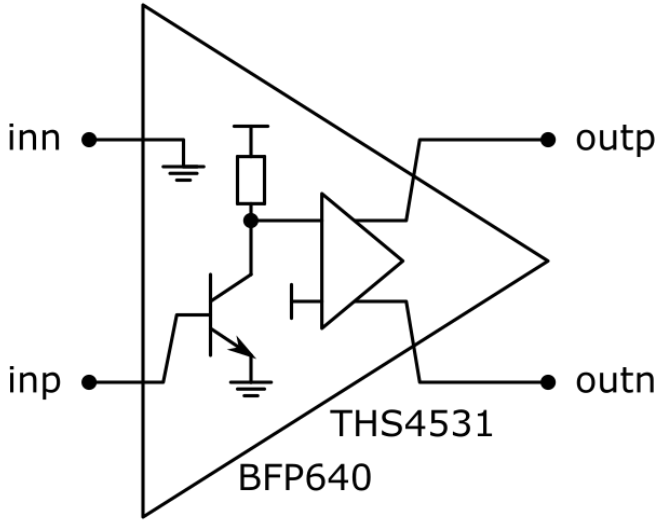
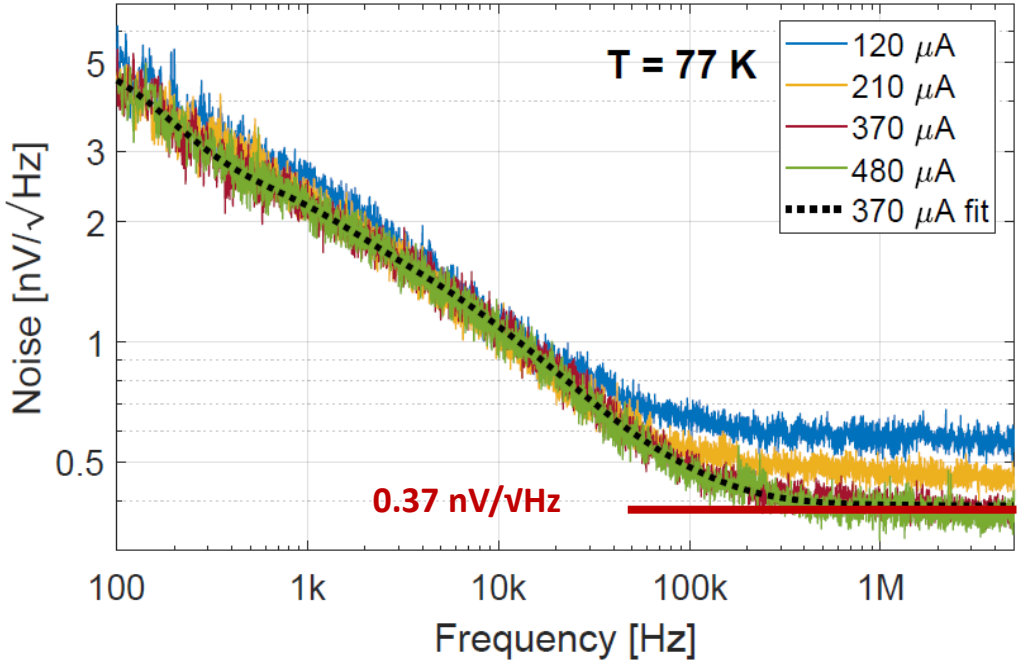
On behalf of the DUNE FD1 PD Photosensors & Electronics WGs

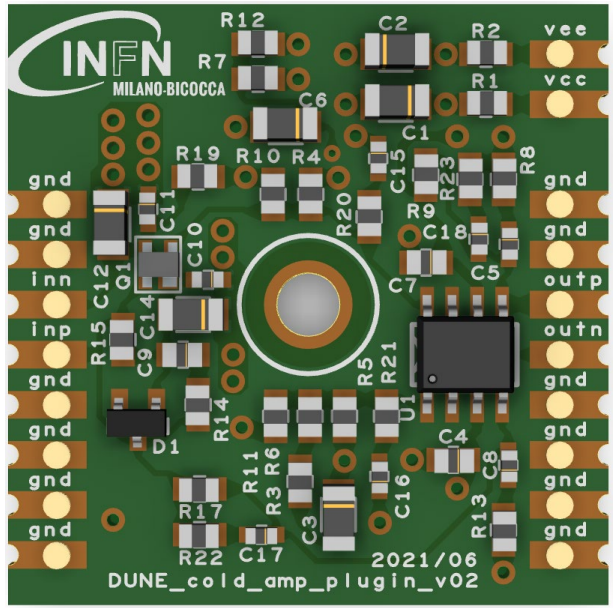
Cold amplifier for FD1-HD (1)

- Pseudo-differential configuration based on discrete commercial components
- **BFP640 SiGe bipolar transistor** for low series noise at low bias current (0.37 nV/√Hz @ Ic=0.4 mA)
- **THS4531 differential opamp** for high loop gain & differential outputs

  → P. Carniti et al 2020 doi:10.1088/1748-0221/15/01/P01008
  → C. Brizzolari et al 2022 arXiv:2207.13616

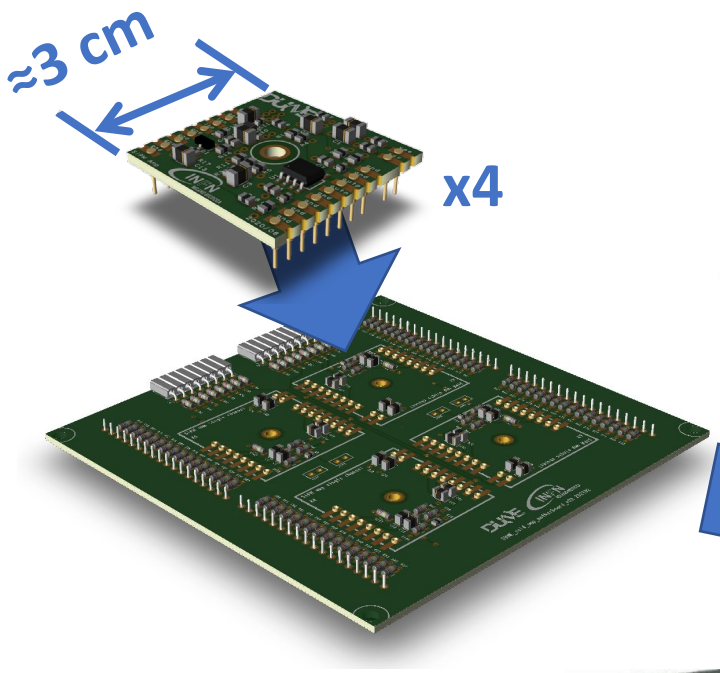


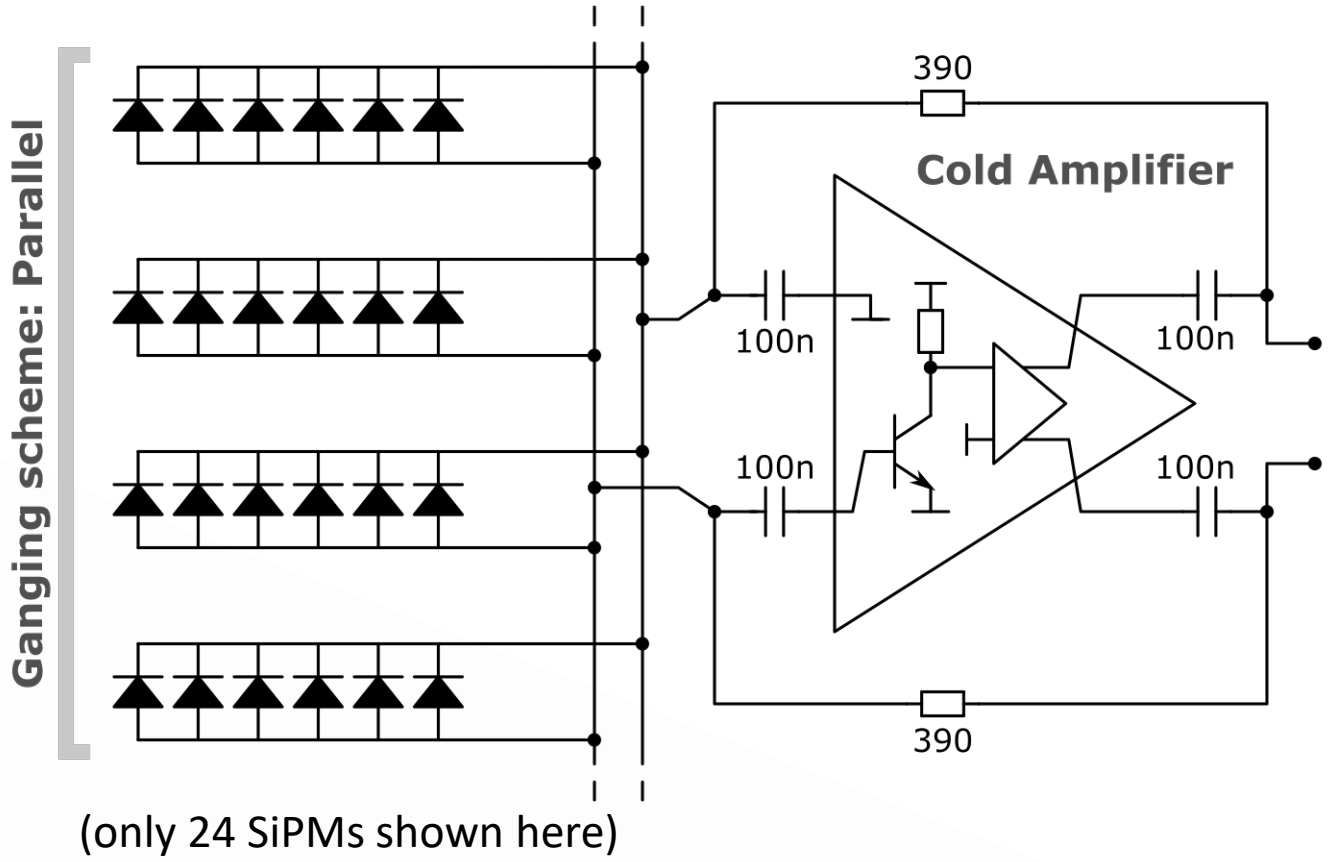




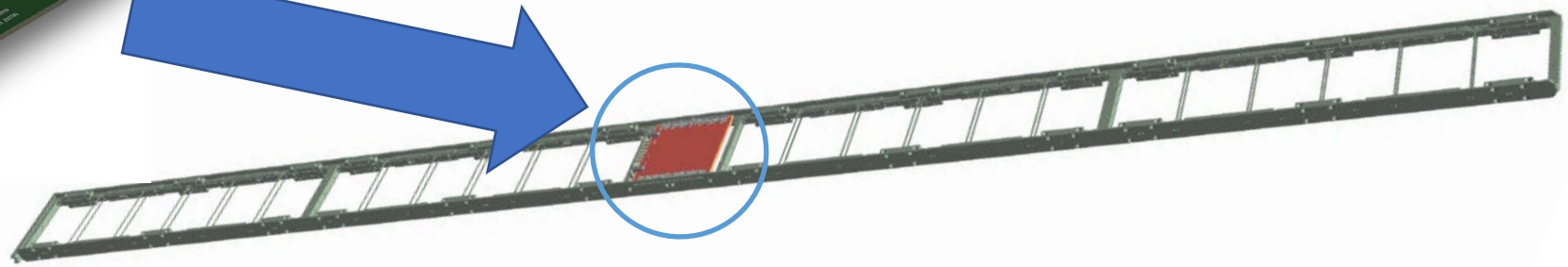
Cold amplifier for FD1-HD (2)

- Dimensions: 3x3 cm^2 (one channel)
- Total power at cold (one channel):
  0.7 mA x 3.3 V ≈ **2.4 mW**
- Max power density **< 1mW/mm²** (1 kW/m^2)
  avoids LAr bubbling





(only 24 SiPMs shown here)

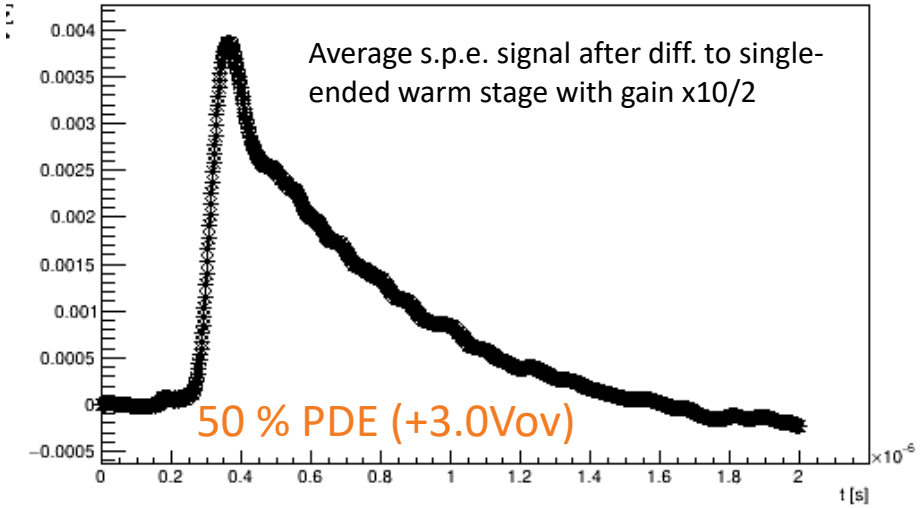


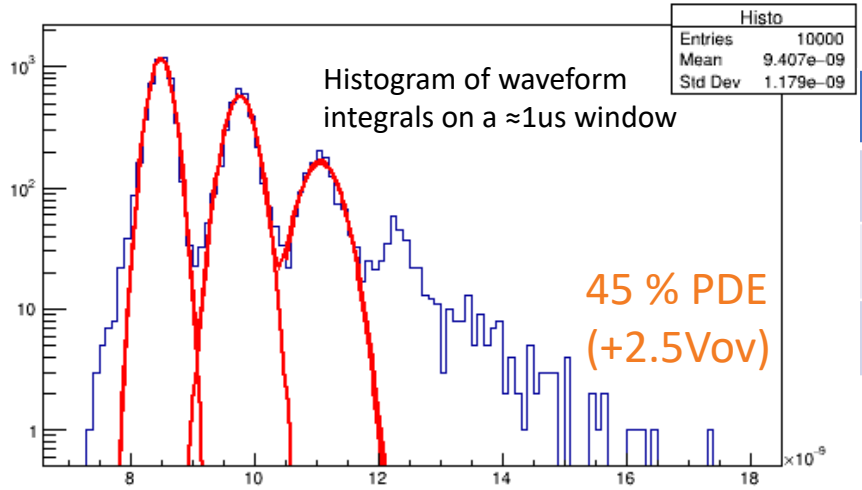
Cold amplifier for FD1-HD (3)

- FD1-HD configuration, 48 SiPMs in parallel

Requirements:
- **≈2000 p.e. dynamic range**
- **<100 ns signal rise time**
- **S/N>4**

Hamamatsu 75um HRQ



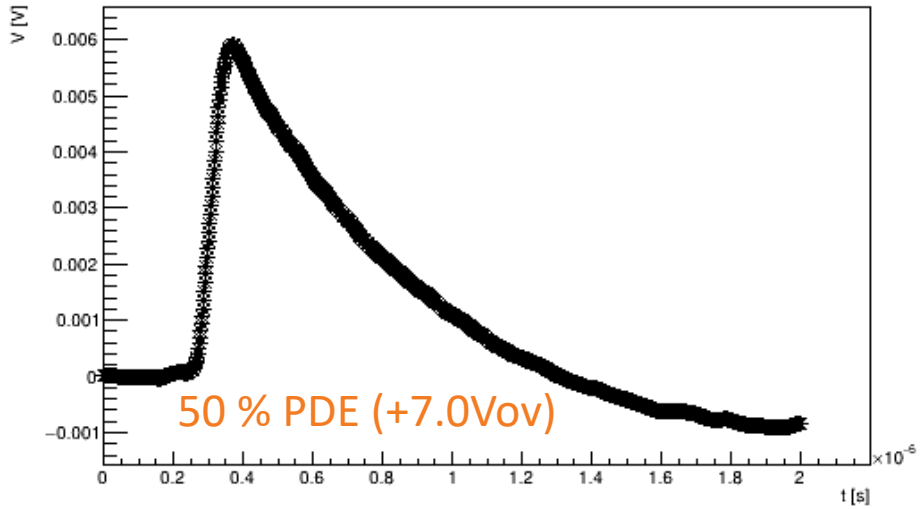


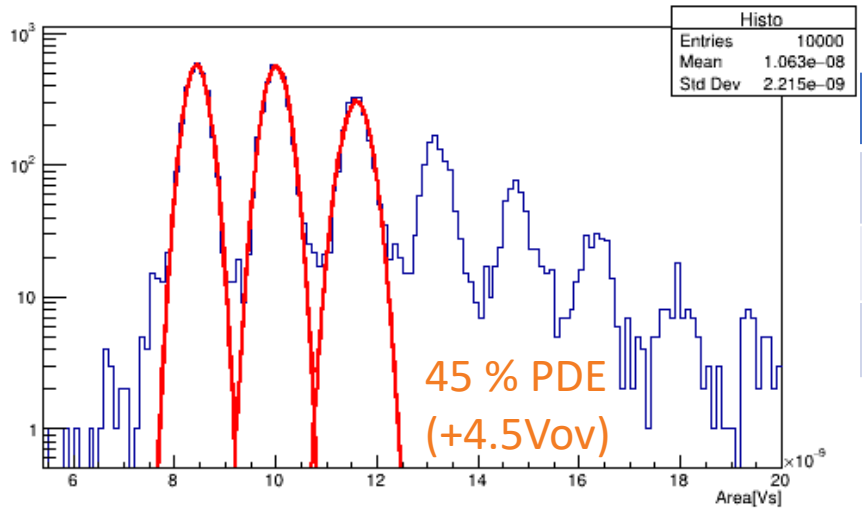
Dynamic range before saturation of the opamp output stage on 100-ohm diff. load

PDE	Vov	DR (p.e.)	S/N
40%	2.0	≈2900	6.30
45%	2.5	≈2350	7.49
50%	3.0	≈2000	8.92

Single p.e. gain divided by sigma of the baseline

FBK 50um TT

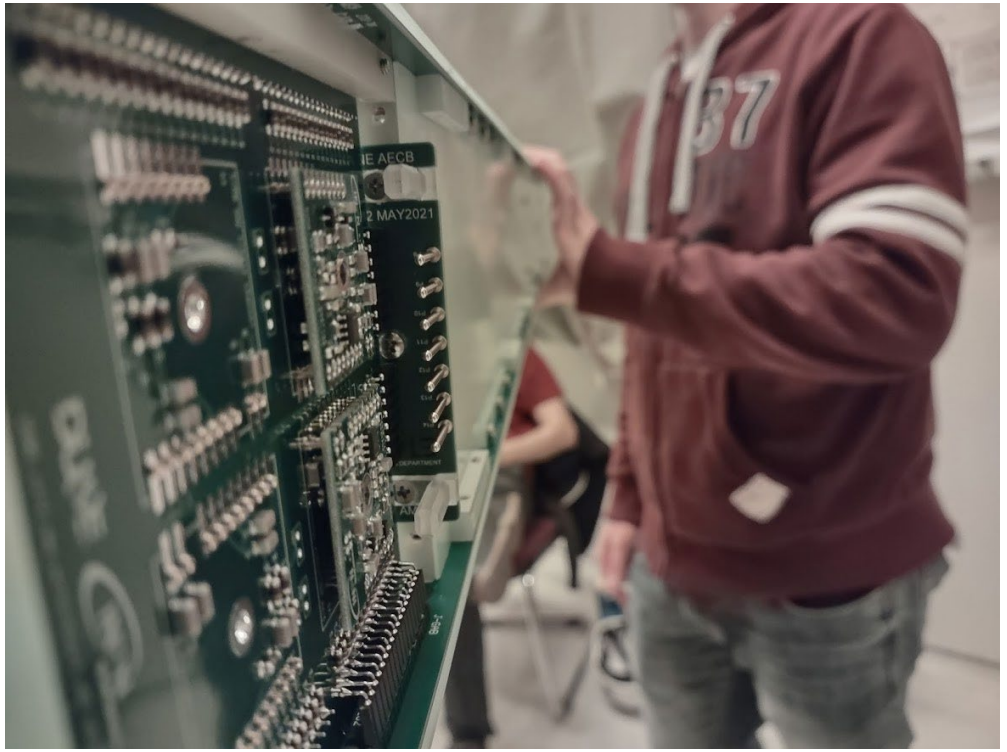




PDE	Vov	DR (p.e.)	S/N
40%	3.5	≈2500	5.64
45%	4.5	≈2000	7.56
50%	7.0	≈1250	11.32

Cold amplifier for FD1-HD (4)

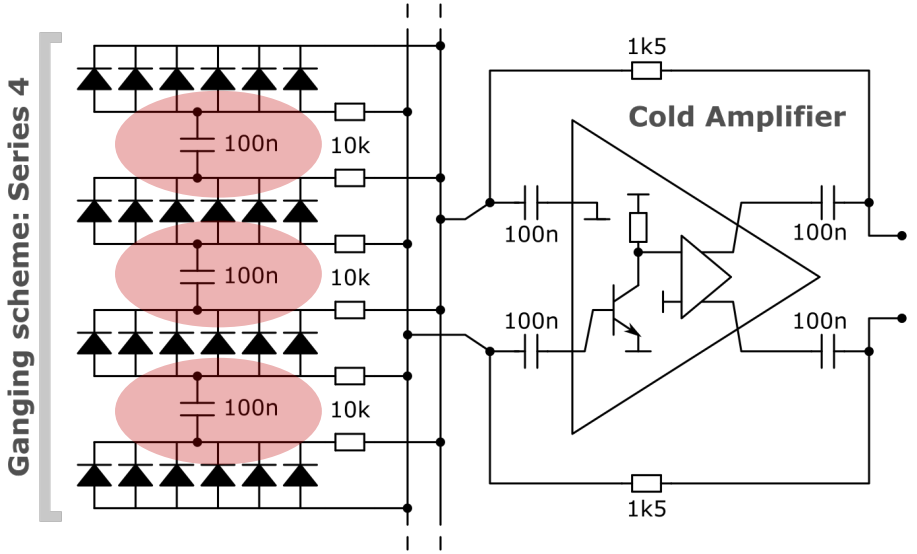
- Design tested in several labs and used for all supercell tests
- 160 chanels produced and installed in ProtoDUNE2
- Possible change for DUNE: 4 channels on one PCB instead of 4x single channel plugins on a motherboard (simpler and lower cost, although less flexible)

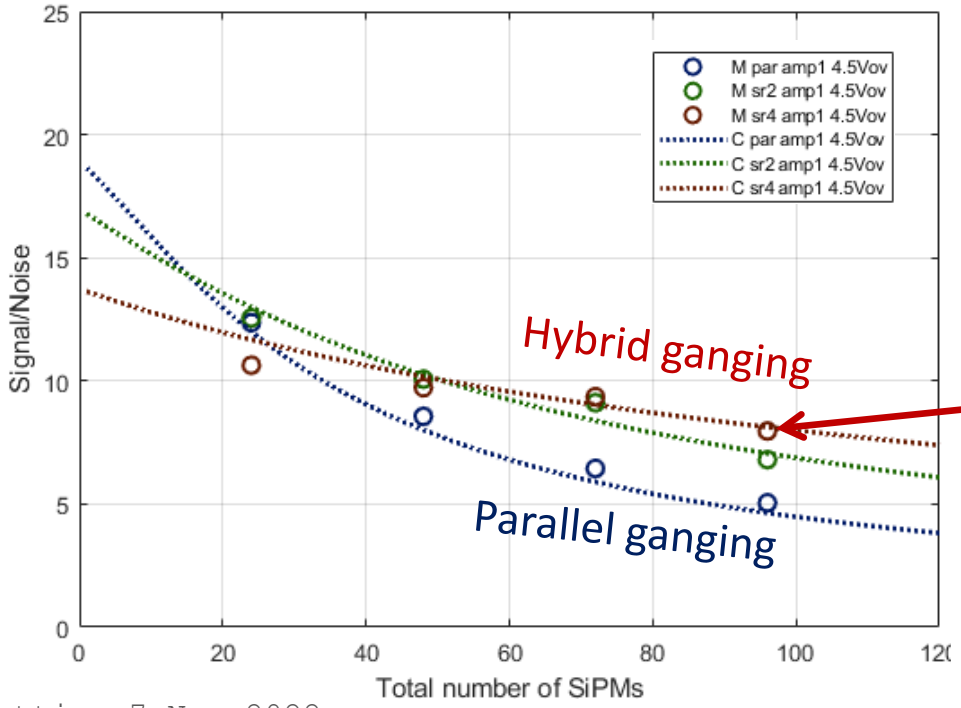


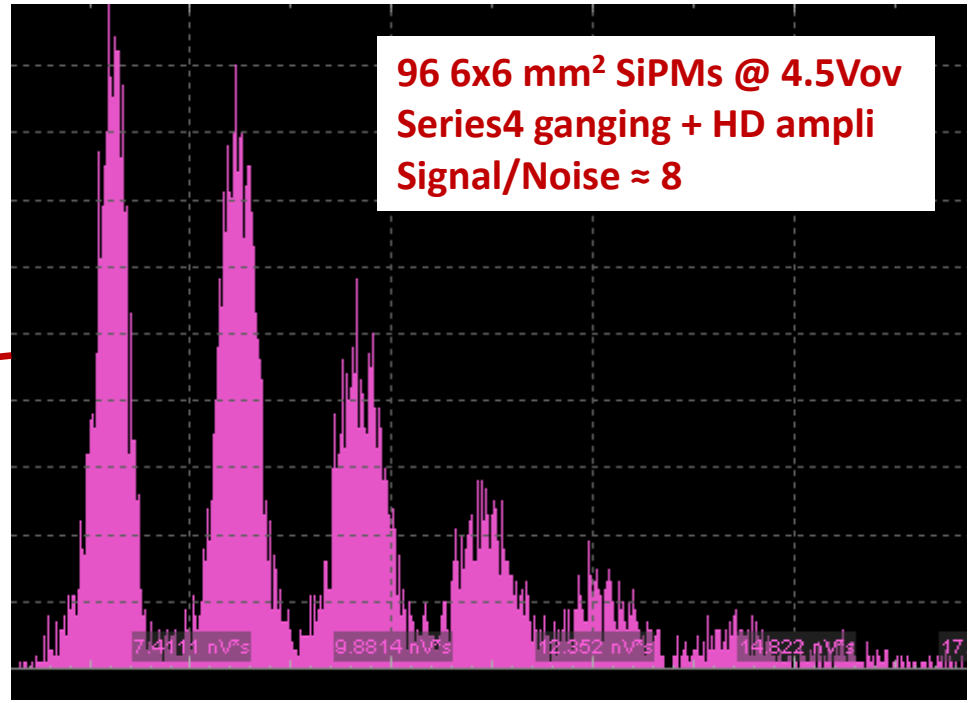
Cold amplifier for FD2-VD

- HD amplifier tested reading out up to 96 SiPMs (with HD SiPM boards)
  - S/N = 5 with 96 SiPMs in parallel
  - S/N = 8 in hybrid ganging (combination of parallel / AC series)
- Tests with VD flex SiPM boards to happen ≈next week
- Plan to readout ≈4 membrane ARAPUCAs (8 channels, 80 SiPMs each) in ProtoDUNE-VD
- Tests with the full «cathode» setup (PoF, SoF, DCDC, …) also planned

Hybrid ganging

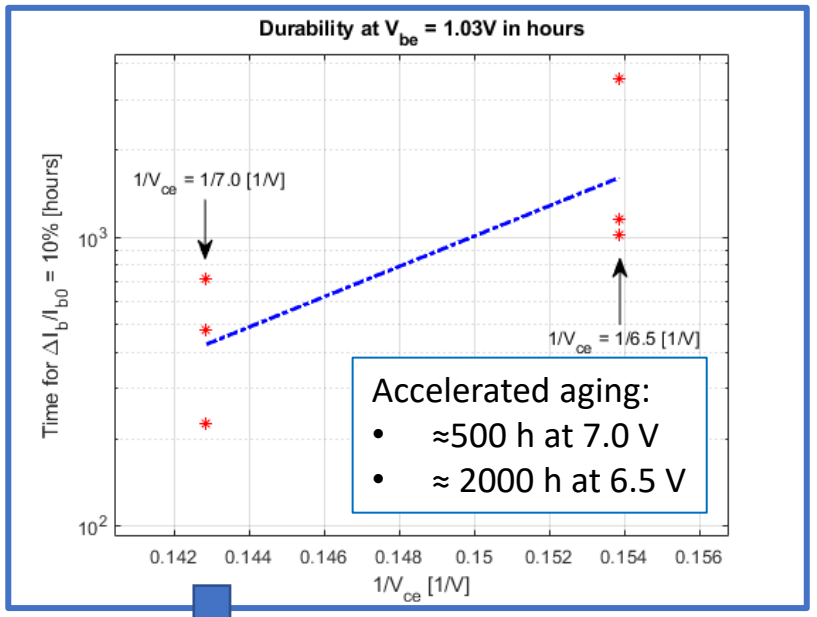






Lifetime of components at cryo T

- At cryogenic temperature, increased carrier mobility can enhance degradation due to **hot carrier effects** (HCE)
- Aging accelerated by operation at high voltage (above max rating)
  → Li et al IEEE TNS doi:10.1109/TNS.2013.2287156
  → Cressler, Mantooth, *Extreme Environment Electronics* ISBN 9781138074224

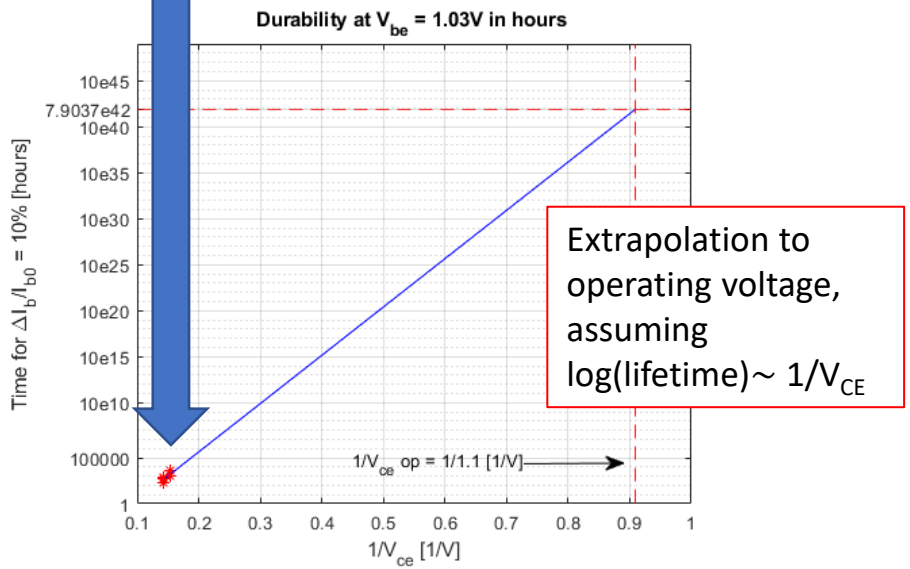


BFP640 SiGe transistor

- Maximum datasheet values (room T): V_{CE}=4.1 V, I_C=50 mA
- Operated at V_{CE}=1.1 V, I_C=0.4 mA → Ample margin
- Stressed up to V_{CE}=7.0 V
- Degradation criterion: 10% increase in base current (decrease in beta)
- Lifetime at the operating point extrapolated to very high values

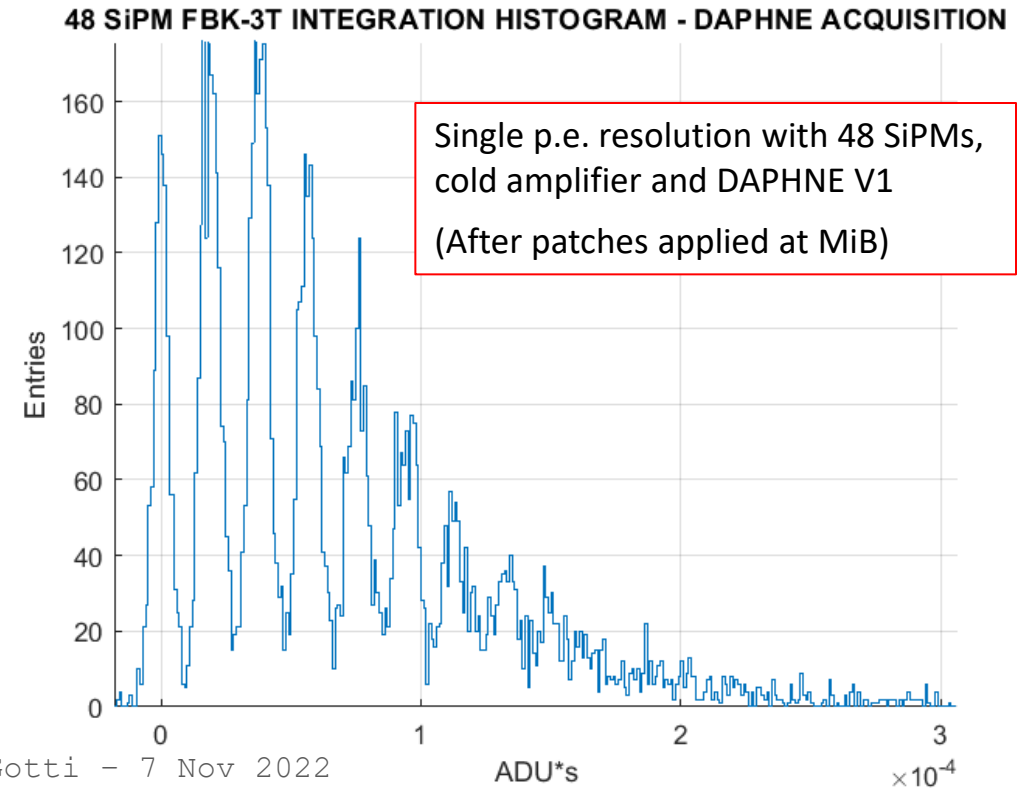
THS4531 fully differential opamp

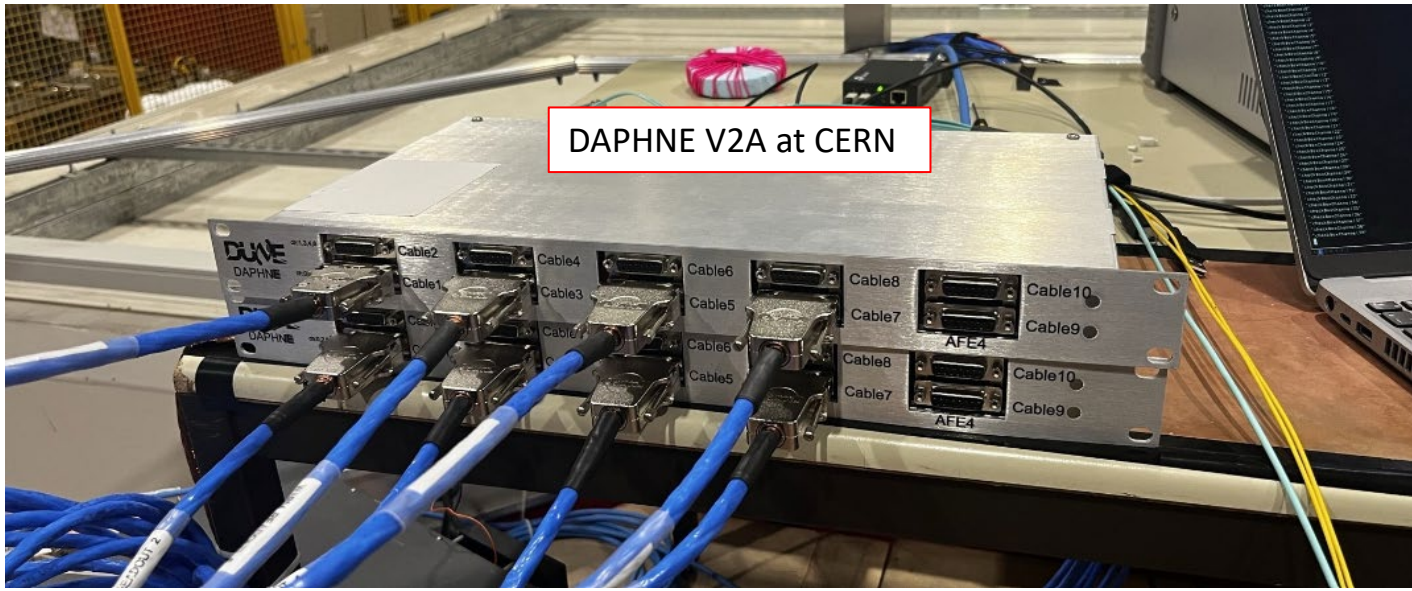
- Maximum datasheet values (room T): V_S = 5.5 V
- Operated at V_S = 3.3 V → Ample margin
- Stressed for HCE up to V_S=8.0 V
- Preliminary results at **INFN LNS (P. Litrico et al)** indicate very long lifetime



DAPHNE for FD1-HD

- 40-channel warm digitizer board developed by Fermilab and several institutions in Latin America (Colombia, Paraguay, Peru)
- Version 1 available since ≈ end of 2021, extensively tested in different labs
- Firmware in advanced state of development, integration with DAQ in progress at CERN
- Analog performance thoroughly characterized at MiB (**E. Cristaldo**), led to revised version DAPHNE V2A
- DAPHNE V2A produced (10 boards), currently under test at CERN and soon to be received at MiB and other labs





DAPHNE for FD2-VD

- A modified version of DAPHNE is planned to be used in the VD
- All «back-end» (digitization, trigger, interface with DAQ, data transmission, …) can probably be reused without changes
- The «front-end» (signal conditioning before digitization) must be adapted
  - For cathode tiles, the SoF optical receiver needs to be added at the input
  - For membrane tiles, changes can be tested to remove/reduce signal undershoot related with differential to single-ended conversion (currently done with a LAN transformer)