Institut de Física d'Altes Energies

Barcelona Institute of Science and Technology

PSD trigger & readout electronics: proposal for discussion

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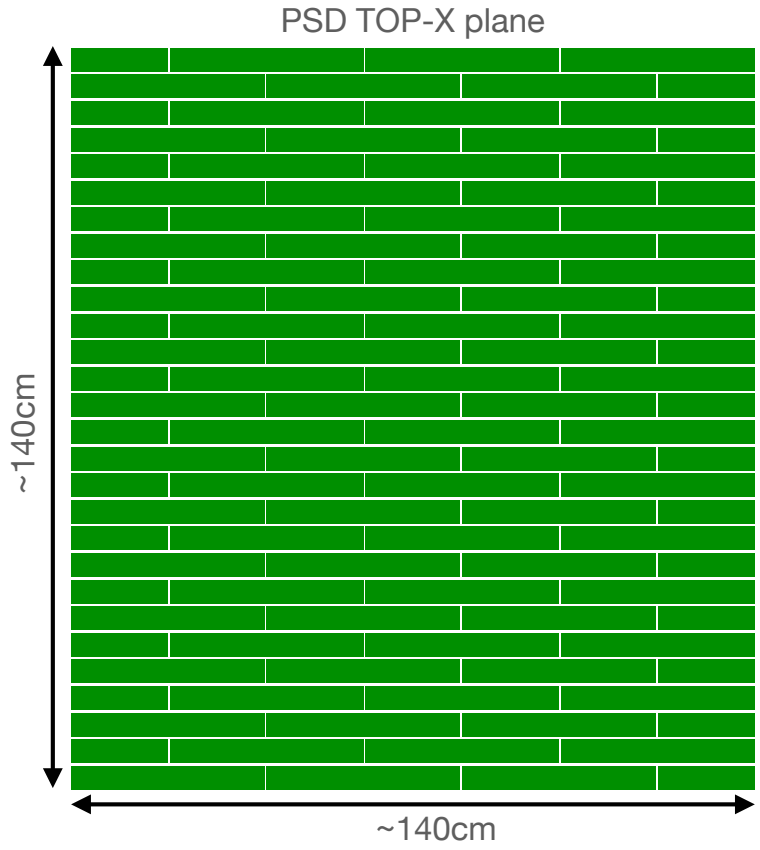
PSD trigger/readout electronics

- Requirements:
  - Provide I/O communication with the BETA chip (configuration, DAQ, trigger, …)
  - Issue veto when a majority of channels of any PSD bar are producing L0 trigger [2/4? 3/4? 2/3?]
  - The PSD trigger/veto should be produced within a latency of ~20 ns, as for FIT
  - ID of the triggering PSD region of interest (RoI) should also be broadcasted (for ULEG trigger)
- Plan:
  - Design and start producing an Electrical and Functional Model (EFM) of the system
  - In parallel, build a prototype (evaluation board) emulating the system architecture for early identification of problems and participation in next beam tests

PSD current [evolving] design

- 5 sectors
- 2 planes per sector with orthogonal orientation of the PSD [short] bars arranged like in a parquet
- Assumed plane dimensions (from geometry in HerdSoftware):
  - TOP: 140cm × 140cm
  - LAT: 130cm × 90cm
- Assumed bar dimensions (from presentation by F. Gargano May 2022):
  - 40cm×5cm
- Each bar read by 3/**4** SiPMs
- Each SiPM read by one BETA16-R2 channel (R2 version needed for providing individual L0 trigger per channel)

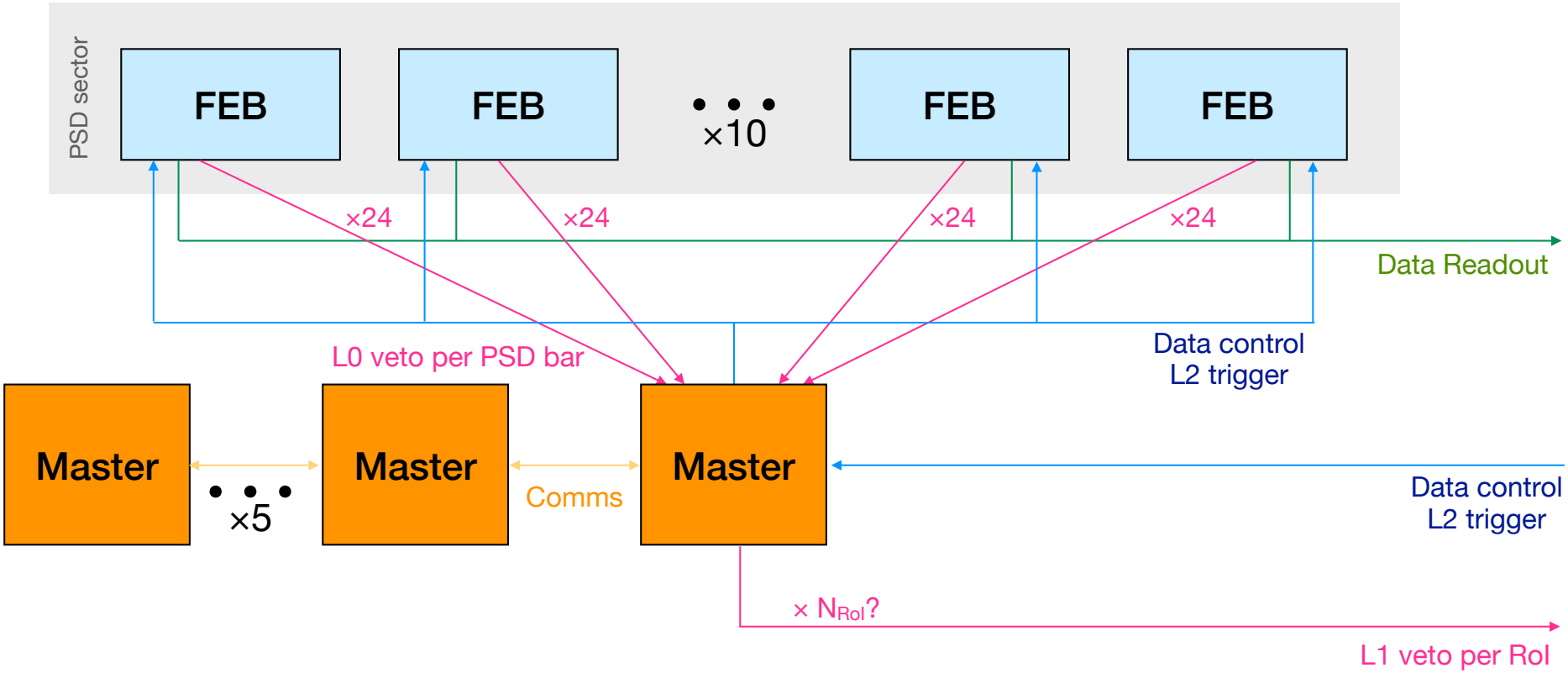


Statistics

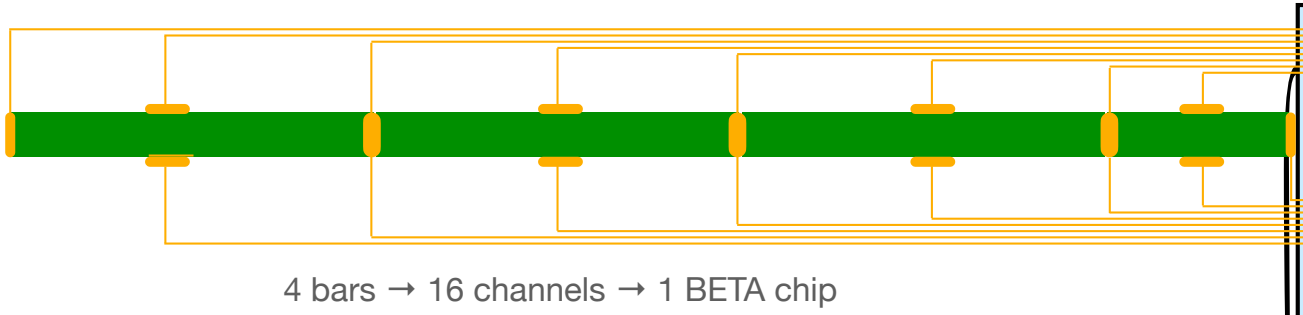
Sector/Plane	# bars	# SiPM	# BETA	# FEB boards	# Master boards
TOP X/Y	28×3.5=112	448	28	5	0.5
LAT H	26×2.25=78	312	20	4	0.5
LAT V	18×3.25=72	288	18	3	0.5
Total [X+Y+4*(V+H)]	824	3296	208	38	5

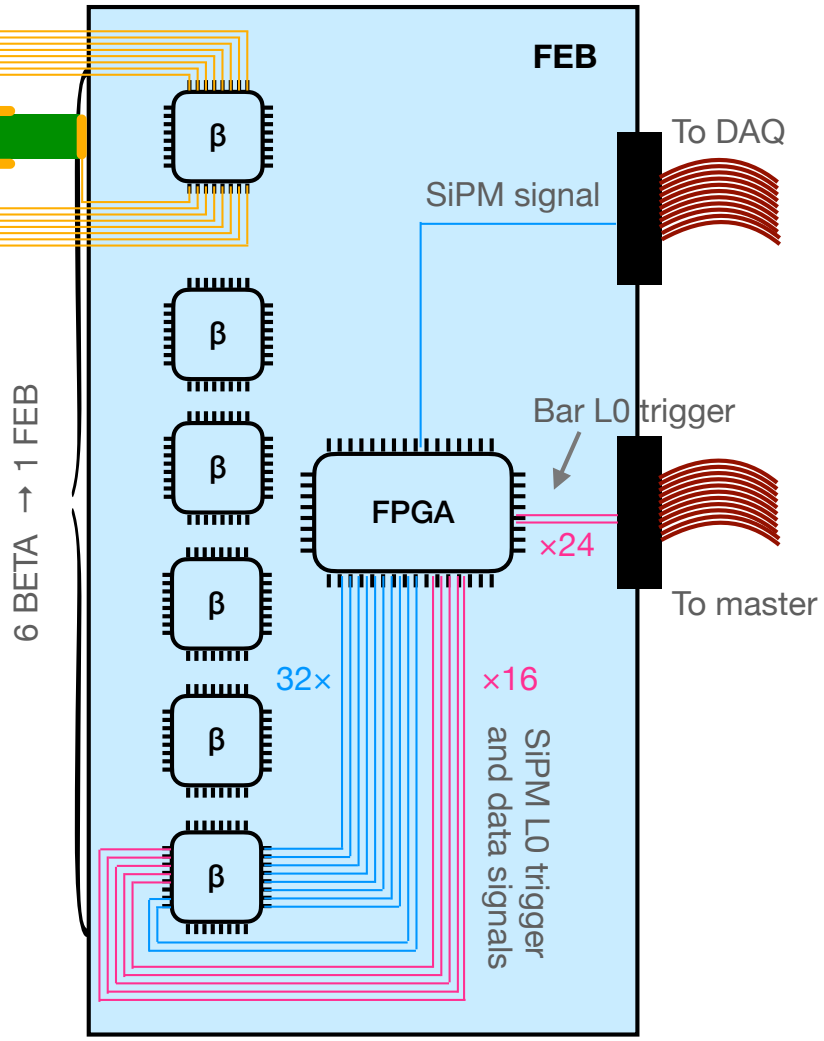
Proposed PSD trigger/DAQ architecture

- Front-end board (FEB):
  - process L0 trigger signals from BETA channel (=SiPM), and combine them into L0 trigger signals from PSD bar
  - Send data to DAQ system
- Master board:
  - Process L0 triggers from PSD bars and produces L1 veto signal(s) in RoI(s)
  - Accepts L2 triggers and orchestrates DAQ



Proposed FEB design

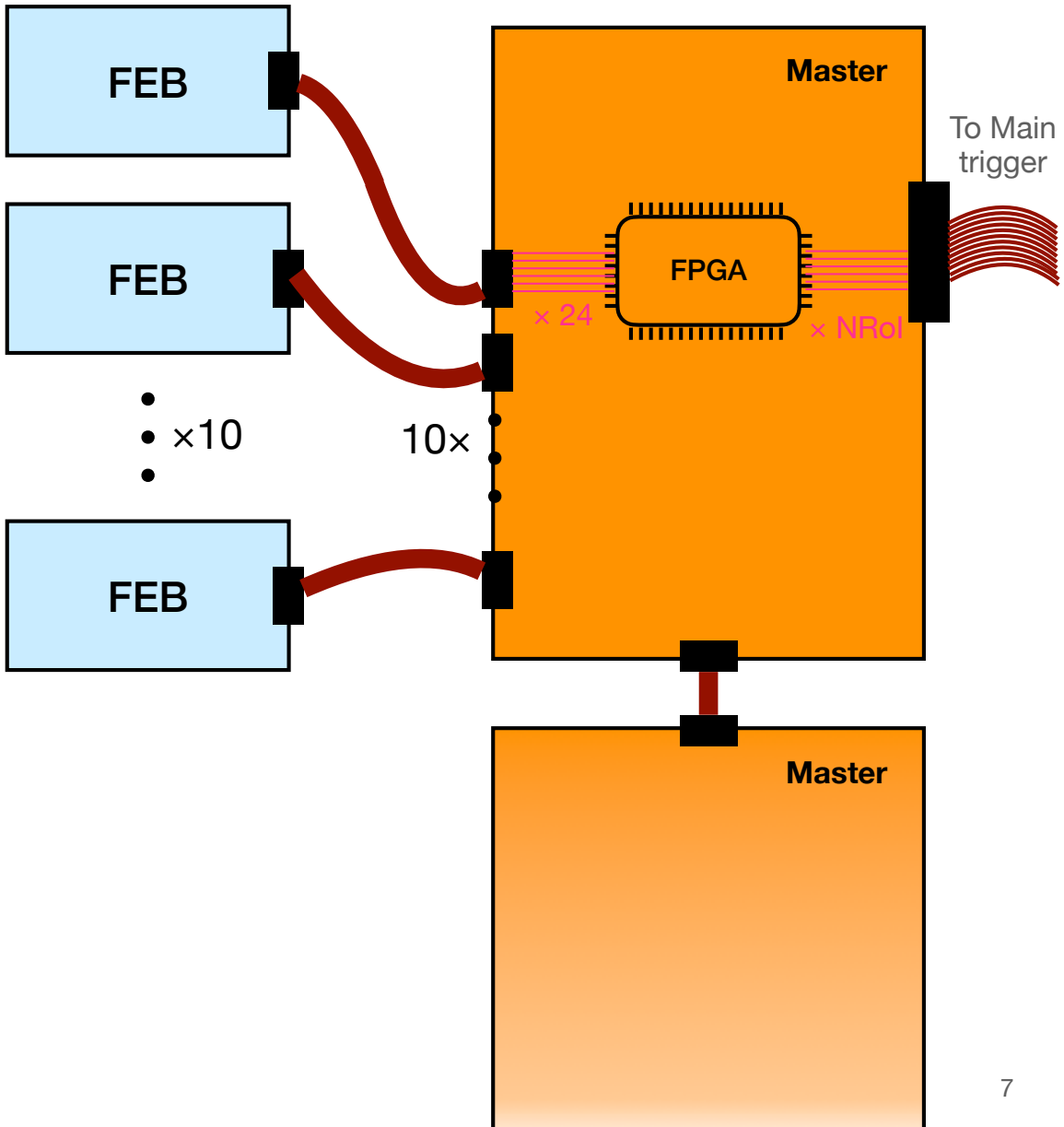




- ★ FPGA:
  - ★ Combines L0 trigger signals per SiPM into L0 trigger signal per PSD bar
  - ★ 96 trigger inputs + 2x96 signal inputs = 288 inputs (3 per SiPM: 1 trigger + 2 signal [differential])
  - ★ 24 output trigger signals (one per PSD bar, 4 SiPM per bar)
  - ★ Total: 312 channels
  - ★ Communication bus with Beta chips and data readout system

Proposed master board design

- Receives input from higher levels:
  - Trigger configuration
  - Data acquisition
  - L2 trigger
- FPGA
  - 24×10 = 240 input channels (L0 trigger signals from all the bars in a given PSD sector)
  - NRoI (<O(10)) output channels
  - Total ~260 channels
- DAQ management (with FEBs)



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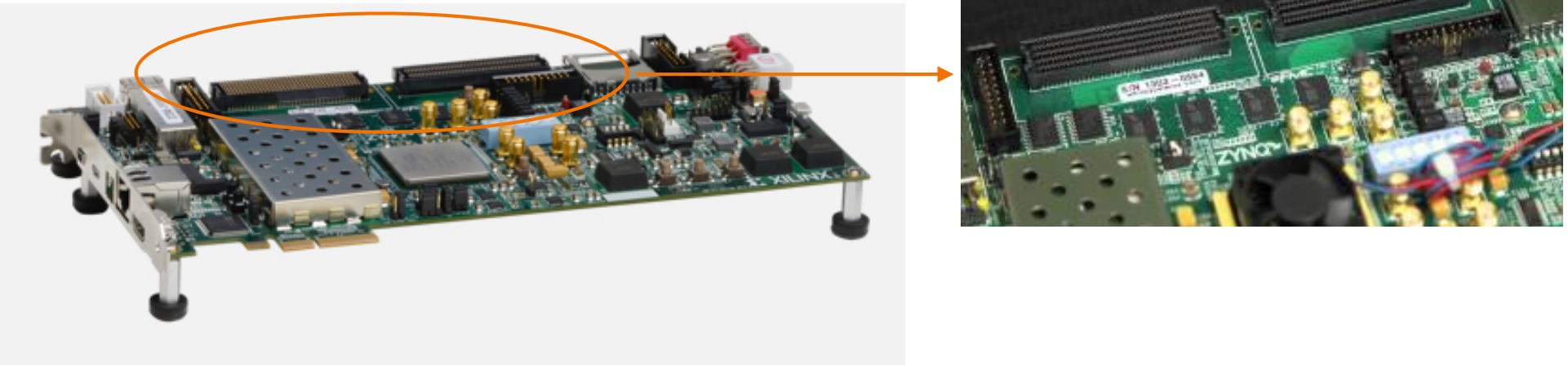
FPGA	Input	Output	Total
FEB	288	24	312
Master	240	2×NRoI [O(10)]	~260

Evaluation board

- Emulate the architecture in an evaluation board:
  - Gain experience with BETA
  - Early identification of problems
  - Test beams 2023
- Evaluation board zc706 from Xilinx with the XC7Z045-2FFG900C FPGA



Evaluation board

- Evaluation board proposal:
  - FMC connector has 136 input/outputs that can be used for trigger & Beta communications & readout.
  - 112 inputs will be used for trigger. It can address up to 28 PSD bars.
  - 112 inputs will require 7 BETA16 to be read.
  - 24 pins will be used for BETA readout & programming.
  - Evaluation board can simulate master & slave boards. Delays between boards can be generated using long cables & additional connectors.

Open questions

- How do we connect the SiPM to the BETA chip?
  - How this influences the physical location of the FEBs?
- Is the FPGA in the FEB really necessary? i.e:
  - Can BETA do the logical combination of the SiPM trigger signals and produce the bar trigger signal directly or do we need to do that in the FEB FPGA?
  - Does BETA includes an internal buffer for the data?
  - If the answer to these questions is “yes”: then we could remove the FPGA in the FEBs
- DAQ:
  - How do we need to serialize the data? Can the L2 signal arrive directly to the FEB or do we need the master to orchestrate DAQ?
- Communication: how do we communicate when the detector is in orbit for re-configurable parameters (e.g. set thresholds, redefine RoIs)
- Trigger:
  - How many output lines for the master? One per RoI? Or the number of bits to hold NRoI? If there is more than one RoI triggering at the same time then we need one line per RoI. Is that feasible for central trigger perspective?

Preliminary calendar

- **October 2022**
  - Design to be presented to/discuss within HERD Collaboration (PSD+trigger groups)
- **December 2022: Tests at IFAE**
  - Start checks latency for veto
  - Characterize overall functionality
  - Use evaluation board with BETA16-R[?, probably 1]
- **May 2023: CERN SPS (p)**
  - Check the PSD veto integrated within the PSD test module(s)
  - Use evaluation board and BETA16-R2
- **September 2023: CERN SPS+PS (e, p, ions)**
  - Verification of the ULEG L1 trigger concept, using enough PSD and FIT pieces
  - Use evaluation board and final BETA version (16-R2)
  - Integration in the main trigger/DAQ systems
- **September 2024: CERN Beamtest**
  - Provide PSD trigger and DAQ capabilities using the EFM