INFN Ground-up iNITiative for μElectronics developments

IGNITE

Programma di attività e preventivo di spesa
Sezione di Pavia

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Resp. Loc.: Gianluca Traversi

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IGNITE

- The goal of the project is to develop a detector-grade ASIC capable of readout different 4D pixel arrays with high-throughput data links for the next generation of HEP experiments

- Duration: 4 years

- Participating INFN groups:
  - INFN Bari
  - INFN Bologna
  - INFN Cagliari
  - INFN Firenze
  - INFN Genova
  - INFN L.N. Frascati
  - INFN Milano
  - INFN Milano Bicocca
  - INFN Padova
  - INFN Pavia
  - INFN Perugia
  - INFN Pisa
  - INFN Torino
  - TIFPA Trento

Physics case and technological challenges

- The feasibility of the HEP program of the next decades relies on a set of three fundamental requirements, which must be satisfied at the same time:
  - Time resolution per pixel σ_t < 10ps
  - Space resolution per pixel σ_s < 10μm
  - Resistance to particle fluence > 10^{17} 1-MeV n_{eq}/cm^2

A huge amount of data generated by the front-ends must be read out at unprecedented rates (order of 100 Gbps per ASIC)

The 2021 ECFA detector research and development roadmap document recommend supporting microelectronics as an essential component of future high-energy physics detector development.

Requirement	LHCbU2[6] Option 1	LHCbU2[6] Option 2	NA62[7] upgrade	CMS[8] run5	FCC-hh[9]
Pixel pitch [μm]	≤ 55	≤42	≤300	≤100	50-25
Matrix size	256x256	355x355	40x45	To be defined	To be defined
Time resolution RMS [ps]	<50	<50	≤50	30	10
Efficiency [%]	≥99	≥99	≥99	≥99	≥99
TID lifetime [MGy]	>24	>3	0.7/year	under study	1000
ToT resolution/range [bits]	6	8	under study	under study	To be defined
Power budget [W/cm^2]	1.5	1.5	4.5	1	To be defined
Power per pixel [μW]	23	14	<280	50	To be defined
Pixel rate [kHz]	<350	<40	<700	under study	To be defined
Data BW per ASIC [Gbps]	<250	<94	<55	under study	To be defined
Material budget (per station)	<0.8% X_0	<0.8% X_0	<0.5% X_0	under study	To be defined

The 28nm CMOS process

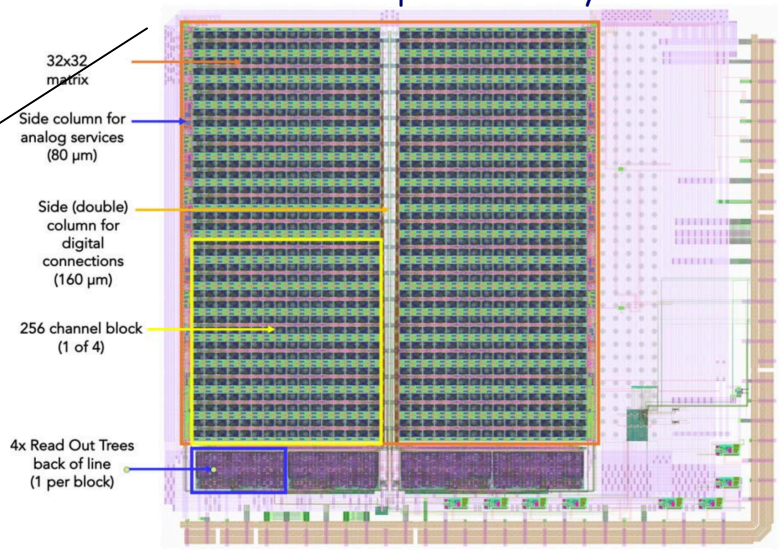
- When high input rates and high-precision timing are required, the integration of a Time-to-Digital-Converter (TDC) per pixel is mandatory, and the 65-nm CMOS technology node is not adequate anymore
- This pushes towards the choice of a more advanced technology node
- Various HEP institutes have officially elected the CMOS 28-nm as the main technology node for the next generation of LHC ASICs, and recently started to organize their design activity

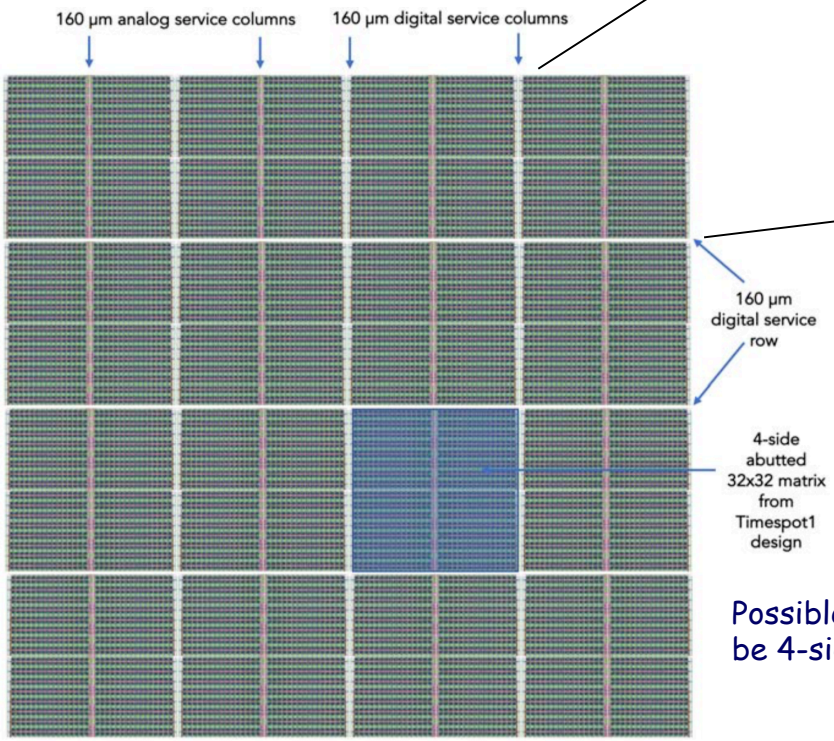
- The INFN experience:
  - (2015) ATLAS FTK team designed the AM-chip series in a full-custom digital design
  - (2015-2018) ScalTech28 project (CSN5) led a study about the 28nm performance against TID
  - (2018-2021) TimeSPOT (CSN5) developed the first CMOS 28-nm ASIC which integrates the full set of functionalities for the processing and read-out of pixels with time information (CSA+TDC)
  - (2020-2022) FALAPHEL (CSN5) is currently exploring the path towards the implementation of a 25 Gbps optical driver and data serializer using integrated photonics and 28-nm CMOS technology

TIMESPOT

- The first IGNITE device can be conceived as an ASIC which integrates, refines, and harmonizes the deliverables from the TimeSPOT and FALAPHEL developments, thus providing a complete read-out solution for 4D pixels.

The Timespot1 ASIC layout

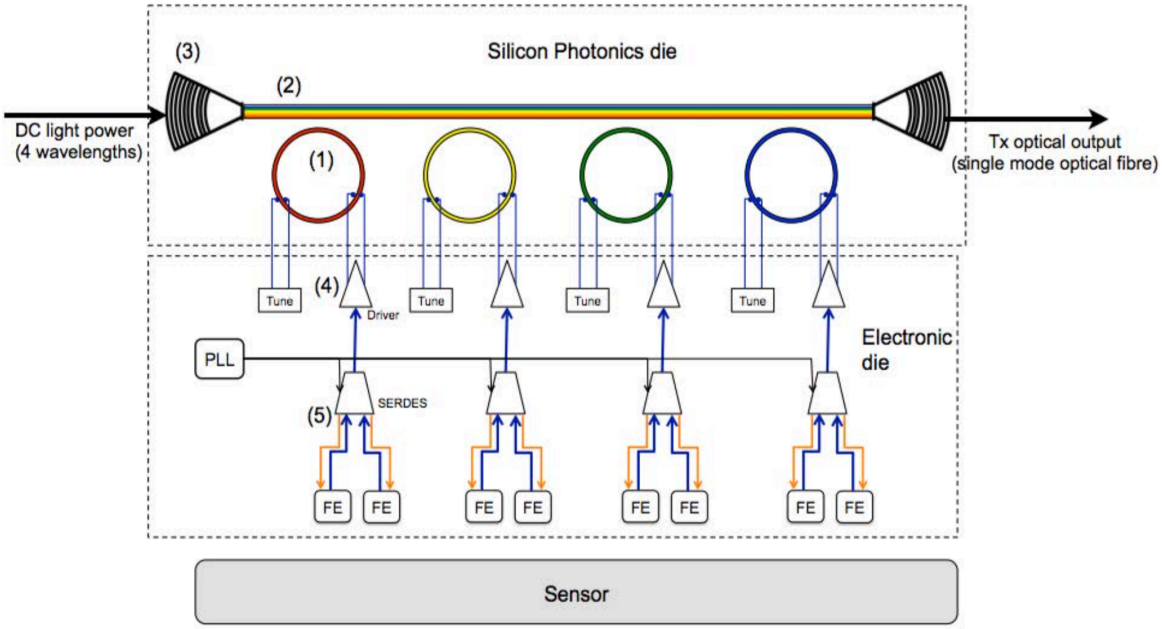


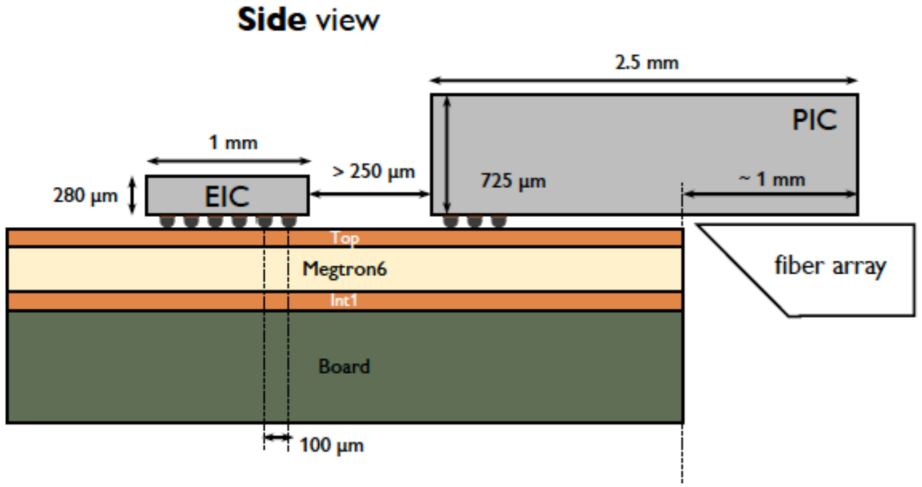


Possible layout of the first IGNITE device (128^2 pixels). The whole structure can be 4-side abutted. 128x128 pixels corresponds to a ≈ 7x7 mm^2 on the sensor side

FALAPHEL

- PIC devices implement a wavelength division multiplexing (WDM) technique. In a single device several Ring Modulators, tuned at slightly different wavelengths, are driven at 25 Gbps by the electronic circuits (EIC), thus effectively multiplying the output bandwidth by the number of wavelengths.

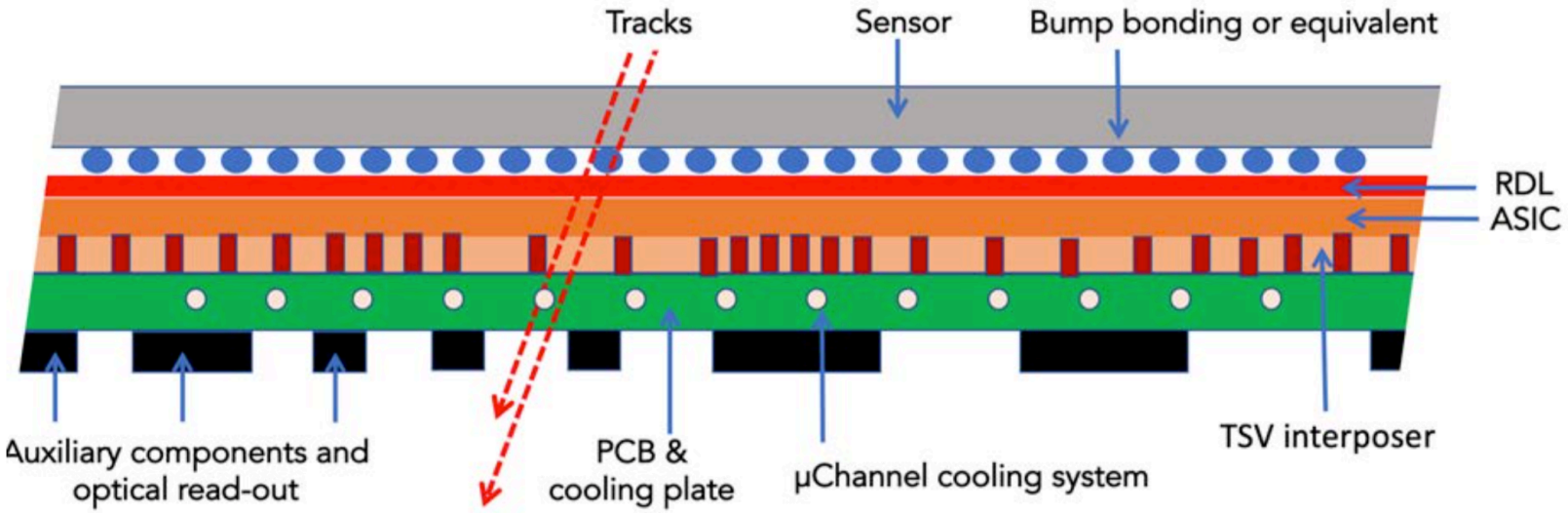




- PCB interposer for the integration of PIC and EIC. The EIC and the PIC are put in contact through a circuit using high-frequency low loss material, such as Megtron6 from Panasonic.
- Other solutions will be investigated, such as extending the TSV (Through Silicon Vias) interposer foreseen for the EIC-to-Sensor integration to the PIC-to-EIC integration.

System integration

- The clock mesh moves along the grid of the pixel-free areas -> suitable for vertical connections (TSV)
- The development of TSVs is crucial, as it would be decisive to solve several integration problems at the system level:
  - possibility to distribute global lines (ground, supply voltages, clock) directly inside the active area using an external interposer would be a much more robust solution concerning signal integrity
  - abutting could be made on the 4 sides also outside the ASIC layout -> production of a very large ASIC not necessary, with an important simplification of the ASIC design
  - vertical connections can be used also for data extraction, after local high-speed serialization, while the silicon-photonics ASIC, containing the line drivers, would be placed outside
- A possible drawback is the increase of the material budget along the track paths -> it requires a suitable study at the system level



Project management

INFN site	Main expertise in IGNITE	CSN1 experiment affiliations	Local responsible	FTE/persons (preliminary)
Bari	Analog IPs, ASIC integration	CMS, LHCb	F. Licciulli	0.7/3
Bologna	ASIC verification, HDL design	ATLAS	D. Falchieri	0.3/2
Cagliari	TDC, Analog F/E, fast signal distribution, system design and verification, photonics	LHCb	A.Lai	2.7/7
Firenze	System integration and test, HDL design	CMS, LHCb, NA62	G. Passaleva	2/8
Genova	System integration and tests, TID characterization	ATLAS	C. Gemme	0.1/1
L.N. Frascati	Complex PCB design	ATLAS, LHCb, NA62	P. Ciambrone	0.3/3
Milano	Fast signal distribution and R/O, analog IPs	ATLAS, LHCb	A.Stabile	1.3/4
Milano B.	Analog IPs, TID modeling	CMS	M. De Matteis	2/7
Padova	TID studies, Analog F/E	LHCb, CMS	P. Giubilato	1.4/7
Pavia	Analog F/E, TID studies on Analog F/E, fast output stages, advanced interconnectivity	CMS	G. Traversi	2/6
Perugia	Analog F/E	CMS, NA62	M. Menichelli	0.2/2
Pisa	Advanced interconnectivity, photonics, fast output stages	CMS, NA62	F. Palla	2/13
TIFPA	System integration and test, photonics	ATLAS	G-F. Dallabetta	1.3/5
Torino	Analog F/E, ASIC integration, TID characterization	CMS	L. Demaria	1/5

Work packages

WP	Development	Sites (preliminary)	WPR (preliminary)
1	Pixel design (Front-end, ADC, TDC, Logic)	Cagliari, Torino, Pavia, Milano, Perugia, Bologna	S.Cadeddu
2	Readout logic & Output stages	Pisa, Pavia, Milano	R. Beccherle
3	ASIC design Integration & verification	Bologna, Bari, Cagliari, Milano, Torino, Pisa, Pavia	F.Loddo
4	Silicon Photonics	Pisa, Cagliari, Trento	S. Faralli
5	TID study and modeling	Milano B, Torino, Cagliari, Pavia, Padova, Genova	A.Baschirotto
6	HDI techniques	Pisa, Pavia, Cagliari, TIFPA, Genova, Firenze	V. Re
7	System Integration and tests	Cagliari, Padova, Pavia, Genova, TIFPA, Firenze, Torino	A.Lai

Personale impegnato nella ricerca nel 2023

Name	Position	Commitment
Gianluca Traversi (responsabile locale)	P.A.	0.5
Lodovico Ratti	P.O.	0.2
Massimo Manghisoni	P.O.	0.2
Luigi Gaioni	P.A.	0.3
Valerio Re	P.O.	0.3
Elisa Riceputi	R.T.D. A	0.5
TOTAL (FULL TIME EQUIVALENT)		**2.0**

Le percentuali di IGNITE sono sinergiche rispetto a qualunque esperimento LHC per quanto riguarda la soglia del 70% per il diritto di firma

L'attività è inoltre anche sinergica con FALAPHEL (CNS 5)

Complessivamente: 52 **Ricercatori** (11.85 FTE) – 21 **Tecnologi** (5.65 FTE)

Richieste finanziarie del quadriennio

Year	Activity	Budget Estimate (k€)
2023	Travels (testbeams, contacts with companies)	15
	Design & submission MPW PC1 5x5 mm2	50
	Design & submission MPW ASIC1 7x7 mm2	300
	System Integration studies & prototypes	50
	Development of PCB for tests of standalone system parts	40
	Labo consumables & tooling for tests	15
	Total (k€)	**470**
2024	Travels (testbeams, contacts with companies)	15
	PCB for system tests	40
	Fast DAQ for system tests	25
	Rent of high-end scopes for tests on data links	20
	Components & cabling for PCB	30
	System integration (ASIC1 and PC1)	150
	Fiber arrays	20
	Labo consumables & tooling for tests	20
	Irradiation	10
	Total (k€)	**330**

55 keuro +
415 keuro SJ

Richieste finanziarie del quadriennio

2025	Travels (testbeams, contacts with companies)	15
	Design & submission MPW run for PC2 5x5 mm2	50
	Design & submission Engineering run for ASIC2	1200
	Finalization of Hybridization & Integration	250
	Labo consumables & tooling for tests	20
	Total (k€)	**1535**
2026	Travels (testbeams, contacts with companies)	15
	PCB for system tests	40
	Rent of high-end scopes for tests on data links	20
	Components & cabling for PCB	20
	Finalization of system integration (Sensor, ASIC2 and PC2)	200
	Fiber arrays	20
	Labo consumables & tooling for tests	20
	Irradiation	10
	Total (k€)	**345**
Total project k€ (w/o personnel contracts)		**2680**

Richieste finanziarie della sezione di Pavia nel 2023

Consumo	Prove tecnologiche su metodologie a interconnessione verticale per primo prototipo IGNITE	**10 keuro**
	TOTALE	**10 keuro**

Nessuna richiesta di servizi alla sezione