EIC_NET
Silicon Tracker update

- **Giacomo Contin**

Università di Trieste and INFN Sezione di Trieste

- Riunione EIC_NET – 03 October 2022

Outline

- EIC Silicon Consortium activities update
- R&D funding proposals
  - FY23 Generic R&D
  - FY23 eRD104 – eRD111- eRD113 Project R&D
- ALICE ITS3 synergies

Silicon Consortium for the EIC

Mission and Organizational tasks:

- coordinating effort towards the EIC silicon tracker
  - ✓ supporting the EPIC Tracking Working group and the R&D activities
  - ✓ open to all the EIC interested groups and institutions
- weekly Coordination meetings, on Monday @1pm EDT:
  - ✓ indico: https://indico.bnl.gov/category/387/
  - ✓ promoting activity progress and coordinating institutional relationship
  - ✓ people: N. Apadula (LBL), **G. Contin** (INFN Trieste), G. Deptuch (BNL), L. Greiner (LBL), **D. Elia** (INFN Bari), L. Gonella (Birmingham), P. Jones (Birmingham), I. Sedgwick (RAL), E. Sichtermann (LBL)
- bi-weekly General meetings (eic-rd-silicon-l@lists.bnl.gov):
  - ✓ indico: https://indico.bnl.gov/category/386/
  - ✓ SC activity progress reports (including activity for projects eRD104 and eRD111 so far)
  - ✓ involving participants and presenters by the different groups
  - ✓ latest meeting: September 29 (discussion of eRD proposal submissions)

Silicon Consortium actions and news

- Promoting SC institutes' participation in ITS3 activities
  - Sensor design: BNL and LBL joined RAL in actively contributing
  - Sensor characterization: test systems received by most of the interested groups
  - ORNL, LBL members hosted at INFN Trieste for training in testing
- Promoting MoU between ALICE/CERN and EIC/DOE
  - Contacts with Luciano Musa, Elke, Rolf continues to draft an agreement
  - BNL designers defining terms of agreement for sensor development
- Finding and planning resources for:
  - EIC-specific development
  - Contribution to ITS3 development
- INFN Padova joining the R&D for the EPIC Tracker!

EIC Generic R&D call FY23

- Call: “This program will support advanced R&D on innovative, cost-effective detector concepts which reduce risk and that either the one detector in the project scope or a second detector could incorporate. “
- Proposal submitted on July 25 2022 by SC/Tracking WG members: “Silicon Tracking and Vertexing Consortium”
- R&D items:
  - **Embedded Monolithic Active Pixel Sensor R&D**
    - **Additive manufacturing of power and data redistribution layers on thin large-area silicon**
  - Aluminum Flexible Circuit Manufacturing Capability
  - Functional Verification Model of EIC Tracking and Vertexing Detectors R&D
  - Ultra-fast Timing Monolithic Active Pixel Sensors
- Total request: 574.2 k$
  - **INFN: ~0.4 Post-doc FTE = 34k$, material = 15k$**

EIC Project R&D - eRD104 Silicon Services Reduction

- Powering goals:
  - Detailed concept and analysis of powering distribution schemes based on DC-DC and SP
  - Evaluation of existing regulators and of powered MLR1 structures performance
- Readout goals:
  - Explore radiation tolerant FPGA options and high speed fiber optic transmission options with evaluation boards and interface boards
  - Develop prototype multiplexing firmware
  - Beam tests for fault testing of the devices
  - Analysis of multiplexing designs and full cost benefit report
  - Development and test of data transmission on high insertion loss cables
- Proponents: UK groups, ORNL, BNL
- Total request: 255.5 k$

EIC Project R&D - eRD111 Silicon Tracking

- **Forming modules from stitched sensors**
  - Optimization of the 65nm stitched sensor dimensions for EPIC
  - Exploration of integration options in the module
- Barrel & discs
  - Conceptual design and prototypes of the vertexing layers including supports
  - Advanced stave and disc conceptual designs and prototypes
- Mechanics, integration, & cooling
  - CAD model of silicon tracker
  - Analysis of the cooling options for the tracker
  - Conceptual designs and prototypes for the full set of detector support structures

- Proponents: UK, **INFN**, LANL, LBNL, ORNL
- Total request: 786.6 k$
  - **INFN: 0.25 Post-doc FTE = 20k$, material = 10k$**

EIC Project R&D - eRD113 Sensor Dev. & Char.

- Establish credibility within the ALICE ITS3, accomplish legal, organizational and export control agreements with CERN to share design databases
- **Progress in testing and characterization**
  - Produce a copy of the test system now under development for the large area sensor and adapt the ancillary test equipment to the new sensor size and characteristics
  - Develop setup and procedures needed to test the stitched sensor prototypes in curved configuration
- Contribute to design of selected blocks
- Understand implications of changing stitching plans and make the plausible plan for LAS for the EIC, evaluate functionalities and circuitry for EIC
- Evaluate implications of adopting serial powering on the sensor biasing

- Proponents: UK, **INFN**, BNL, LBNL, ORNL, LANL
- Total request: 2,628 k$
  - **INFN: 0.25 Post-doc FTE = 20 k$, material = 10 k$**

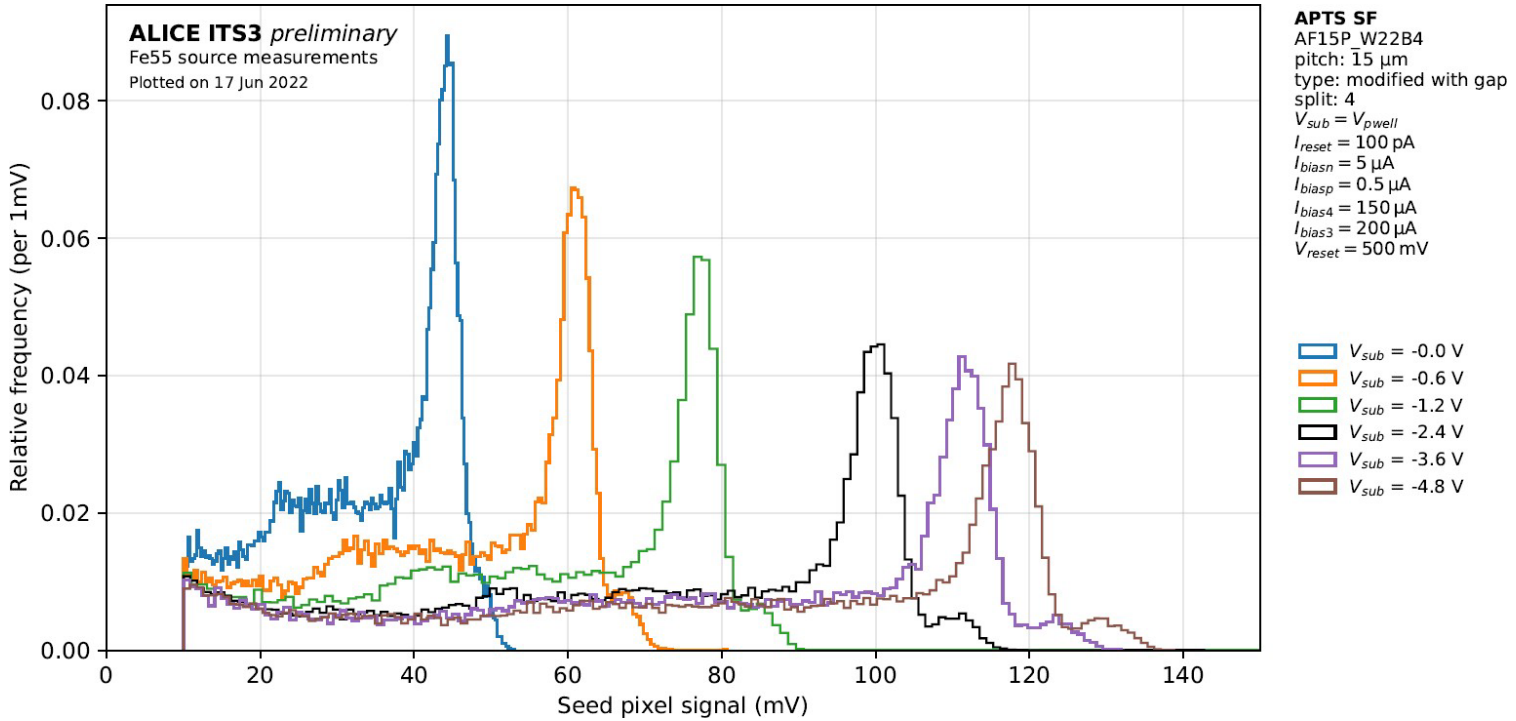
Progress report from ALICE ITS3

Quantitative results are from public presentations

APTS-SF: Substrate bias amplifies the signal

From S. Senyukov at IWORID '22

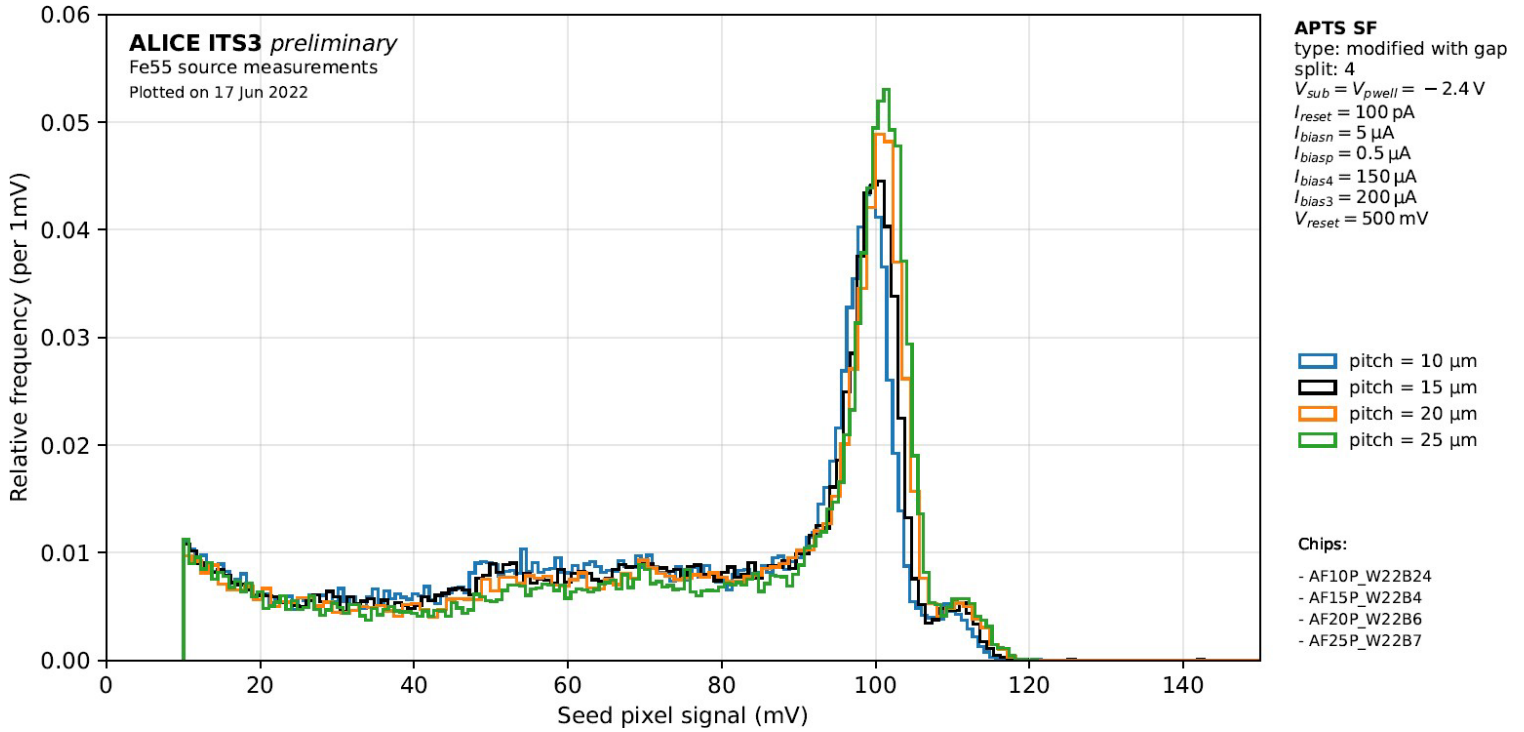
- Substrate bias lowers the node capacitance to as low as 2.2 fF
- Signal amplitude increases



APTS-SF: Charge collection vs. pixel pitch

From S. Senyukov at IWORID '22

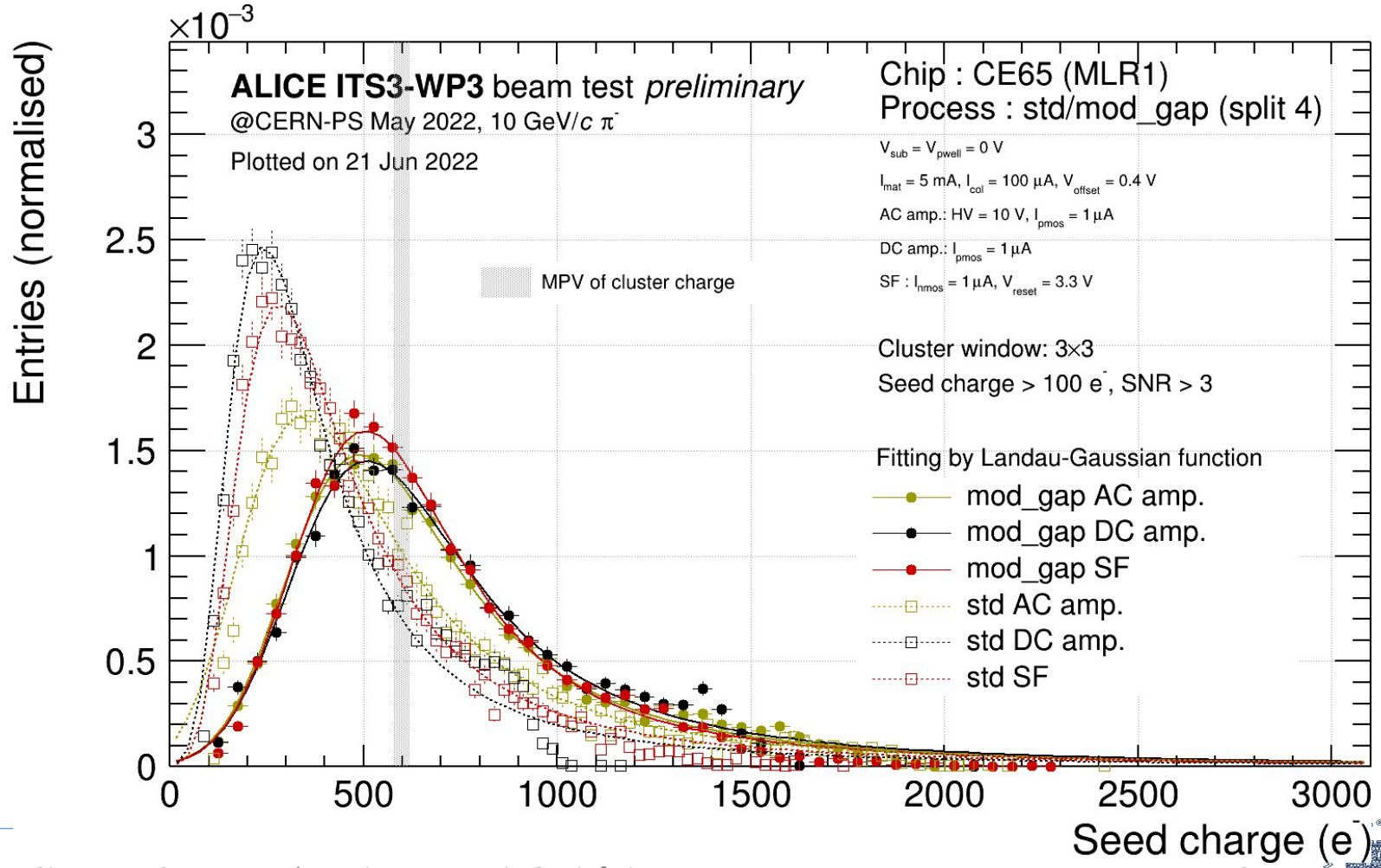
- Charge collection efficiency doesn't seem to depend on pixel pitch
- Remarkable result to be confirmed by beam test
- If efficiency stays high at larger pitches -> way to decrease the power consumption



CE65: Process modification reduces charge sharing

From S. Senyukov at IWORID '22

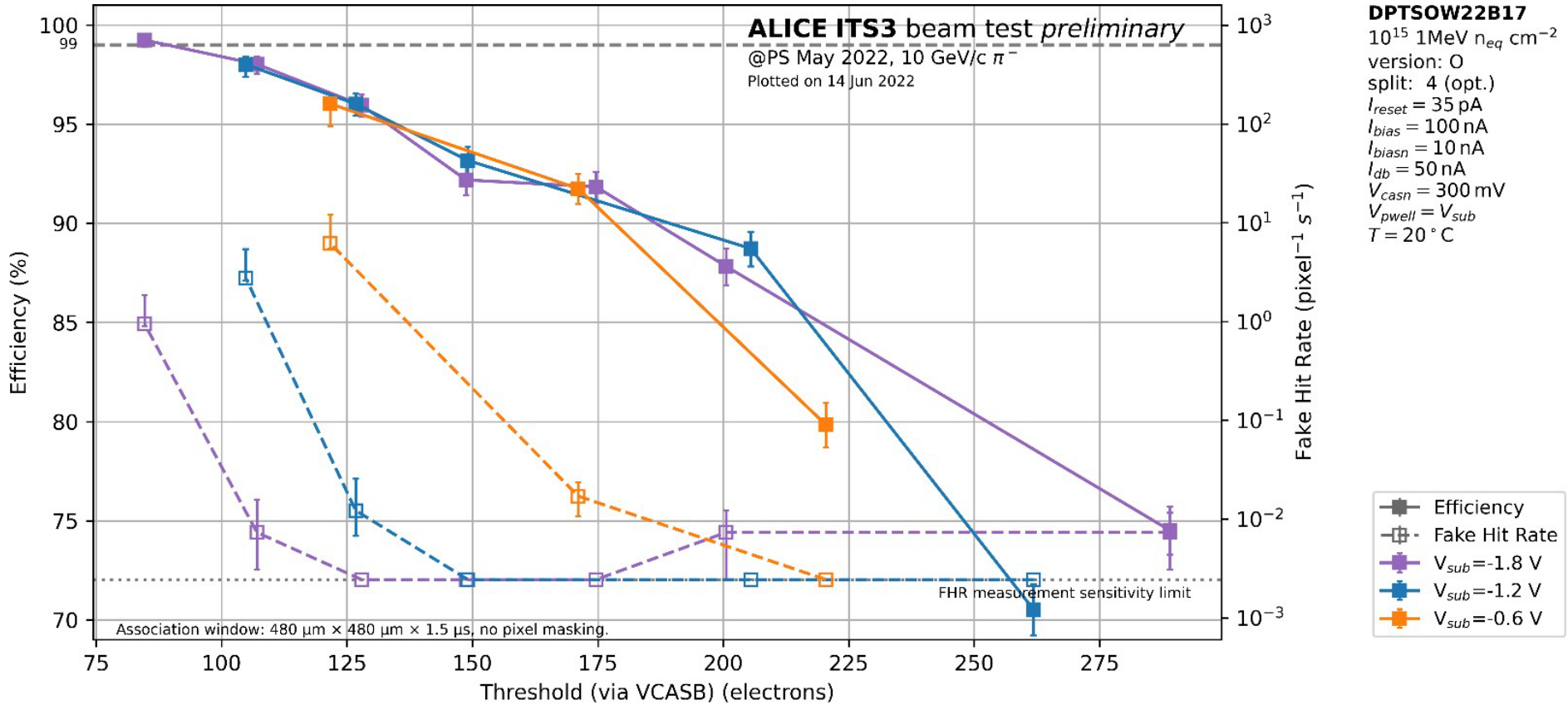
- Effect observed in APTS with ^{55}Fe sources confirmed at beam test
- In modified process all charge is mostly collected by single pixel



Irradiated DPTS (10^{15} n_{eq})

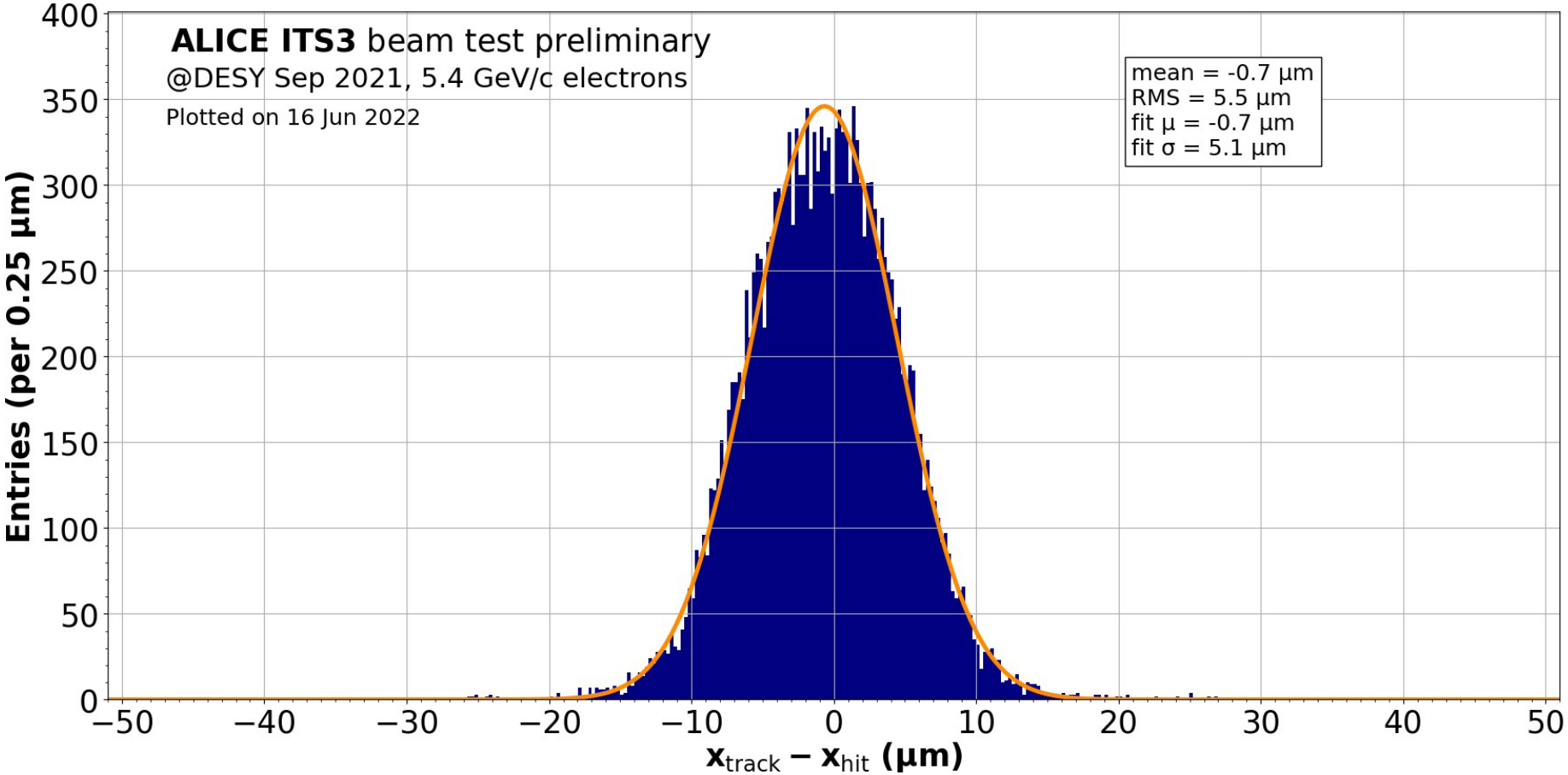
- Efficient at 20 °C with limited fake hit rate

From S. Senyukov at IWORID '22



DPTS: Spatial resolution ~5 µm

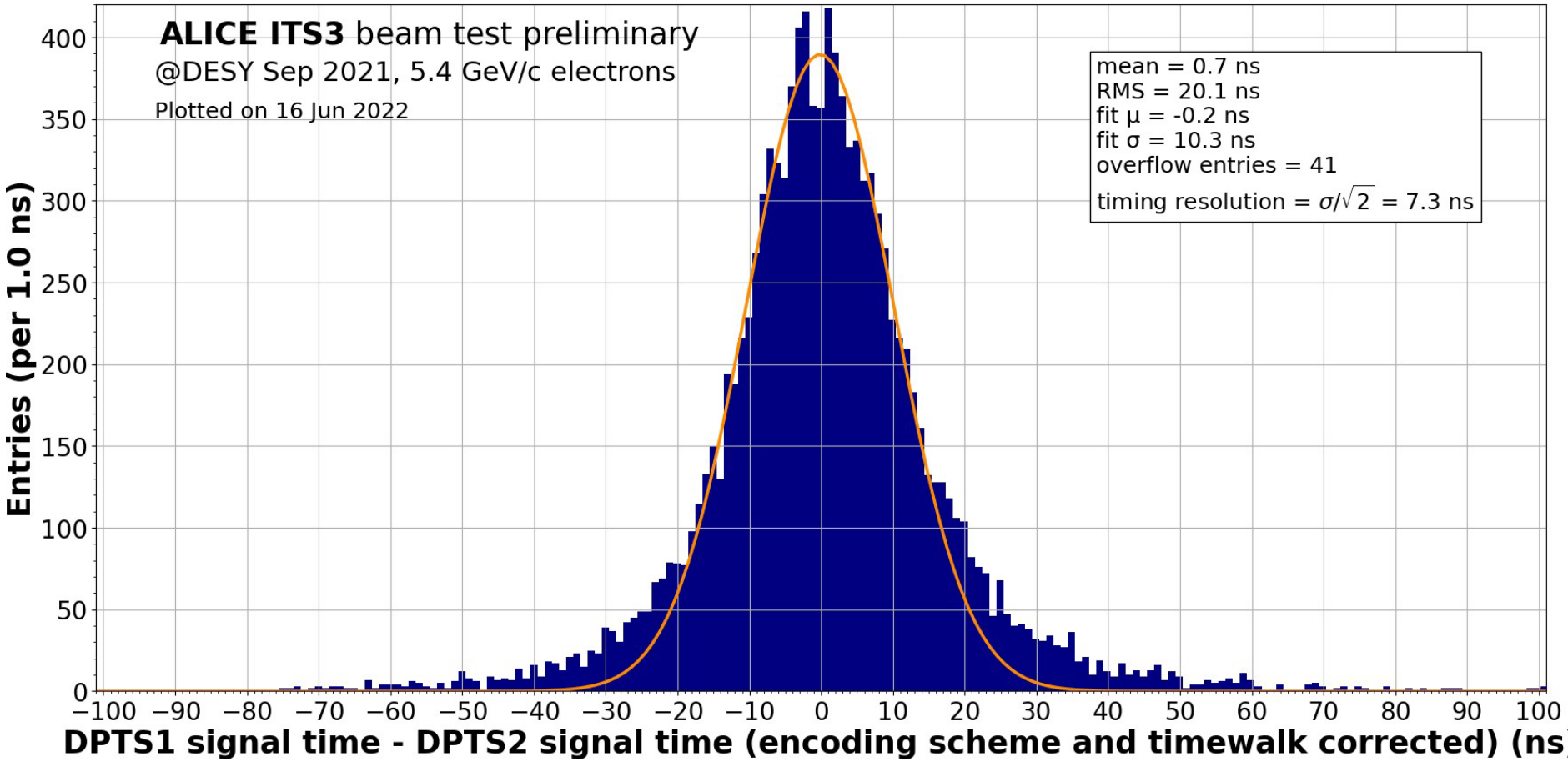
From S. Senyukov at IWORID '22



DPTSOW22B3 (not irradiated)
version: O
split: 4 (opt.)
$I_{reset} = 10\,pA$
$I_{bias} = 100\,nA$
$I_{biasn} = 10\,nA$
$I_{db} = 100\,nA$
$V_{casn} = 300\,mV$
$V_{casb} = 250\,mV$
$V_{pwell} = V_{sub} = -1.2V$

DPTS: Temporal resolution ~7 ns

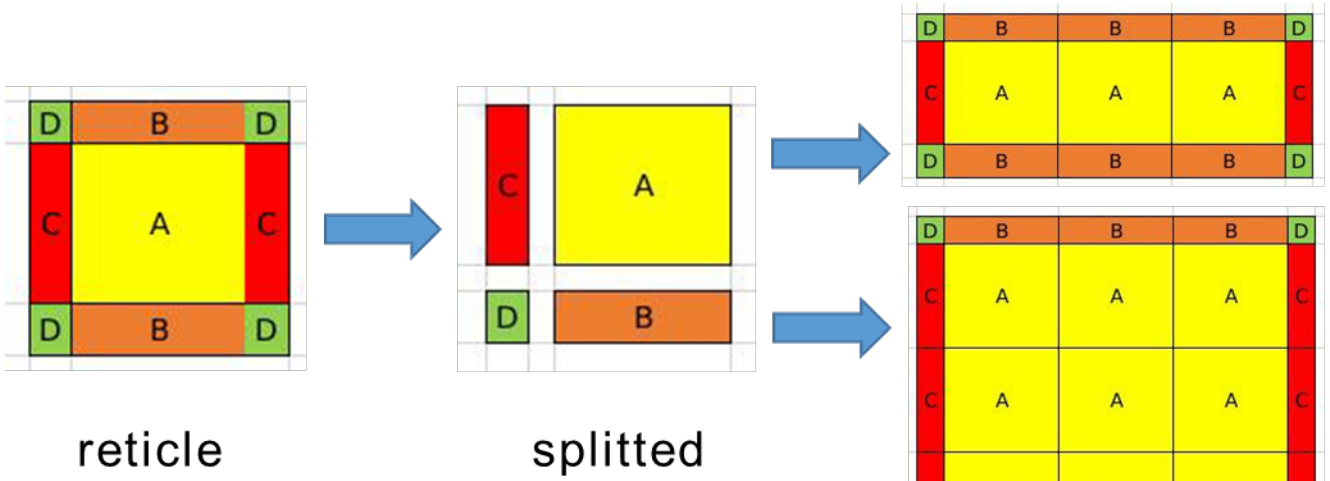
From S. Senyukov at IWORID '22



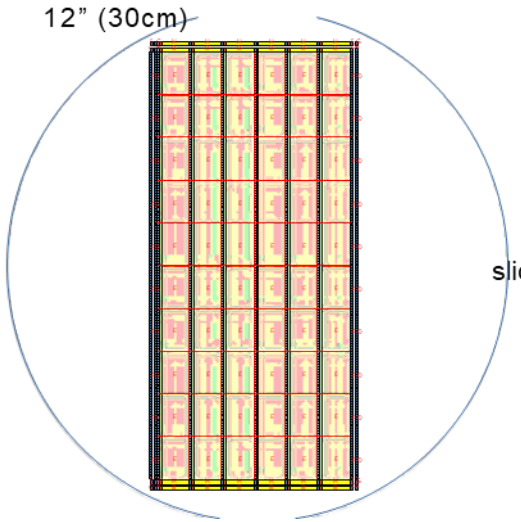
DPTSOW22B3 (not irradiated)
version: O
split: 4 (opt.)
$I_{reset} = 10\,pA$
$I_{bias} = 100\,nA$
$I_{biasn} = 10\,nA$
$I_{db} = 100\,nA$
$V_{casn} = 300\,mV$
$V_{casb} = 250\,mV$
$V_{pwell} = V_{sub} = -1.2V$

DPTSXW22B1 (not irradiated)
version: X
split: 4 (opt.)
$I_{reset} = 10\,pA$
$I_{bias} = 100\,nA$
$I_{biasn} = 10\,nA$
$I_{db} = 100\,nA$
$V_{casn} = 300\,mV$
$V_{casb} = 280\,mV$
$V_{pwell} = V_{sub} = -1.2V$

ITS3 progress report: ER1 stitched sensor



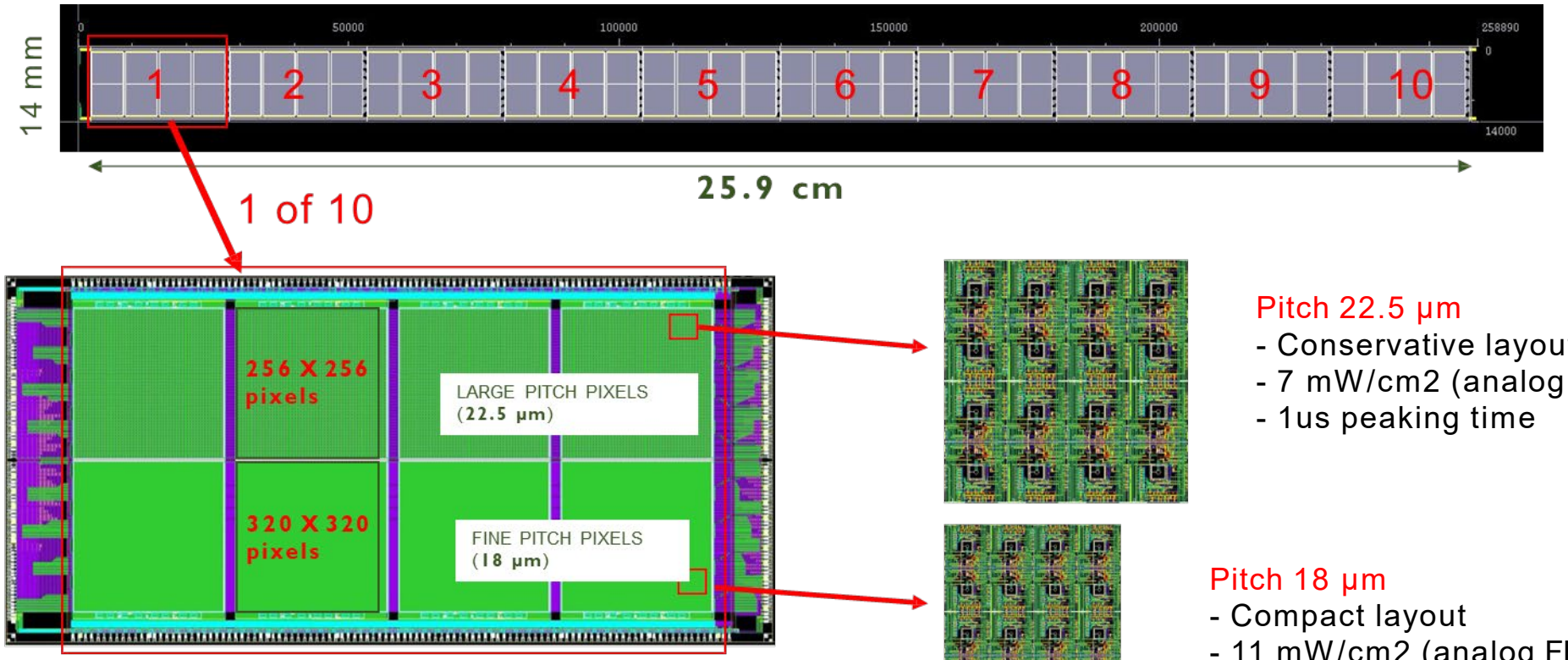
From [P. Leitao at TWEPP '22]



thinned wafers to < 50 um
slice wafers to size depending on radii

6 wafers make the entire ITS3 production

ITS3 progress report: ER1 MOSS Prototype



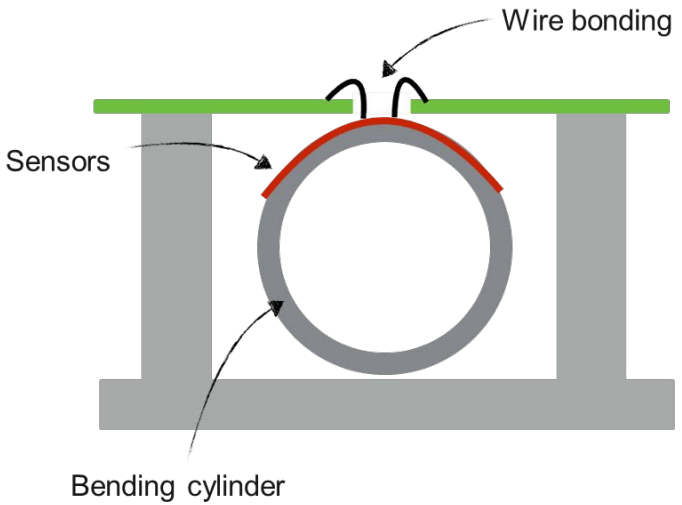
Pitch 22.5 µm
- Conservative layout
- 7 mW/cm2 (analog FE)
- 1us peaking time

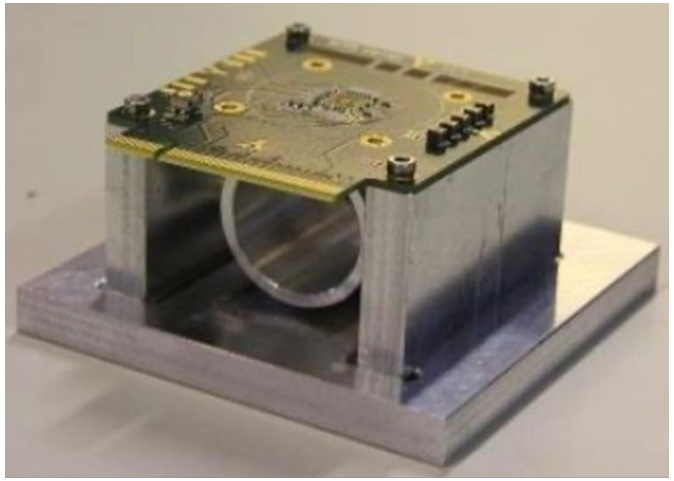
Pitch 18 µm
- Compact layout
- 11 mW/cm2 (analog FE)
- 1us peaking time

- 1.4 x 26 cm monolithic stitched sensor
- Binary readout with parameterizable strobe duration
- In-pixel latch with fast OR for column and row signals
- Analog and digital pulse testing per pixel
- 736.3 Million transistors
- 1.67 Million pixels

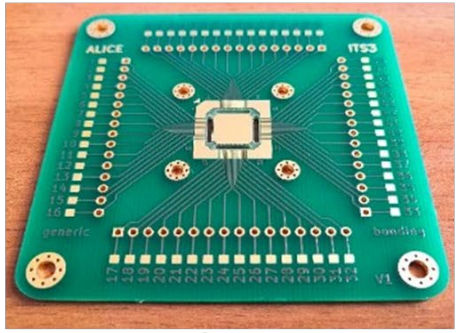
From P. Leitao at TWEPP '22

ITS3 progress report: bending 65nm chips





APTS_SF modified board



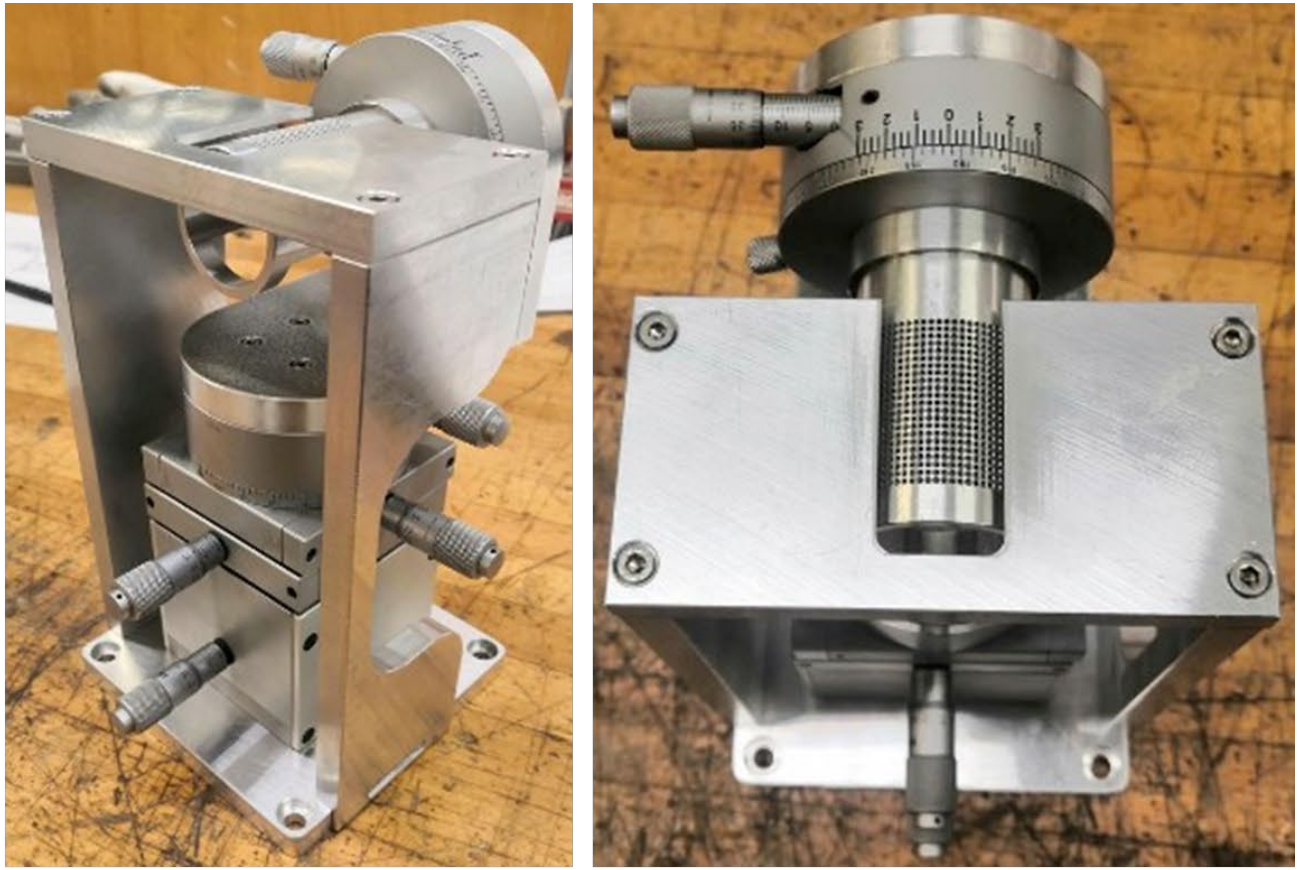
Transistor/multi-purpose adapter

From D. Colella – AUW 9/22

ITS3 progress report: bending 65nm chips

- ➡ Jig for chip-cylinder alignment ready
- ➡ Carrier jig being adapted to telescope setup
- ➡ Starting assembly in September with dummy chips

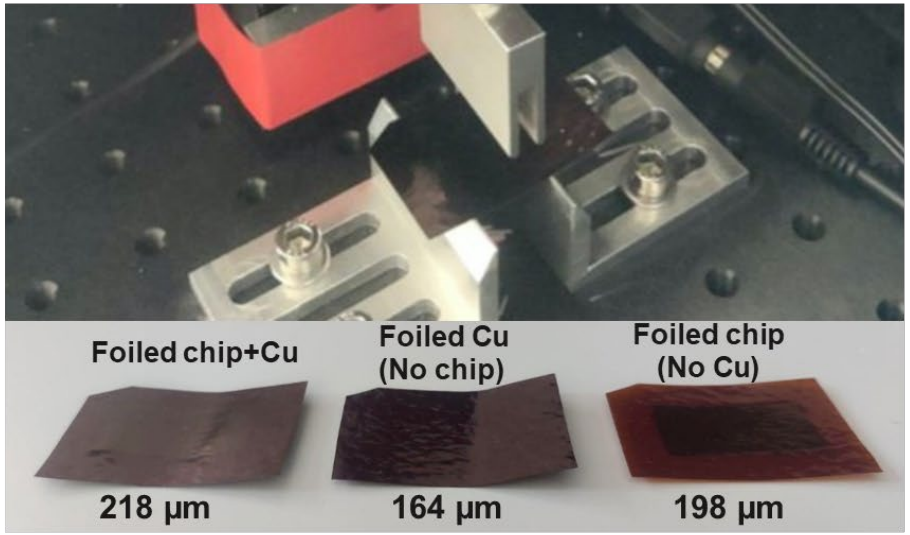
From D. Colella – AUW 9/22



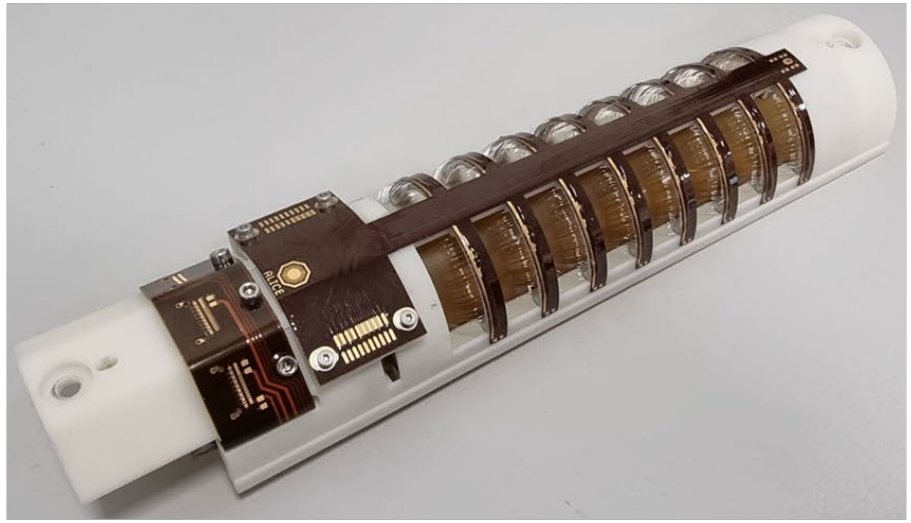
Chip-cylinder alignment jig

ITS3 progress report: integration

➡ **MAPS foil: new measurements looking for breaking point**



➡ **Super-ALPIDE: starting the assembly of first functional sample**



➡ **ITS3 FPC: design and simulation ongoing**

From D. Colella – AUW 9/22

Conclusions

- EIC Silicon Consortium pursuing tracker development for EPIC
  - Proposals submitted for Generic and Project R&D Programs for FY23
  - INFN Padova joins Bari and Trieste for FY23

- EIC SC participation in ITS3 is crucial
  - Test system received by several groups, training is ongoing
  - Active participation in sensor design by BNL, LBL, RAL
  - Working on DOE/CERN, EIC/ALICE, SC/ITS3 agreements