FALAPHEL Meeting

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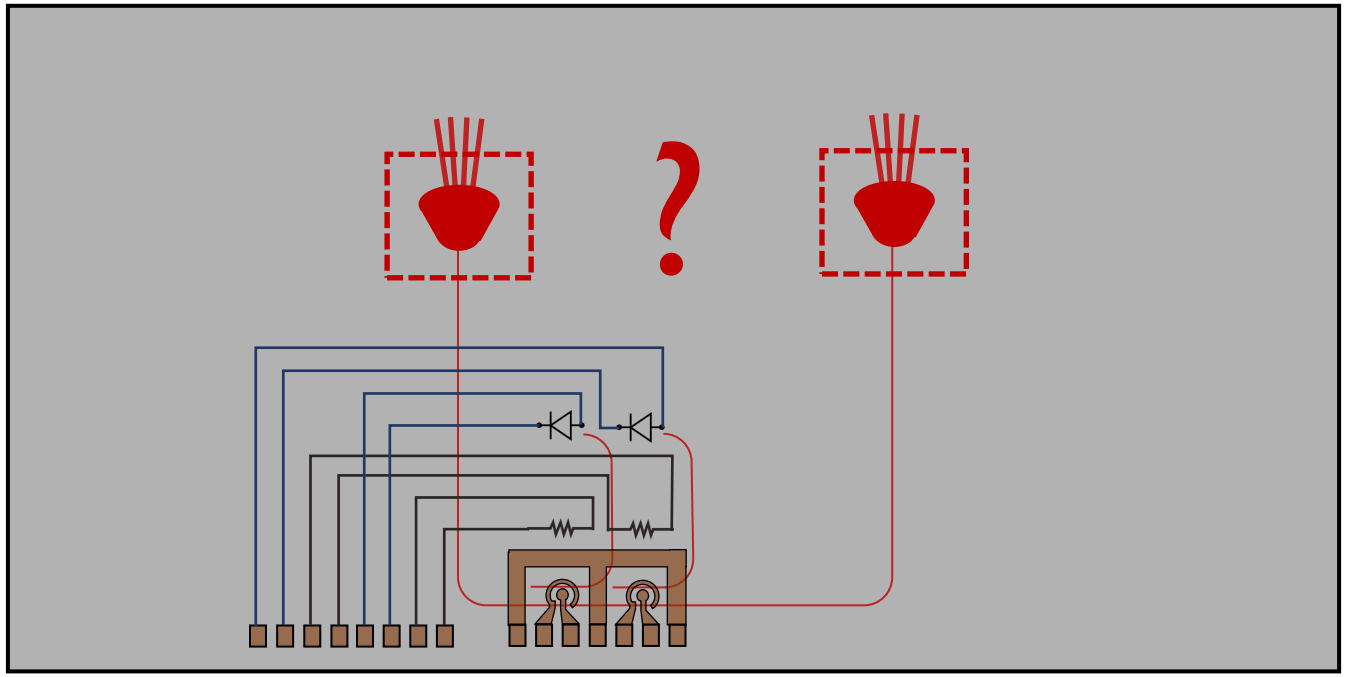
Pisa, 12 October 2022

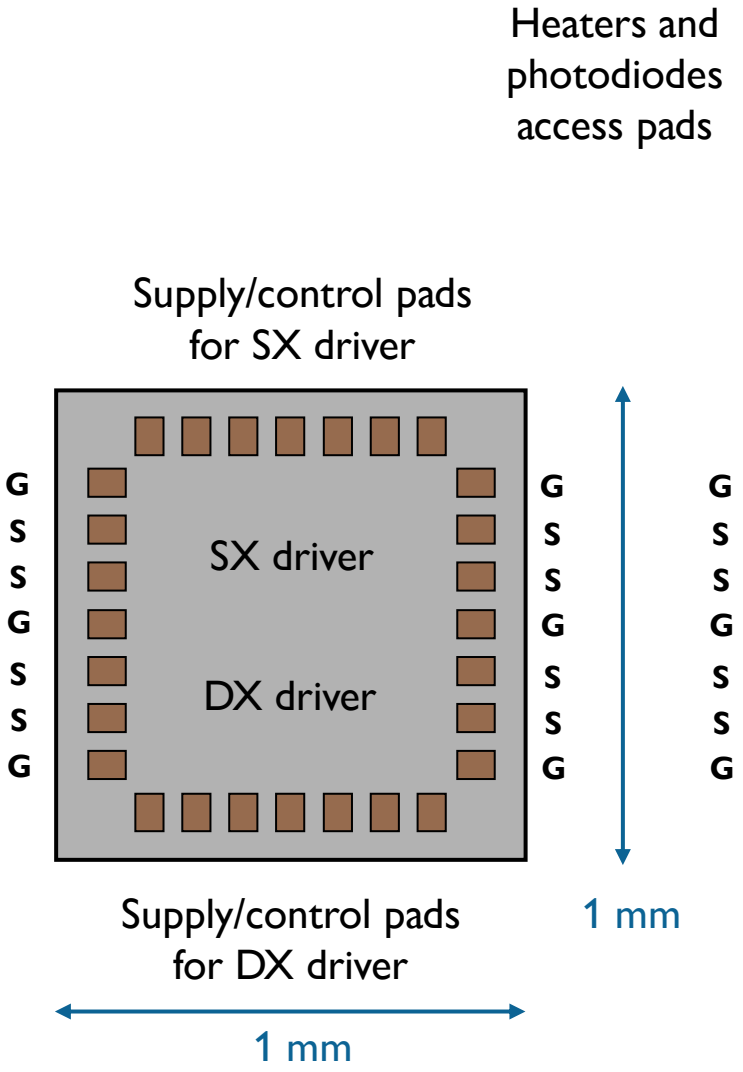
PIC v2 – Goals (06/2022)

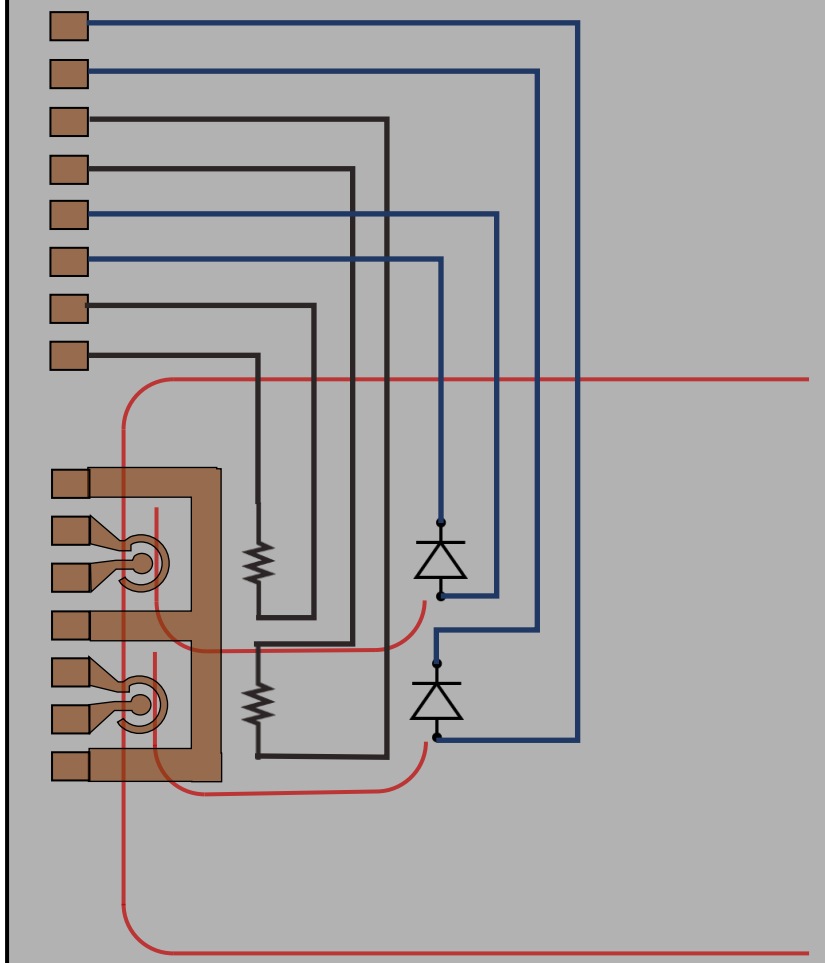
- Test vehicles for 50 Gb/s 2-WDM electro-optical demonstrators
- Solutions with both building block devices (no optical feedback) and custom ones
- Add-drop custom RMs need to be completely redesigned
- At most 4 complete 2-WDM structures can be probably accommodated on the PIC
- External wavelength demultiplexer to be used for testing



PIC v2 – Integration (06/2022)

- Differential driver architecture to double effective peak-to-peak voltage swing on RM
- RM as differential load on a CML-like output stage requires signal-signal (SS), i.e., anode-cathode, pad configuration
- **GSSG** pattern preferred to limit RM-to-RM cross-talk
- **2-WDM** demonstrator: 2 drivers in a single EIC





PIC v2 – Timeline

- Design start ~ end of Aug 2022
- Notification of major PDK change ~ early of Sept 2022
- PDK with quantitative technological performances delivery ~ end of Sept 2022
- Original GDS submission deadline 05 Oct 2022
- Extended GDS submission deadline **12 Oct 2022**
- Final DRC free GDS submission ~ 05 Nov 2022

- Expected PIC delivery Oct 2023 (12 months turn-around)

Considering Imec's general tendency (and previous experience!) it is likely that the PIC will be delivered around Dec 2023/Jan 2024

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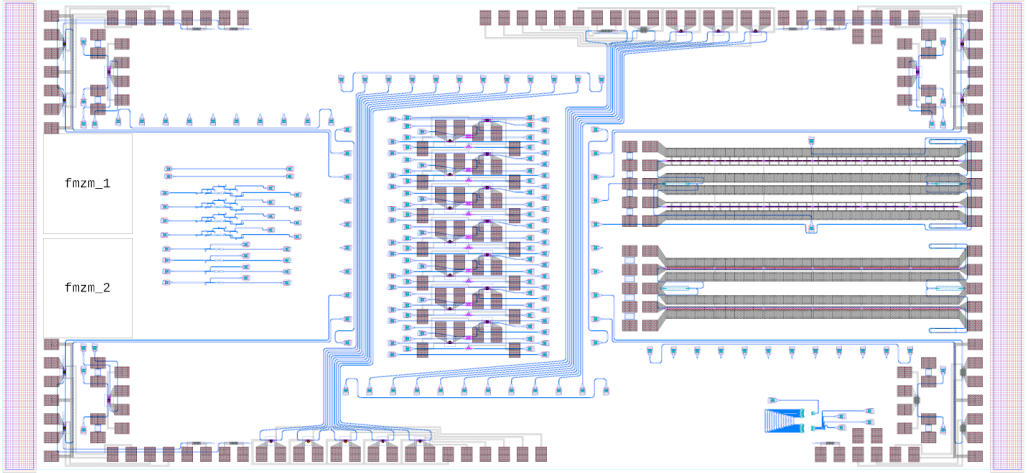
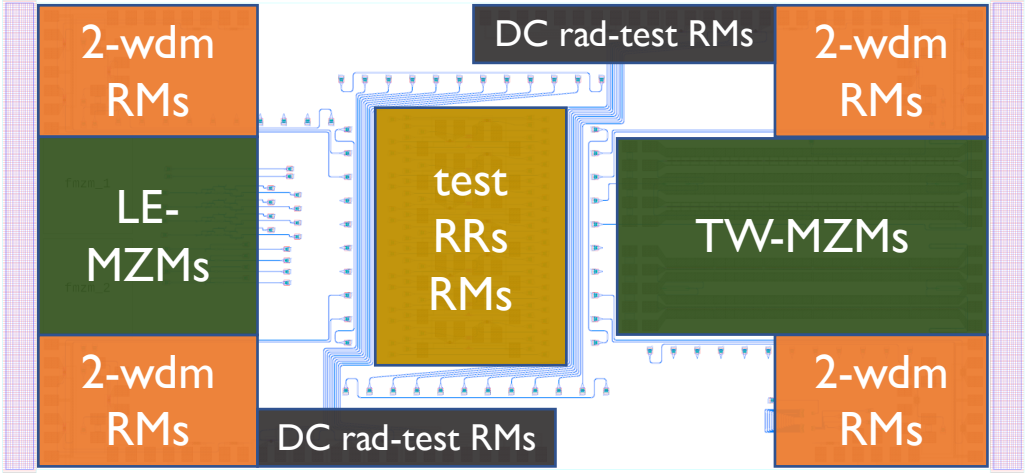
PIC v2 – Quick Summary and Floorplan

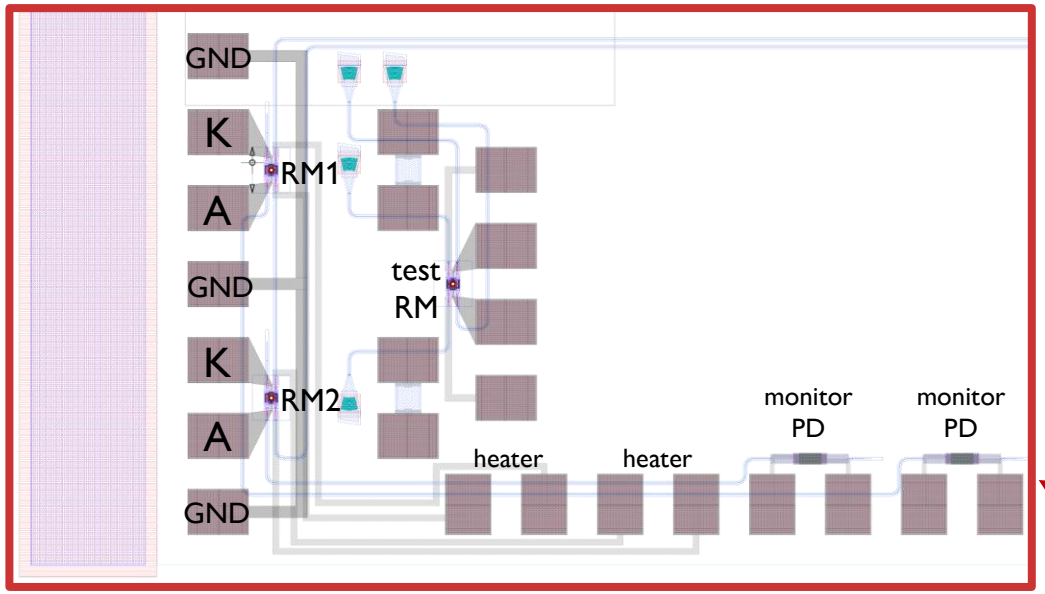
- 2-WDM RM-based structures: 1 with imec's RM, 3 with **new** custom add-drop RMs
- Several optical-bench test-able RMs to validate custom building blocks for final demonstrator run
- DC-testable all-pass RM designs for radiation-hardness validation
- MZMs follow-up designs from previous PIC, traveling-wave and lumped versions
- Passive components: polarization beam-splitters and rotators, AWGs as passive wavelength demux

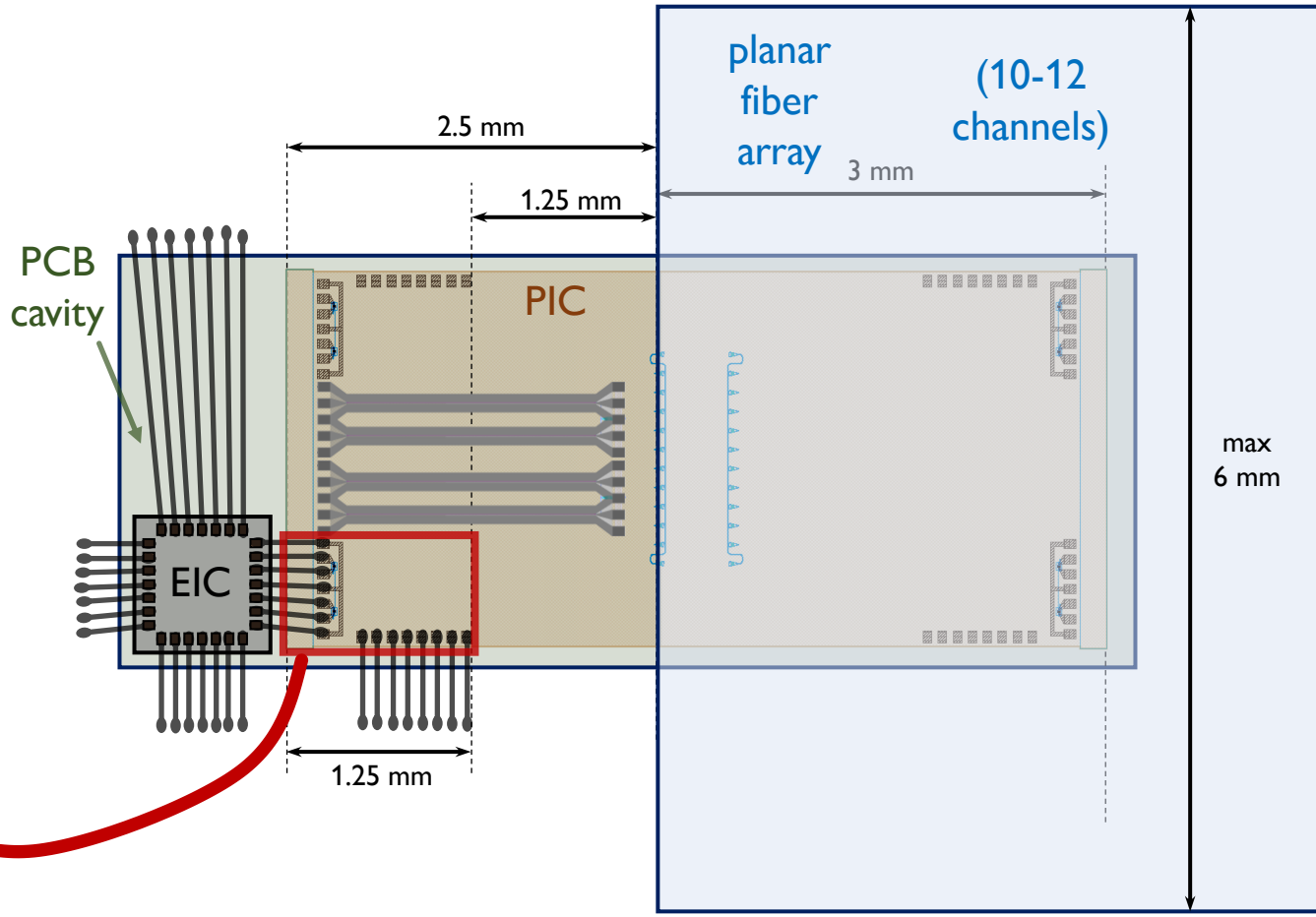




PIC v2 – Integration with EIC

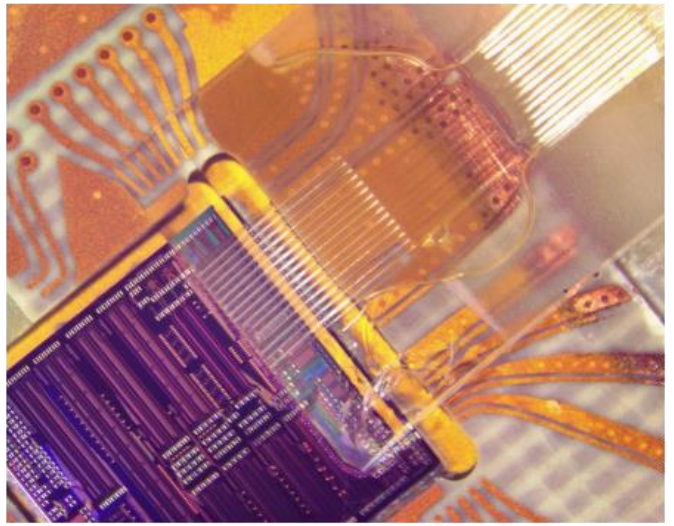
- 2D integration: wirebonded PIC and EIC in PCB cavities
- Short wire bonds for RF signal path
- Lateral DC supply/control signals

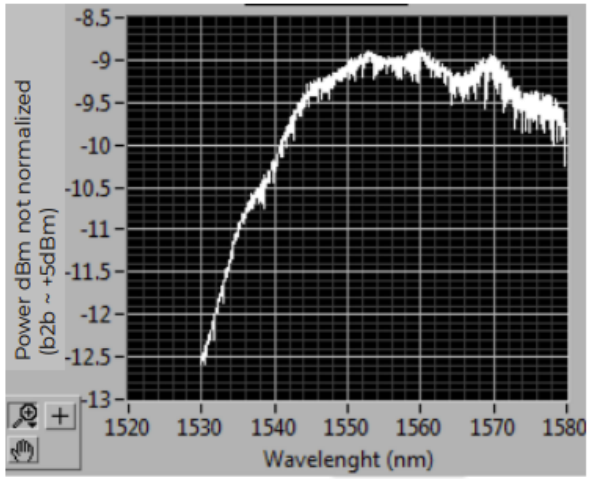


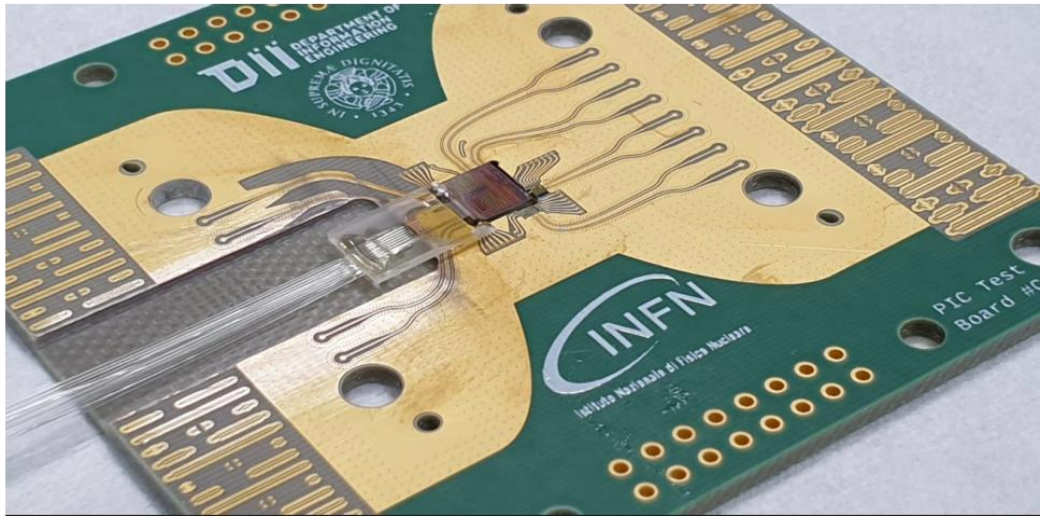


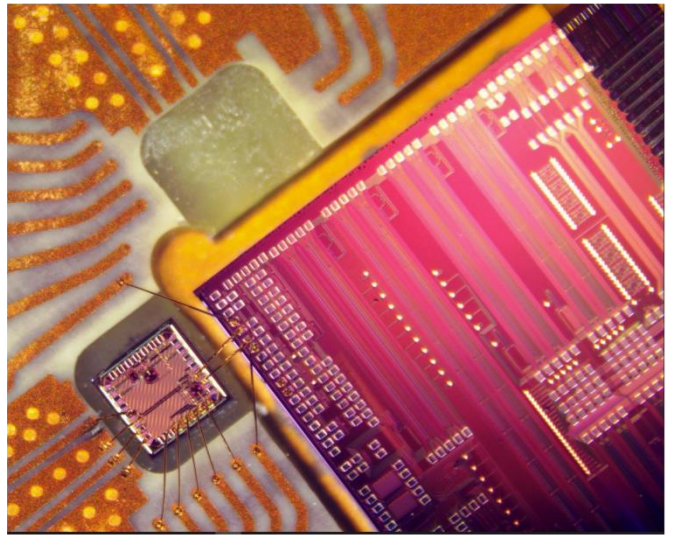
Packaged PIC-EIC on PCB - CamGraphIC

- PCB hosting imec's RM + driver 28nm finally packaged (the one with custom RM has been chosen to be tested on optical bench)
- Several issues with fiber arrays led to mechanical post-processing on PCBs and lengthy pigtailing process
- Low power coupling: -14 dBm at peak λ=1560nm



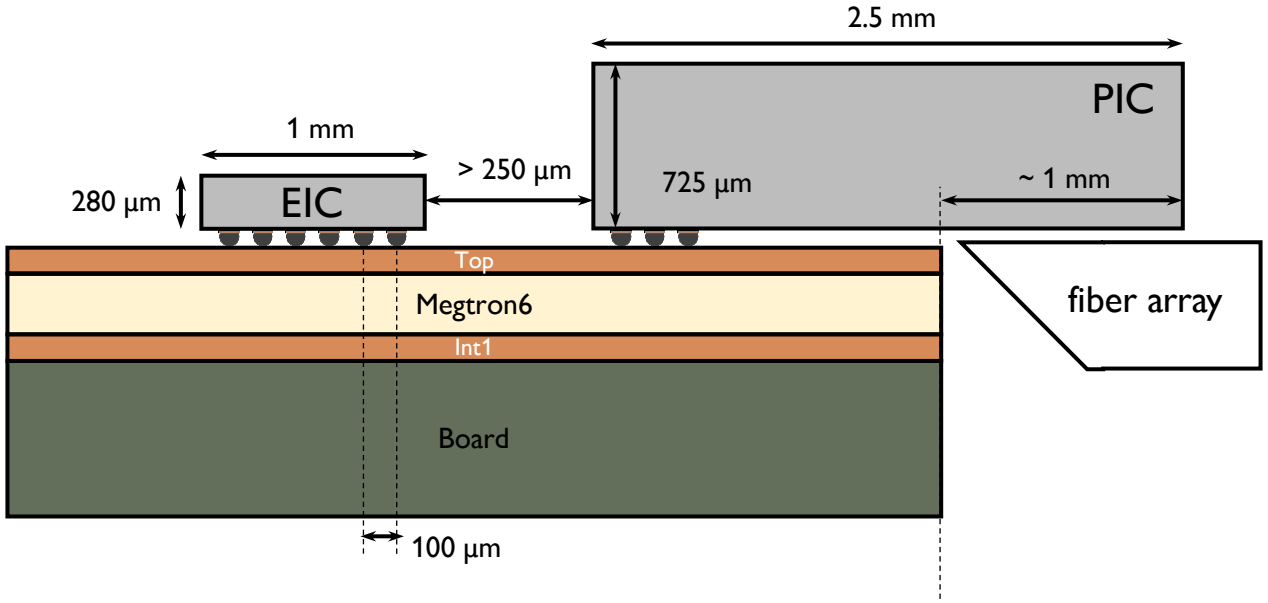




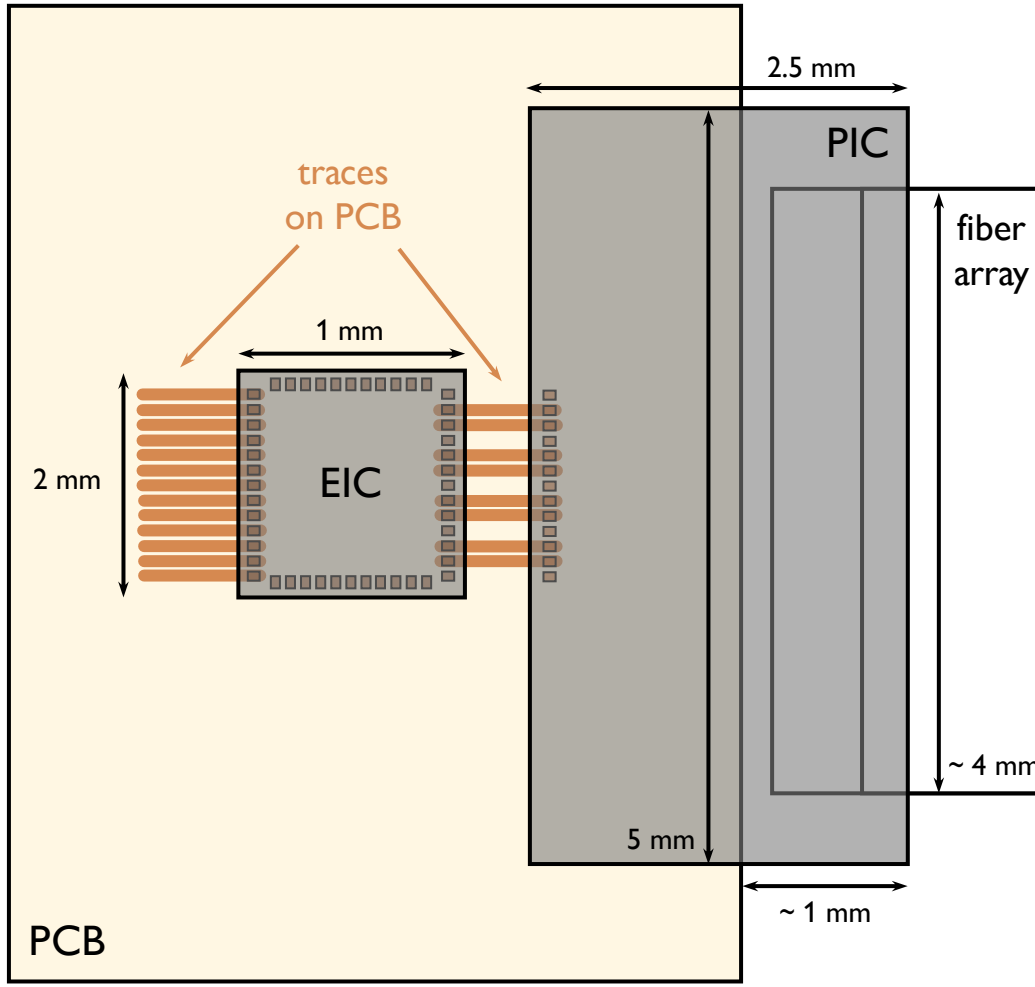


2.5-D Integration

Side view



Top view



- **Interposer-free** single-bumping flip-chip design
- Au stud-bumping (CamGraphic) + solder jetting (Valencia) + die attach (CamGraphic)
- Technology validation to be done on imec PIC**v1**
- Schedule?

DEPARTMENT OF INFORMATION ENGINEERING

UNIVERSITÀ DI PISA

Thanks for the attention

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Pisa, 12 October 2022