

FALAPHEL

General Meeting 12/10/2022

Gabriele Ciarpi



Outline



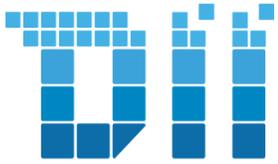
- Status of 25 Gb/s RR-driver in 28 nm (Heavy-Ions Test)
- Next submission is approaching (26 October)



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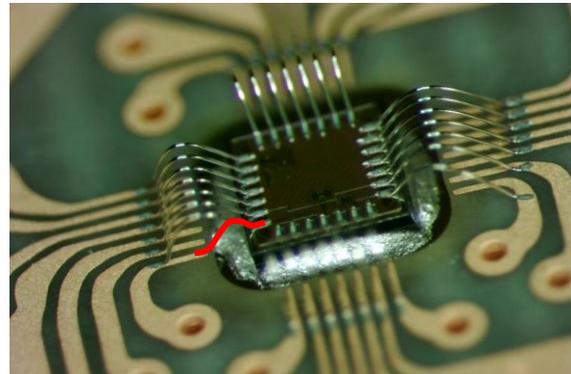
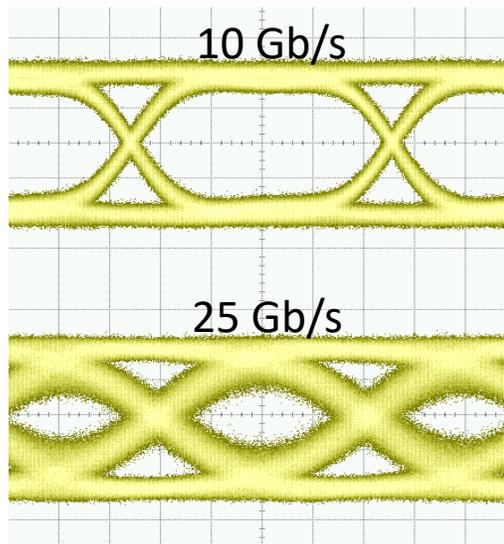


25 Gb/s Driver

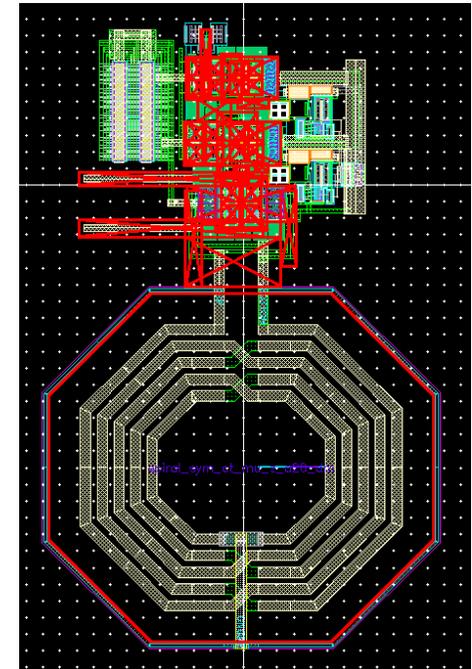


Driver for SiPh Ring Resonator operating up to 25 Gb/s:

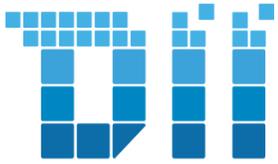
- 28 nm HPC technology
- 8 Metal technology
- CML stages
- Passive and Active Bandwidth enhancement techniques (inductors)



Only preliminary electrical tests
Radiation and optical tests: waiting



Layout of the 25 Gb/s driver in 28 nm



Heavy-Ions Test setup



Both chip hosting the PLL (65nm) and the driver (28nm) are mounted on testing boards with COTS components protected from ions by lead shield.

Test cases:

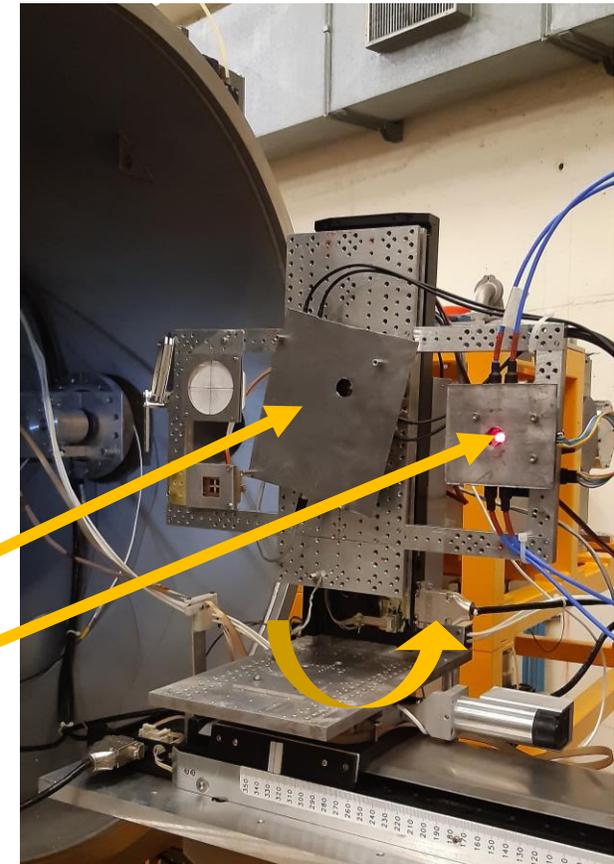
- Eight ion species (O, F, Si, Cl, Ni, Br, Ag, I)
- Four inclination angles between the flux direction and chip surface

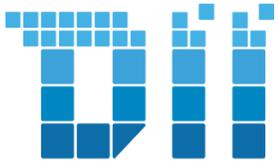
Setup Instruments:

- FPGA Kintex Ultrascale KCU116
- Oscilloscope Tektronix 23 GHz
- Multimeters/Power Supplier
- Cables

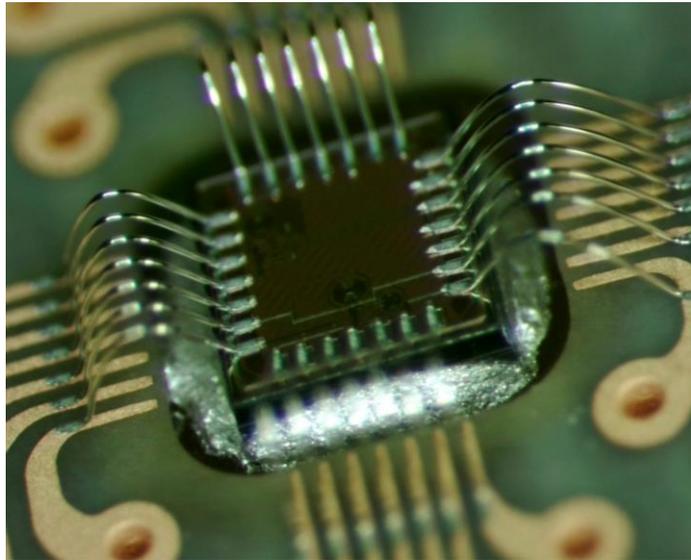


PLL device
Driver device





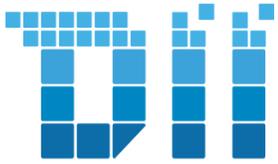
Test Chip2: Driver in 28 nm CMOS technology



Driver in TSMC 28 nm technology for electro-optical modulators able to sustain 25 Gb/s links

Chip connected to board using wire bonding only for electrical test. The electro-optical test are scheduled for the next months

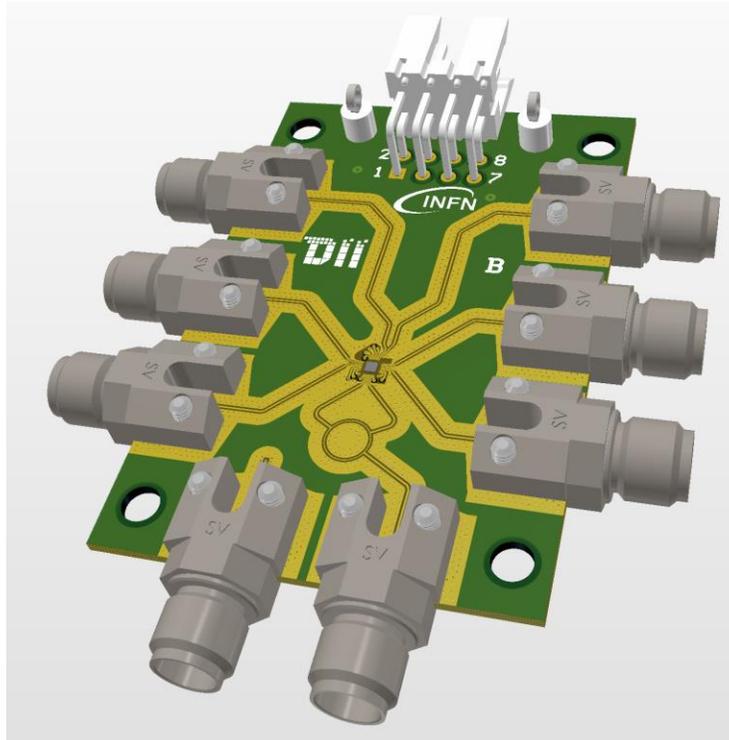
The driver is designed to work with a Ring-Resonator device at less than 1 mm. However, during the test, it was capable to drive a 50 Ω load ad a distance of about 2 m.



Custom devices

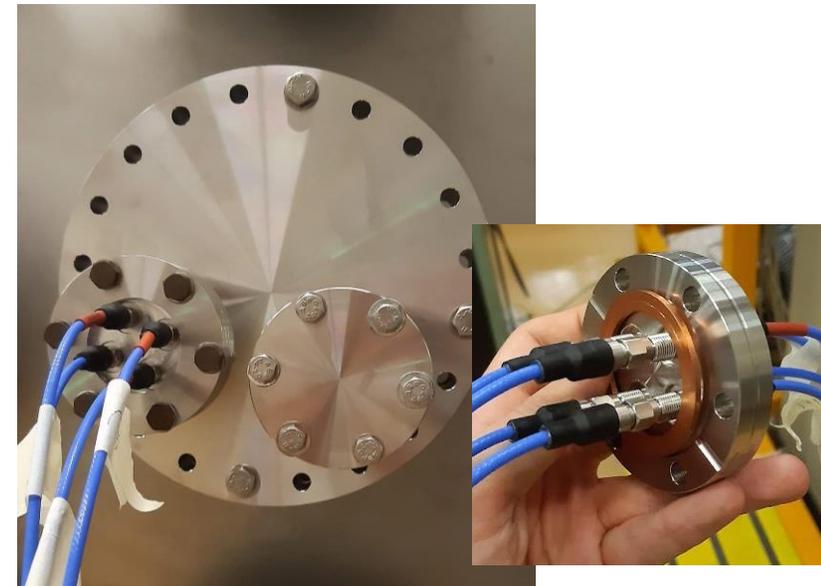


High-frequency High-speed testing board

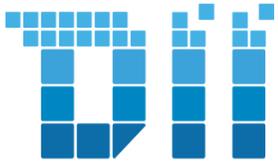


Custom board hosting the chip is designed to sustain 25 Gb/s links

Custom Flange



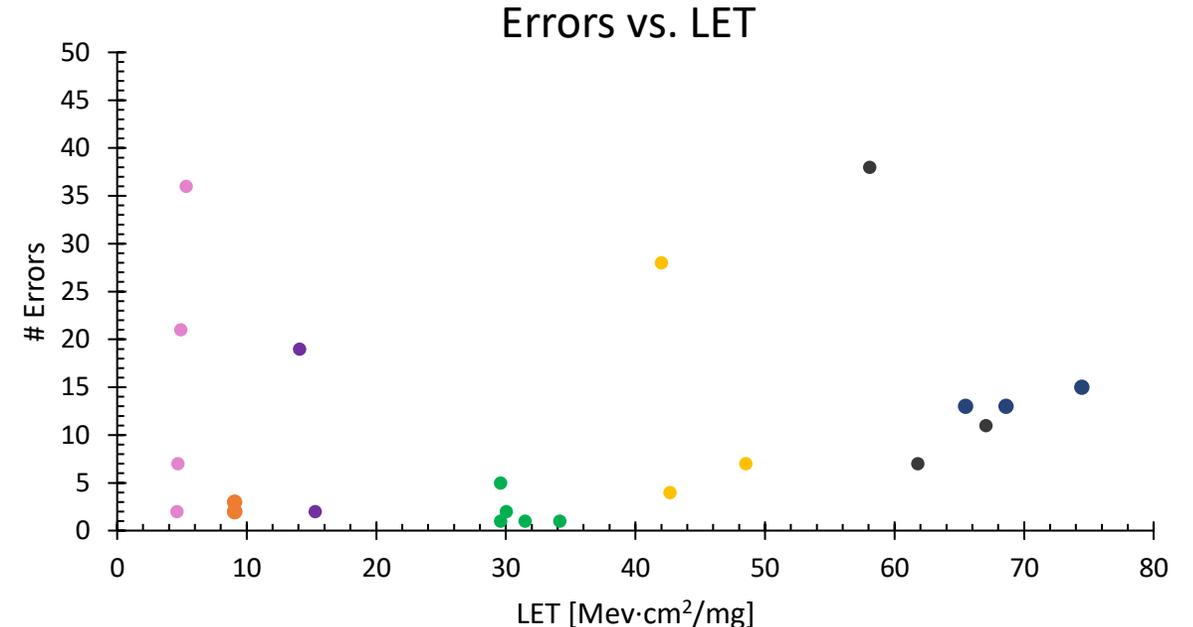
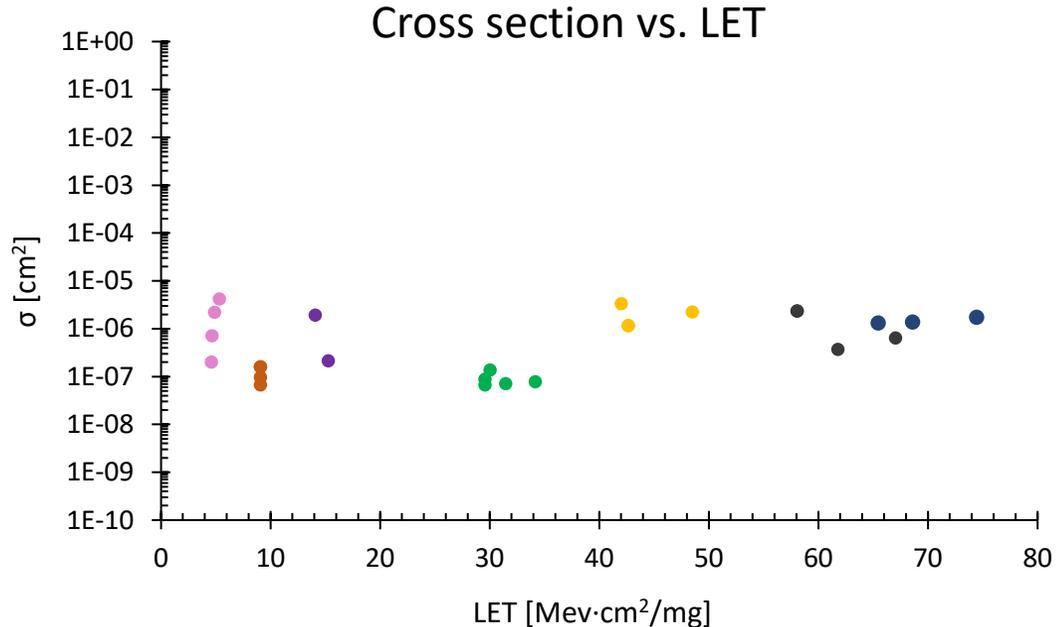
The custom flange is currently equipped with 4 SMK connector feeds able to sustain up to 40 GHz. Optical feeds will be added for next electro-optical tests



Driver Results



The driver was tested comparing the bit sequence transmitted and that received looking for flip bits (BERT). The test was performed in the worst possible condition for the driver (well worst than that planned): link speed of 25 Gb/s over 2 m cable with some connectors in a vacuum environment.



Test cases:

- Eight ion species (O, F, Si, Cl, Ni, Br, Ag, I)
- Four inclination angles between the flux direction and chip surface



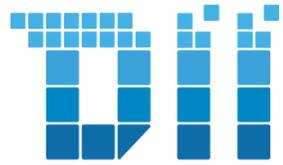
Test Conclusions



- The 28 nm driver shown to operate in worst condition (2 m cable and 50 Ω load) at 25 Gb/s.
- Because of the low error rate detected during tests run for tens minutes (time limited by schedule), statistical analysis of the data is not possible. However, in the worst case a cross-section less than $4 \cdot 10^{-6}$ could be considered.
- The chip hosts also custom ESD protections that could be sensitive to latchup problems. However, no latchup events occurred in whole chip during the tests.

Future works

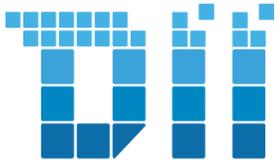
- Deeper data analysis.
- Expose both chips to X-ray to study their behavior for high cumulated dose (TID).
- Perform Electro-optical measurement of the driver also when exposed to heavy ions.



Outline



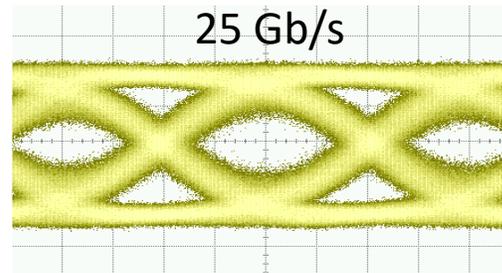
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Problem

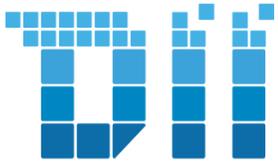


- Could we improve the driver performances?



- CERN is moving on 28nm 9M stack (no library inductors)

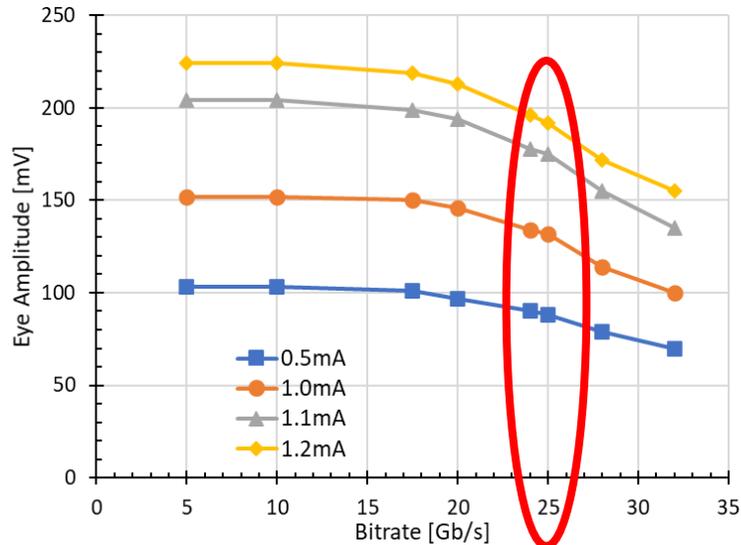
28 HPC+ (use MMWAVE PDK)	7M	lp7m_4x1y1z_alrdl	/
	8M	lp8m_5x2r_alrdl	lp8m_5x1z1u_ut-alrdl
		lp8m_5x2r_ut-alrdl	
	9M	/	lp9m_5x1y1z1u_ut-alrdl



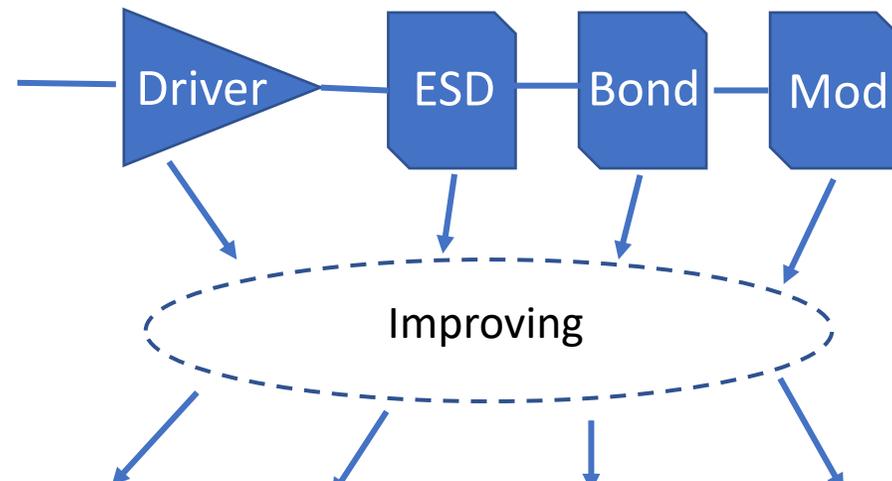
What can we do?



HPC driver results



How can we improve the driver bandwidth?
Which is the main limitation of driver bandwidth?



Inductive peaking

???

Custom Low Cap

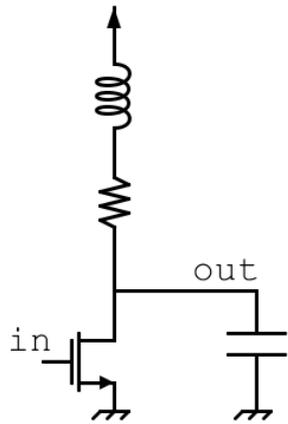
Short Wires 3D?

Ring Resonator



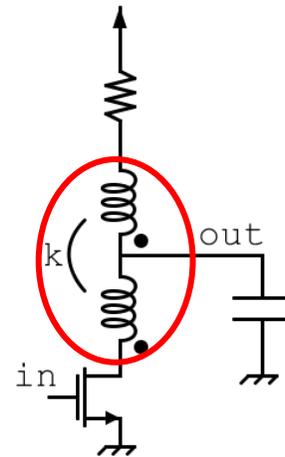


Other bandwidth extension techs



Inductive peaking

BWER ≈ 1.72

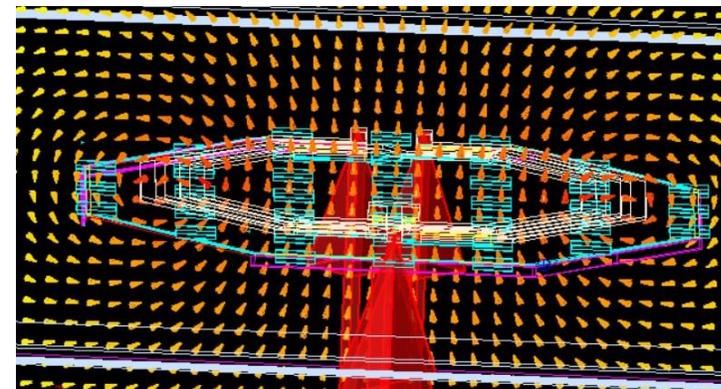


T-coil peaking

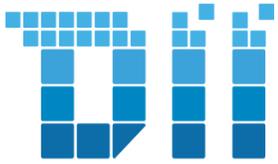
BWER ≈ 4.1

Custom design of T-coil transformer:

- First simulations of TSMC library inductors did not match the tech results (10% discrepancy in L and 55% discrepancy in Q)
- Now simulations match technology devices (less 10% discrepancy to be refined)
- Many TSMC inductors show a resonant frequency below 10-20 GHz
- Work in progress...



BWER: Bandwidth Extension Ratio

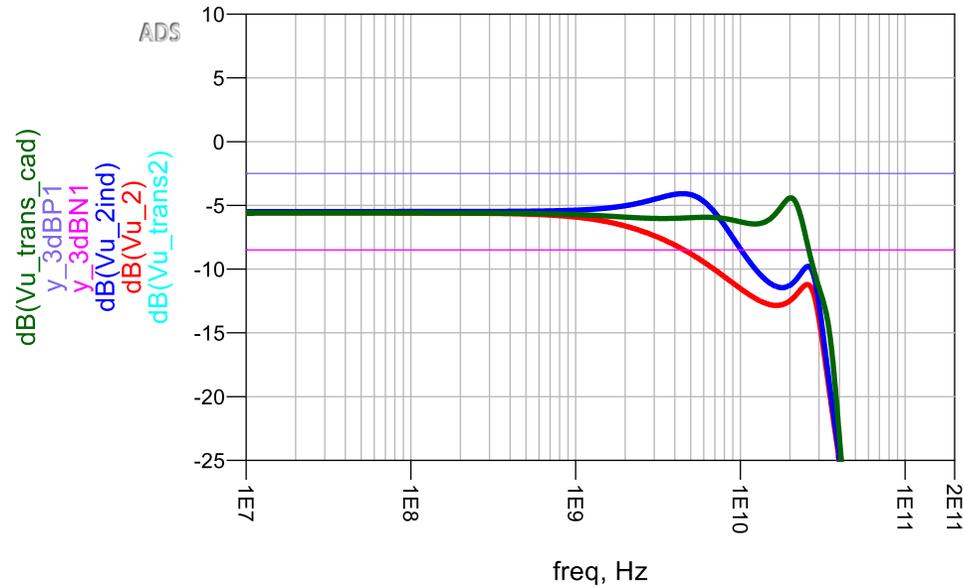


Which T-Coil?

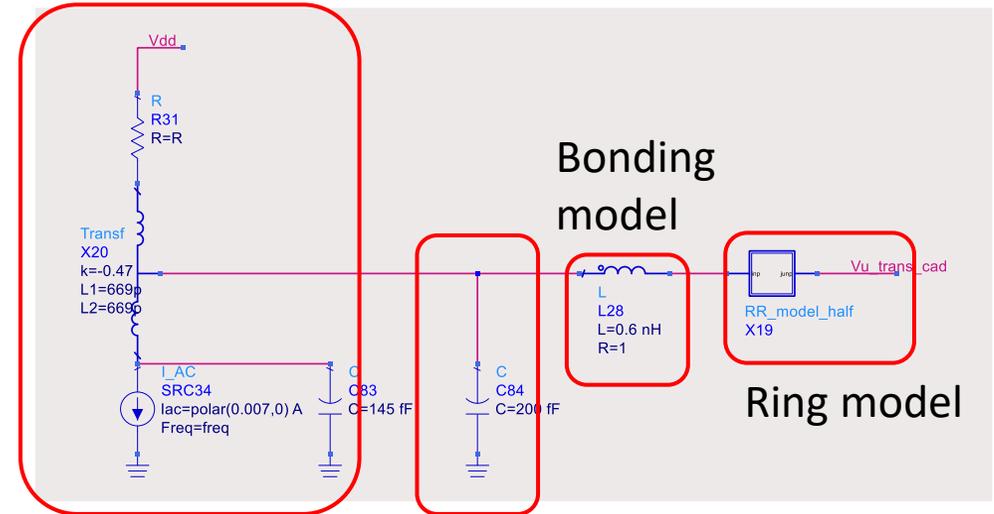


Tree grade of freedom in T-Coil:

- Inductance L1
- Inductance L2
- Coupling factor k



Driver model



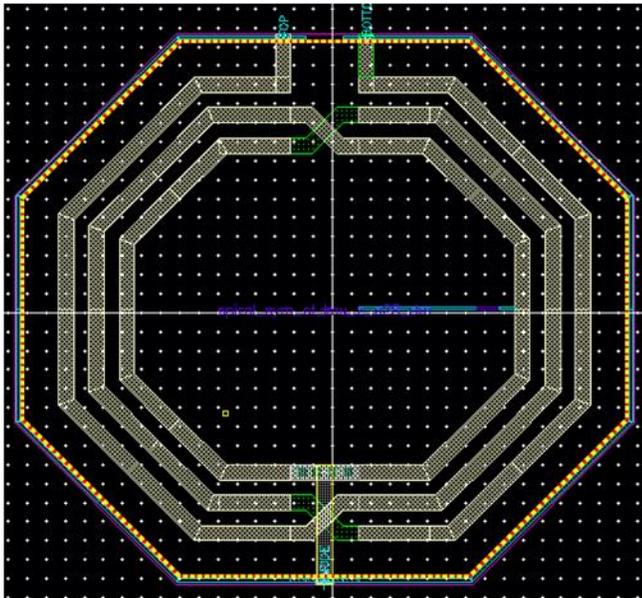
- No inductor
- Inductor Peaking
- T-Coil



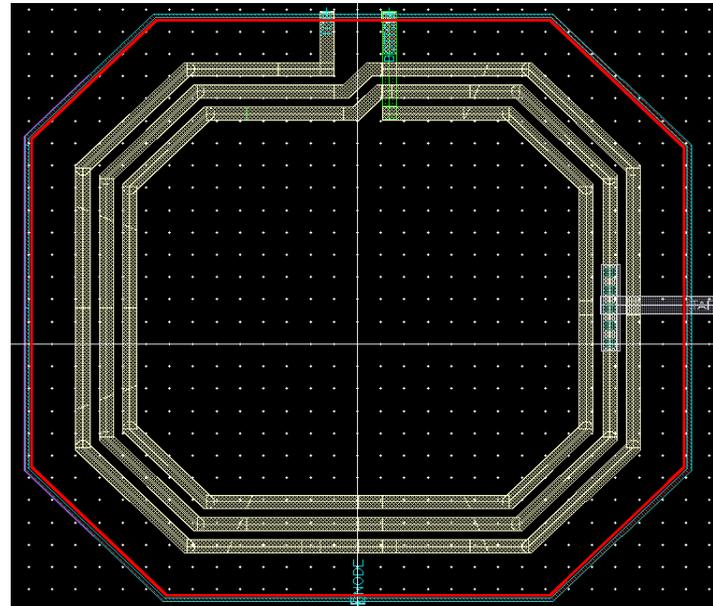
Are we able to design that T-coil?



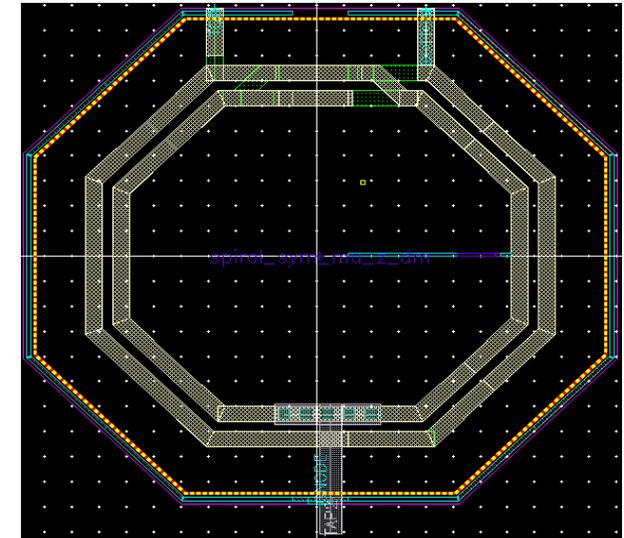
Symmetrical T-coil



Symmetrical T-coil, square shape



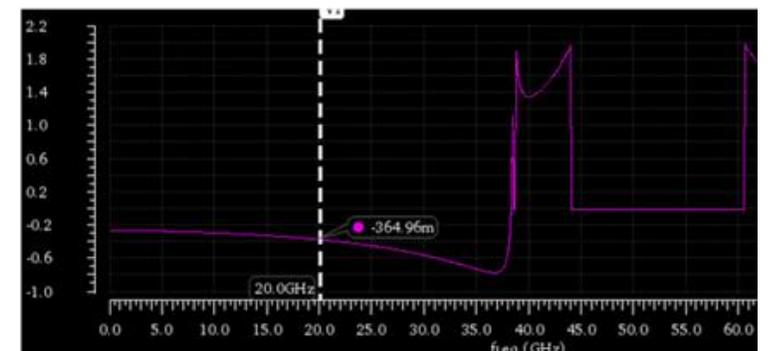
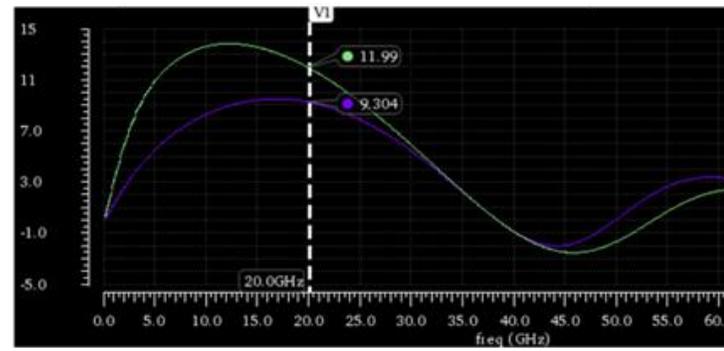
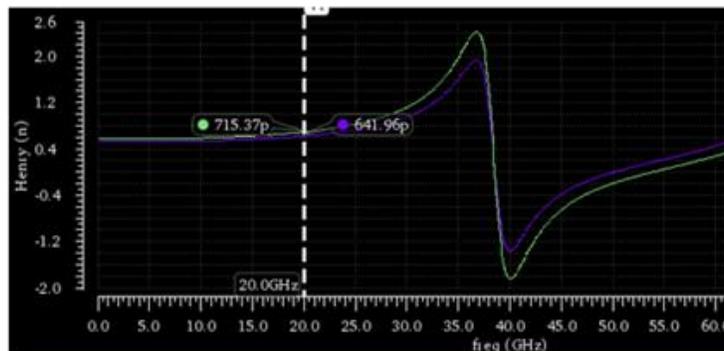
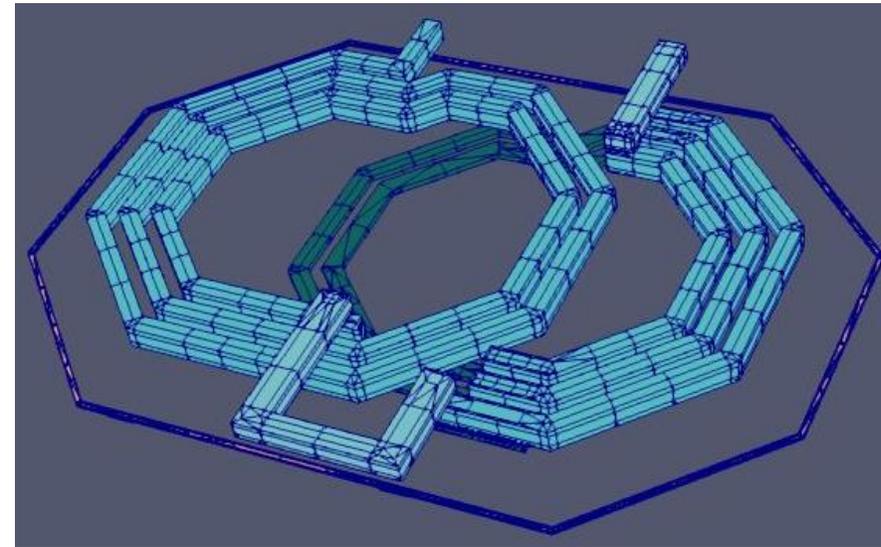
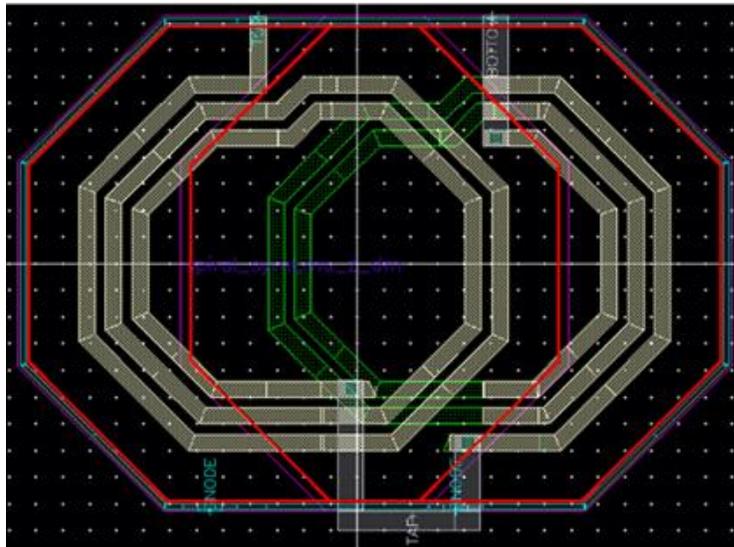
Stacked Symmetrical T-coil

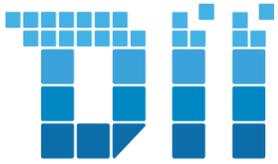


Different shape, different area, different performances but coupling factor too high for the model

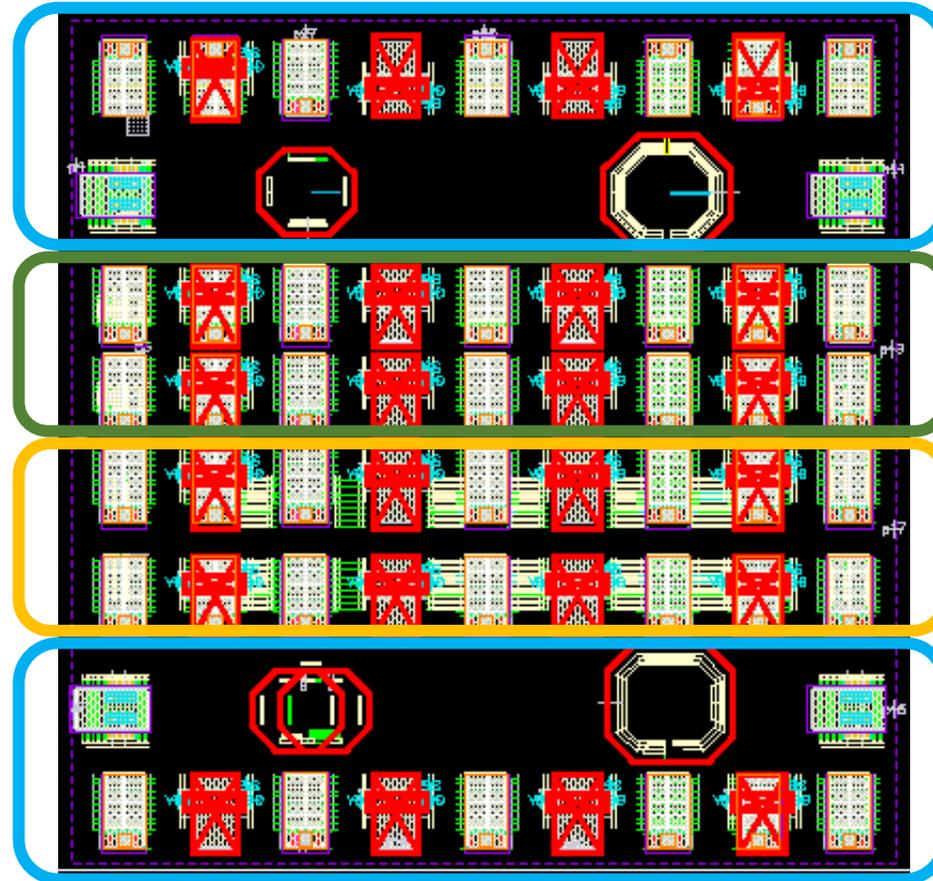


Solution for RR-driver model





Chip Submission

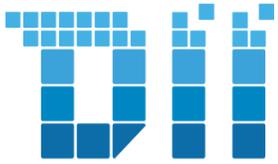


Inductor test

Some MOSFET test

ESD High-speed test

Inductor test



Thanks for your attention