Nuclear Physics Mid Term Plan in Italy

LNF session, 1-2 December 2022





Silicon detectors for high energy experiments



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Contents

Silicon sensors for tracking/vertexing detectors

- hybrid vs monolithic technologies
- planar vs 3D internal structure
- Iarge dimensions
- timing information

Detector integration

truly cylindrical detector



CMS Pixel sensor



ALPIDE MAPS



35 µm FBK LGAD

Silicon sensors for tracking/vertexing detectors



Hybrid vs Monolithic sensors

Characteristics of a sensor for tracking/vertexing

- » High space point resolution (~10 μ m)
- » High detection efficiency (~100%) and low fake-hit rate
- » Low material budget (< 0.1%)
- » Low power density (\rightarrow material budget) $\uparrow \downarrow$
- » Time resolution
- » Radiation hardness (HL-LHC ~2×10¹⁶ 1 MeV n_{eq}/cm²)

Hybrid sensor



- » pro optimisation of readout and electronics
- » pro large signal
- » cons large material budget
- » cons large power consumption

Monolithic sensor



- » pro standard CMOS readout integration
- » pro low material budget
- » pro low power consumption
- » pro low noise
- » cons small signal
- » cons limited radiation tolerant
- » cons slow (charge collection by diffusion)

Hybrid sensor

» State of the art for all LHC detectors during Run1 and Run2





3D sensors to improve radiation hardness

 » 3D sensors: depletion region grows laterally between the electrodes, whose distance is much smaller than the substrate thickness
→ depletion voltage dramatically reduced with respect to planar sensors

ATLAS Insertable B-Layer (IBL)





- » First 3D sensor application in ATLAS innermost layer (2014)
 - >200 V needed to fully deplete the sensor, while 1000 V for a 200 µm thick planar
- » During **HL-LHC** (2029) innermost tracking layers of ATLAS and CMS will have to cope with extreme radiation fluences (up to 2×10^{16} 1 MeV n_{eq}/cm^2)
 - → 3D sensors are good candidates but needs improvements: increased pixel granularity, reduced material budget and better geometrical efficiency

Monolithic Active Pixel Sensor (MAPS)

- » First application of MAPS technology in a collider environment for STAR HFT PXL detector @RHIC (2014) → Mimosa28
 - pixel pitch: 20.7 µm
 - matrix: 928 × 960 pixels
 - CMOS technology: twin well, 0.35 μm
 - readout: rolling-shutter fashion in 185.6 µs
 - power budget: 150 mW/cm²



J. NIMA 765 (2014) 177–182



- » MAPS development for ALICE ITS2 detector @LHC (2021) → ALPIDE
 - pixel pitch: 28 µm
 - matrix: 512 × 1024 pixels
 - CMOS technology: TowerJazz 0.18 μm
 - readout: continuous or triggered global-shutter (priority encoder)
 - power budget: 40 mW/cm²
 - several applications: sPHENIX, protonCT, calorimetry, test beam telescopes

Monolithic Active Pixel Sensor (MAPS)

- » Standard process, partially depleted epitaxial layer → doesn't allow full charge collection by drift, mandatory for more extreme radiation tolerance
 - Charge collection time < 30 ns
 - Operational up to 10¹⁴ 1 MeV n_{eq}/cm²
- » Modified process, toward fully depleted epitaxial layer (still keepings small collection electrode) → planar junction separated from the collection electrode in the epitaxial layer
 - Charge collection time < 1 ns
 - Operational up to 10^{15} 1 MeV n_{eq}/cm^2

» Modified with gap

- In modified process electric field in sensor reaches a minimum in the pixel corners → degraded timing resolution and efficiency loss after irradiation
- A gap in the deep n-implant increases the lateral electric field at the pixel borders
- » Modified process further pursued with MALTA, CLICpix, FastPix, ITS3...







Large dimensions sensors

- » Chip size limited by field of exposure of photolithography equipment (~20 x 20 mm²)
- » Stitching technique allow sensor size exceeding the photolithography limitations
 - Building blocks are integrated in the photolithography mask as different mask regions

Ę	Electronics	TR
L-drive	r by s PIXELS	R-drive
BL	Readout	BR

Sketch of an image sensor design



separately on the reticle

ΤL	Electronics	Electronics	Electronics	TR
L-drive	r by s PIXELS	r by s PIXELS	r by s PIXELS	R-drive
L-drive	<i>r</i> by <i>s</i> PIXELS	r by s PIXELS	<i>r</i> by <i>s</i> PIXELS	R-drive
BL	Readout	Readout	Readout	BR

Extending the size of the sensor beyond the reticle field of view

Tower Semiconductor Ltd, Stitching design rules for forming interconnect layers, US Patent 6225013B1 (2001)

Large dimensions sensors

ALICE ITS3 stitched sensor MOSS Monolithic Stitched Sensor Prototype



Timing information for 4D tracking



- » Low Gain Avalanche Diodes: additional moderately doped deep p-implant → In the region between this implant and the read-out electrode, the electric field is high enough for generating multiplication of the drifting electrons
- » Low gain allows segmenting and keeping the shot noise below electronic noise \rightarrow low leakage current
- »Could reach ~30 ps resolution (sensor) and 20-30 ps (ASIC)
- » New design, AC-LGAD architecture, uses charge sharing to achieve excellent time and spatial resolutions while reducing the number of channels by more than a factor of 10.



Timing information for 4D tracking

» At HL-LHC: average 1.6 collisions/mm

- trackers mostly mitigates pile-up effect, but still challenging, specially, in the forward region
- timing information (~30 ps) can be used to mitigate the effect of pile-up
- » ATLAS and CMS proposing timing detector systems for HL-LHC



ATLAS High Granularity Timing Detector (HGTD)



- » Future experiments like ePIC@EIC and ALICE3@LHC foresee a Time-Of-Flight PID detector, requiring ~20 ps timing resolution
 - LGAD technology is explored
 - Fully depleted MAPS also under investigation



Motivations

ALICE

» It is well known that thin silicon (<50 µm) can be bent without mechanical damages





- » Silicon makes only about 15% of total material
- » Irregularities due to support/cooling and overlap of adjacent modules
- Removal of water cooling
 - possible if power consumption stays below 20mW/cm²
- Removal circuit board (power+data)
 - **possible** if integrated on chip
- Removal of mechanical support
- **benefit** from increased stiffness by rolling Si wafers

How to realise it?

ALICE ITS3 implementation



Key ingredients

» Wafer-scale chips using stitching (~28x10 cm)

» Sensor thickness 20-40 µm

» Chips bent in cylindrical shape at target radii

» Si MAPS sensor based on 65 nm technology

» Carbon foam support structures

The whole detector will comprise six chips and barely anything else!

Beam pipe inner/outer radius (mm)	16.0/16.5		
IB Layer Parameters	Layer 0	Layer 1	Layer 2
Radial position (mm)	18.0	24.0	30.0
Length of sensitive area (mm)	300.0		
Pseudo-rapidity coverage	±2.5	±2.3	±2.0
Active-area (cm ²)	610	816	1016
Pixel sensor dimension (mm ²)	280 × 56.5	280 x 75.5	280 x 94
Number of sensors per layer		2	
Pixel size (μm²)	O (10 x 10)		

How to realise it?

EIC ePIC SVT implementation

Same ITS3 sensors dimensions but larger layer radii \rightarrow More sensors needed per layer

Key ingredients

» Wafer-scale chips using stitching (~28x10 cm)

- » Sensor thickness 20-40 µm
- » Chips bent in cylindrical shape at target radii
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R&D activities - ALPIDE chip bending

- » MAPS at thickness used in current detectors (~50 µm) are quite flexible
- » Large benefit from going even a bit thinner: the bending force scales with thickness to the third power
- » The breaking point moves to smaller bending radii when going thinner
- » Project goal thicknesses and desired bending radii are in a "not breaking" regime



R&D activities - ALPIDE chip bending



R&D activities - Wafer-scale silicon bending

» Developed procedure allows silicon bending in a repeatable reliable way » Bending tool: tensioned mylar foil wrapping around a cylindrical mandrel



R&D activities - Carbon foam characterisation

» Different foams characterised for machinability and thermal properties



Longerons and wedge ← ERG DUOCEL Support

Half-ring ← ALLCOMP LD Support + Cooling



Fleece to reduce glue



R&D activities - Carbon foam characterisation







- » Analysis of the kink angle distributions at the position of a scatterer
- » Material budget image: represents the widths of the scattering angle distribution of all particles traversing a given bin

R&D activities - Layer assembly procedure

» Different options under study (including vacuum clamping)» Currently working solution based on adhesive caption tape





R&D activities - Layer assembly procedure

» Different options under study (including vacuum clamping)» Currently working solution based on adhesive caption tape





Wedges replaced with half-ring due to excessive deformation from cylindrical shape



Detector integration: a truly cylindrical detector TOWARD FIRST WORKING LARGE DIMENSION SENSOR



Super-ALPIDE: 18 not diced ALPIDE chips

» Super-ALPIDE

- 18 not diced ALPIDE chips
- dimensions close to the ones for L0 sensor
- » Goals
 - verify bending tools for large-size working chips
 - verify mechanical support alignment tools
 - develop wire-bonding over bent surface tools
 - develop first bent flex prototype (for powering and data streaming)
 - assemble first working large dimension bent sensor



Detector integration: a truly cylindrical detector TOWARD FIRST WORKING LARGE DIMENSION SENSOR





Five main components

- super-ALPIDE
- support structures
- exoskeleton
- edge-FPC
- exo-FPC (not shown)

Detector integration: a truly cylindrical detector TOWARD FIRST WORKING LARGE DIMENSION SENSOR



R&D activities - Embedded MAPS

Idea and history

- I learned about a similar technique (and forgot about it inbetween), at FEE2014 (Argonne): <u>https://indico.cern.ch/event/276611/contributions/622863/</u> attachments/502969/694527/dulinski_FEE-2014.pdf
- This actually followed the SERWIETE idea: <u>https://arxiv.org/abs/1006.5424</u>
- To my knowledge it was not followed up much further, and had two difficulties:
 - redistribution layer on the chips was necessary since the chips had small pads
 - It required on AI metallisation (good for material budget, bad for using standard techniques)





Magnus Mager (CERN) | ITS3 WP4 | 28.04.2022 | 2

R&D activities - Embedded MAPS



Cross-section through one interconnection



arXiv:2205.12669v1



Summary

ECFA Detector R&D Roadmap (10.17181/CERN.XDPL.W2EX)

Solid State Detectors Task Force identified essential Detector R&D themes

- 1. Achieve full integration of sensing and microelectronics in monolithic CMOS pixel sensors
- 2. Develop solid state sensors with 4D-capabilities for tracking and calorimetry
- 3. Extend capabilities of solid state sensors to operate at extreme fluences
- 4. Develop full 3D-interconnection technologies for solid state devices in particle physics

First test submission: MLR1

- Main goals:
 - Learn technology features
 - Characterize charge collection
 - Validate radiation tolerance
- Each reticle (12×16 mm²):
 - 10 transistor test structures (3×1.5 mm²)
 - 60 chips (1.5×1.5 mm²)
 - Analogue blocks
 - Digital blocks
 - Pixel prototype chips: APTS, CE65, DPTS
- Submitted in December 2020
- Received diced chips in July 2021



APTS: Analogue Pixel Test Structure

- 6×6 pixel matrix
- Direct analogue readout of central 4×4 submatrix
- Two types of output drivers:
 - Traditional source follower (APTS-SF)
 - Very fast OpAmp (APTS-OA)
- AC/DC coupling
- 4 pitches: 10, 15, 20, 25 μm
- 3 process variations
- Presented results with ⁵⁵Fe source



APTS-SF:

Process modification reduces charge

sharing

- In standard process seed pixel takes ~50% of charge
- In modified process most of the charge is collected in one pixel
 Effect on efficiency and spatial resolution to be verified at beam test



APTS-SF: Substrate bias amplifies the signal

- Substrate bias lowers the node capacitance and increases signal amplitude
- Values as low as 2.2 fF were observed



APTS-SF: Charge collection vs. pixel pitch

- Charge collection doesn't seem to depend on pixel pitch
- Remarkable result to be confirmed by beam test
- If confirmed another way to reduce power consumption



APTS-OA: Process modification reduces charge collection time

- Fast readout allows to estimate the charge collection time via signal fall time
- In modified process the charge is collected faster



DPTS: Digital Pixel Test Structure

- 32×32 pixel matrix
- Asynchronous digital readout
- Time-over-Threshold information
- Pitch: 15×15 μm²
- Only "modified with gap" process modification
- Tunable Power vs Time resolution



Non irradiated DPTS: Excellent efficiency and low fake hit rate



Irradiated DPTS (10¹³ n_{eq}): Larger fake hit rate, but has margin



Irradiated DPTS (10¹⁵ n_{eq}): Efficient at 20 °C with limited fake hit rate



DPTS: Spatial resolution ~5 µm



DPTS: Temporal resolution ~7 ns





Service pigtail adds a challenge to the assembly sequence



NPMTP22 | 1-2 December 2022 | Domenico Colella



ALICE 2 ITS2 for LHC Run 3





ITS2 installed and under commissioning



ITS2 will provide unprecedented performances \rightarrow pointing resolution: 15 µm at p_T of 1 GeV/c \rightarrow tracking efficiency: above 90% for p_T > 200 MeV/c



Improved pointing resolution and tracking efficiency for low momenta (×2 at all p_T)

ALICE Simulation

Study of the enhancement of charm quarks in heavy-ion collisions



MLR1 SUBMISSION AND TEST + ER1

» MLR1 is the first submission in the TowerJazz 65 nm technology

- scoped within CERN EP R&D WP1.2, but significant drive from ITS3
- this technology will allow to build larger sensors (300 mm wafers)
- » More than just "first test structures"
 - transistor test structures
 - analog building blocks (band gaps, LVDS drivers, etc.)
 - various diode matrices (small and large)
 - · digital test matrices
 - Essentially covers the initial goals of MPW1 and MPW2
- » First wafers received
 - · laboratory characterisation ongoing
 - test beam campaign (PS, SPS and DESY) in Oct-Dec 2021
 - · characterisation of bent test structure
- » ER1 Stitched Sensor prototype
 - Key requirements and architectures defined (sensor, primary features, dimensions and floorpan, powering scheme, I/Os and global busses)
 - Mock submission by end of November



Chip design

expect O(300) dies per wafer





- » Central barrel ($-0.9 < \eta < 0.9$)
- » Muon spectrometer ($-4.0 < \eta < -2.5$)
- » Forward detectors: trigger, centrality, luminosity, reaction plane
- » Tracking and PID per large kinematic range
- » High resolution vertex reconstruction

LHC Run 1 and Run 2 data taking			
Colliding System	Year(s)	√S _{NN} (TeV)	
Pb-Pb	2010-2011 2015-2018	2.76 5.02	
Xe-Xe	2017	5,44	
p-Pb	2013 2016	5.02 5.02, 8.16	
рр	2009-2013 2015, 2017 2015-2018	0.9, 2.76, 7, 8 5.02 13	







Shutdown/Technical stop Protons physics Ions Commissioning with beam Hardware commissioning/magnet training

Data taking strategy

» Record large minimum-bias data sample

- → read out all Pb-Pb interactions up to maximum LHC collision rate of 50 kHz (was ~1 kHz in the central barrel)
- \rightarrow increase Pb-Pb Run 2 minimum-bias sample by factor 50-100

Colliding System	Integrated luminosity	Comment
Pb-Pb @ $\sqrt{S_{NN}}$ = 5 - 5.5 TeV	13 nb ⁻¹	Plus pp reference data
p-Pb @ √S _{NN} = 8 - 8.8 TeV	0.6 pb ⁻¹	Plus pp reference data
pp @ √S = 14 TeV	200 pb ⁻¹	Focus on high multiplicity and rare signals

» Improve tracking efficiency and resolution at low- p_T

- \rightarrow increase tracking granularity
- \rightarrow reduce material thickness

» Preserve Particle IDentification (PID)

 \rightarrow consolidate and speed-up main ALICE PID detectors

Programme is presented in CERN Yellow Report (<u>https://arxiv.org/abs/1812.06772</u>) Future high-energy pp programme with ALICE (<u>https://cds.cern.ch/record/2724925/files/ALICE_HEpp_PublNote.pdf</u>) <u>LHC schedule</u>



New Inner Tracking System (ITS 2)

Based on the ALPIDE Monolithic Active Pixel Sensor

- » In-pixel amplification, shaping discrimination and Multiple-Event Buffers (MEB)
- » In-matrix data sparsification
- » High detection efficiency (>99%) and low fake-hit rate (<< 10⁻⁶ /pixel/event)
- » Radiation tolerant:
 - > 270 krad TID
- > 1.7×10¹² 1 MeV/n_{eq} NIEL
- » Low power consumption ~40 mW/cm²

	ITS (Run 1/Run 2)	ITS 2
Number of layers	6 (pixel, drift, μ strip)	7 (MAPS)
Rapidity range	η < 0.9	η < 1.3
Material budget per layer	1.14% (SPD)	0.35% (IB)
Distance to interaction point	39 mm	22 mm
Pixel size	50 x 425 μm²	29 x 27 µm²
Spatial resolution	12 μm x 100 μm	5 µm x 5 µm
Max. readout speed Pb-Pb	1 kHz	100 kHz





New Inner Tracking System (ITS 2)







Performance



Integrated Online-Offline system (O²)



Readout upgrade for other detectors



» Continuous readout

- · Upgrade of all detector readout boards
- Heartbeat from CTP
- Timeframe (instead of events)

» Multi-step reconstruction chain

• Detector \rightarrow FLP \rightarrow EPN \rightarrow Storage

» Synchronous processing (EPN farm)

- Data volume reduction (factor 35)
- Online calibration
- · Clusterization and tracking (using GPUs)
 - \rightarrow Compressed Time Frames (CTF)

» Asynchronous processing (EPN farm/T0/T1)

- Final refined reconstruction
 - \rightarrow Analysis Object Data (AOD)



