Characterization of Josephson junctions for JTWPA at T = 0.3K

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DARTWARS

Detector Array Readout with Traveling Wave AmplifieRS

INFN

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DI RICERCA METROLOGICA

Outline

- Experimental setup
- Samples description
- Preliminary results
- Conclusions and outlook

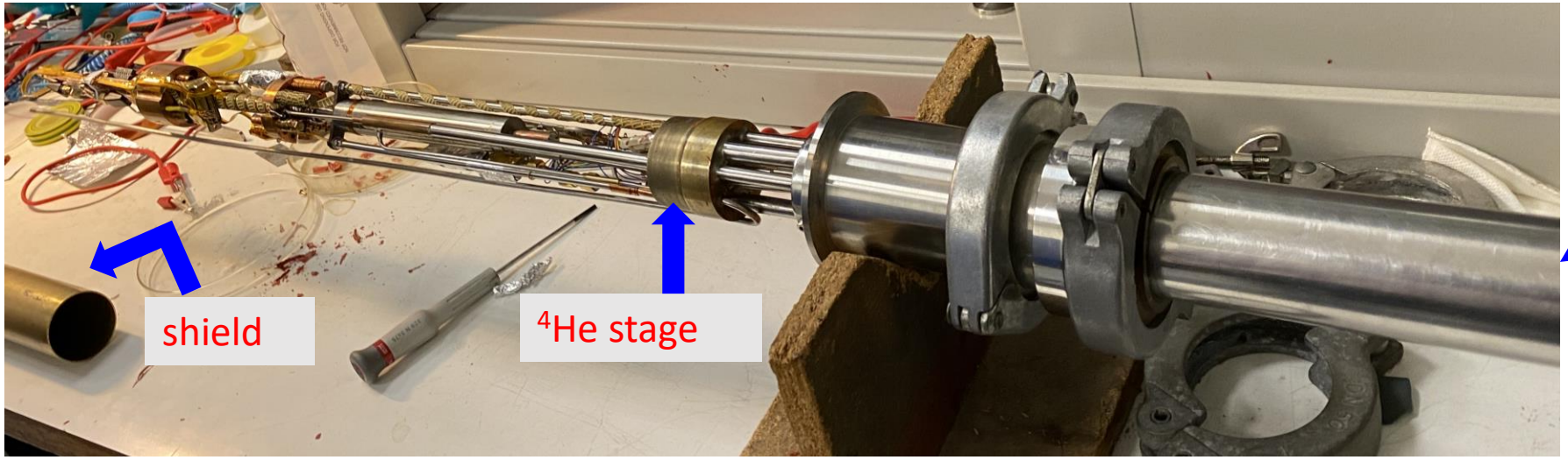
Oxford Heliox VL ^{3}He cryostat

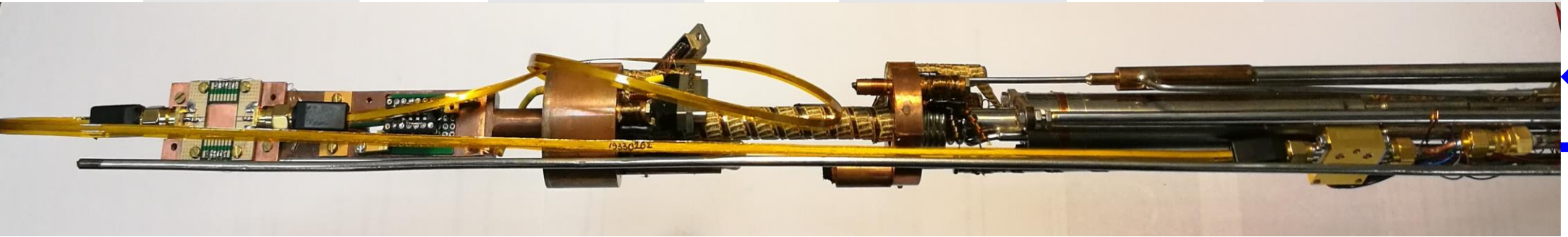
Base T = 245mK Cooling Power = 40 µW at T < 290 mK

Hold time = several hours Recycle time = 1h

OK for testing Al based junctions

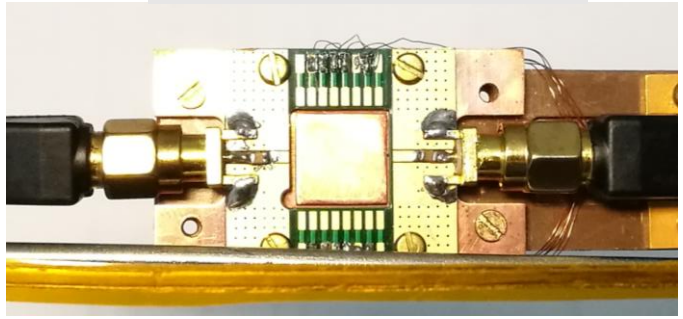
Needed adaptations for MW signals

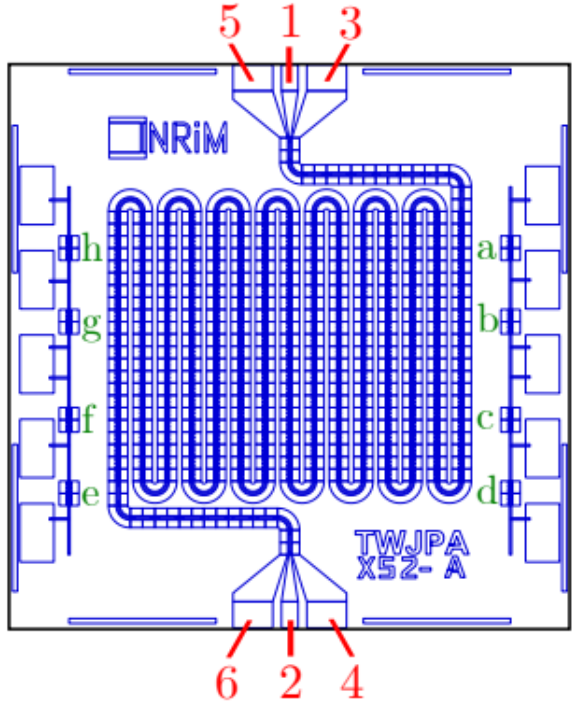




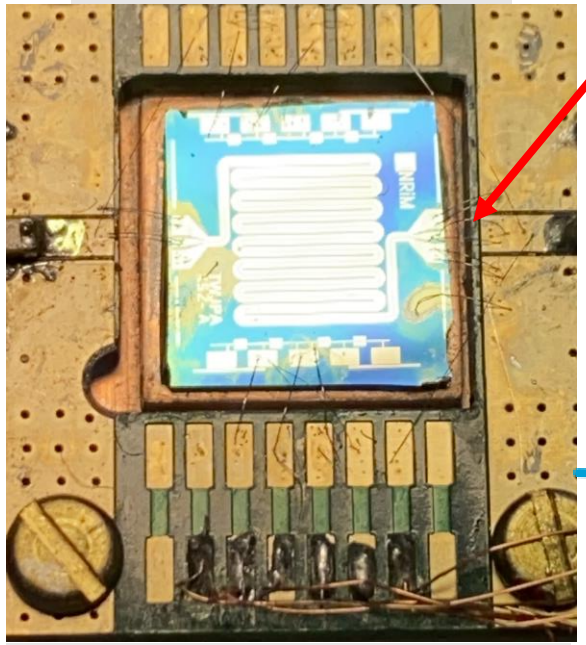
DC Setup

Sample holder





TWJPA X52-A



Ultrasonic bonding

RF out

RF in

PC

DAC/ADC

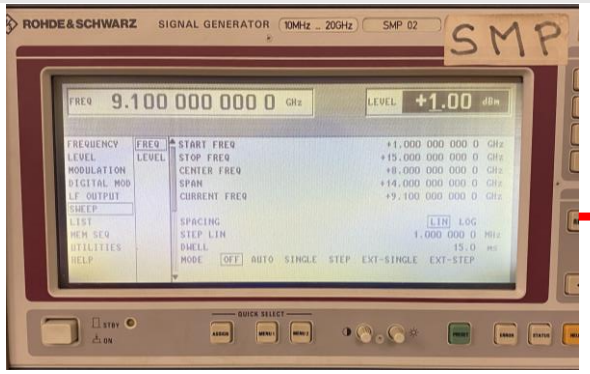
DC bias and JJ test lines

Filtering and grounding box

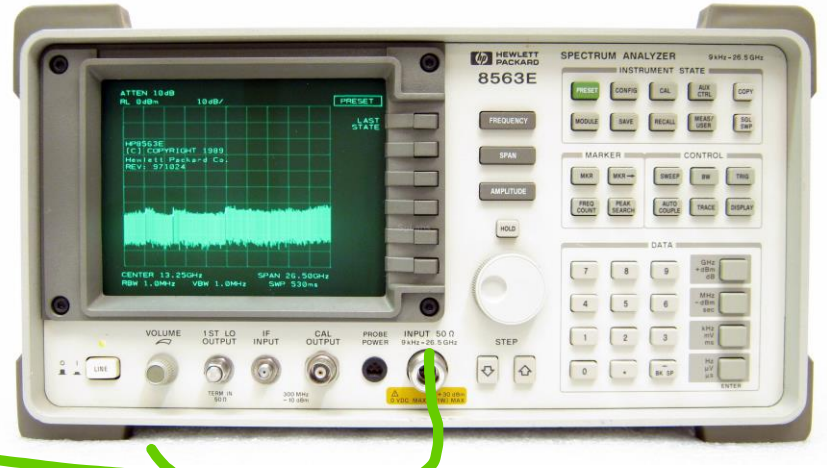
Low Noise DC readout

RF setup

0-20 GHz generator (Pump)

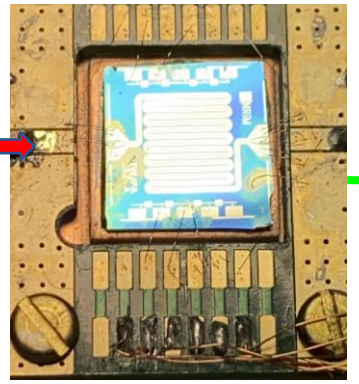


20 dB dir coupler

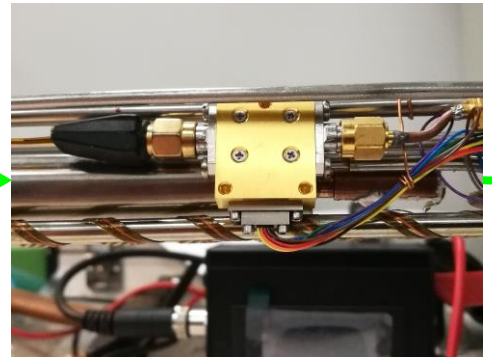


0-19 GHz generator (Signal)

0-10 dB var attenuator



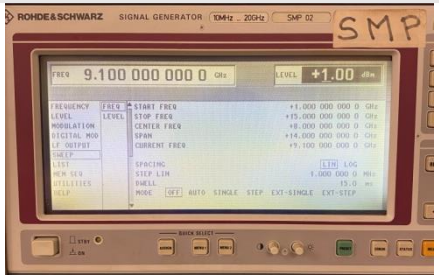
TWJPA (0.3 K)



Cryogenic amplifier (4.2 K)

System calibration

0-20 GHz generator (Pump)

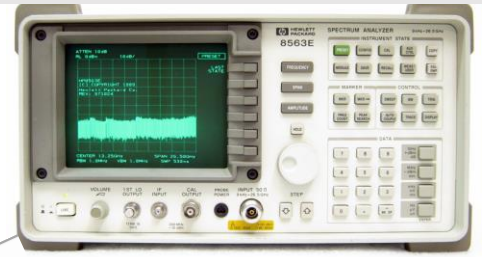


20 dB attenuator

20 dB dir. coupler

Heliox ^{3}He insert

9 kHz -26.5 GHz spectrum analyzer

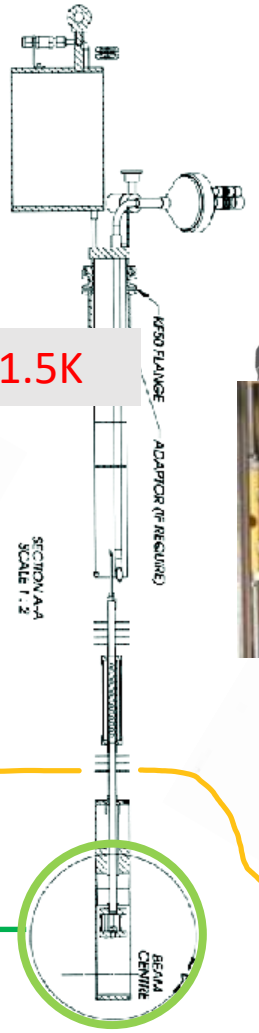


RF in

RF out

0-19 GHz generator (Signal)

0-10 dB var. attenuator



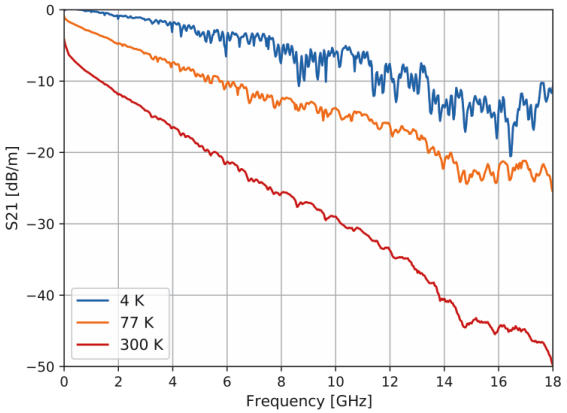
T = 1.5K

T = 4.2K

Cryogenic Low Noise Amplifier
LNF 0.3-14 GHz Gain ~36 dB

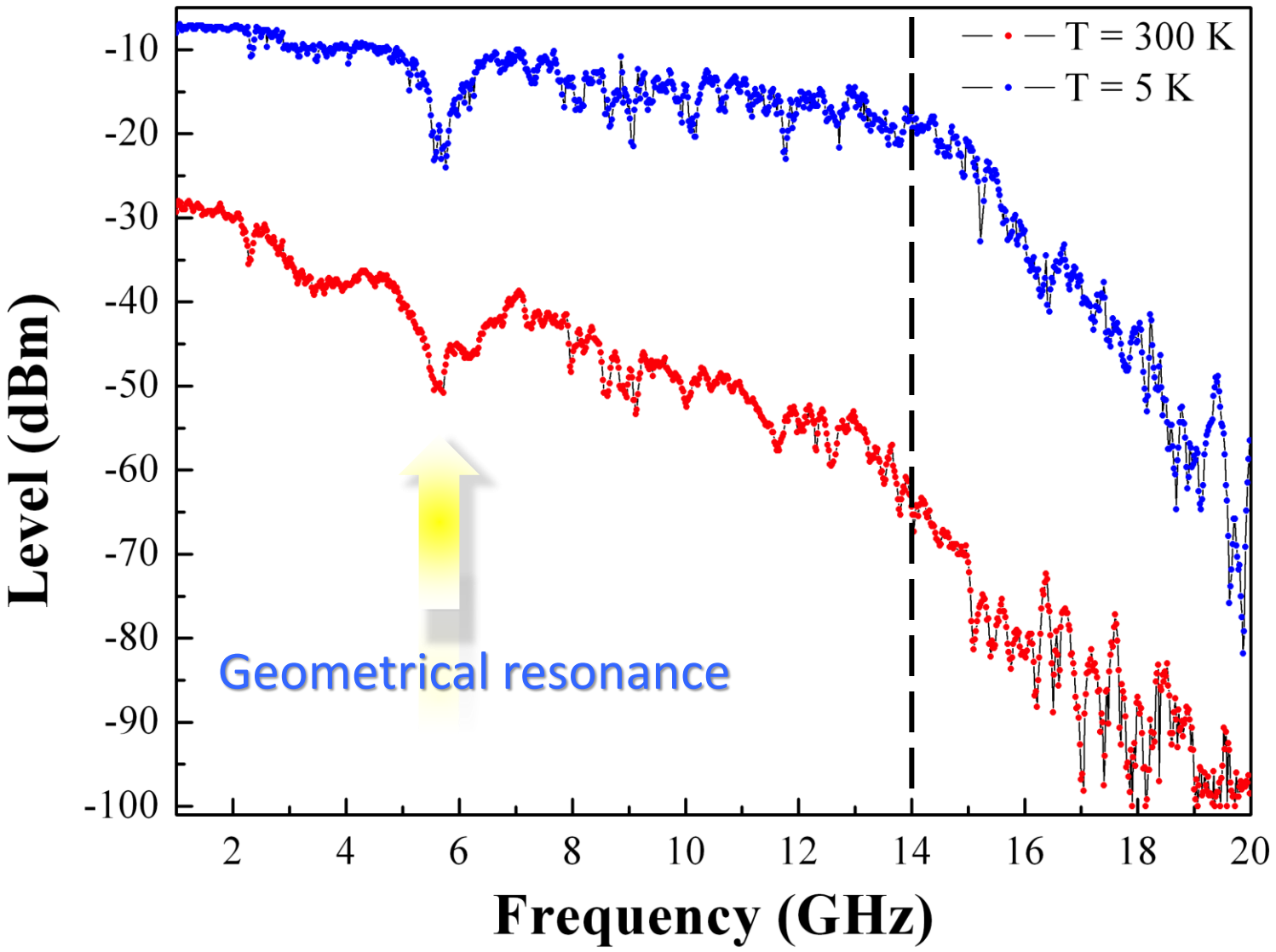
Cri/oFlex 2 (CF2)

Cri/oFlex 2 (CF2)



TWJPA (0.3 K)

IN/OUT measurement of frequency response with sample bypassed



Input Power = -30 dBm
Amplifier gain 40 dB

Results:

- Overall coax lines attenuation@ 1GHz = 17 dB
- Beside a geometrical resonance at 6 GHz, the frequency response decreases linearly of 10 dB from 1 to 14 GHz (the amplifier bandwidth)

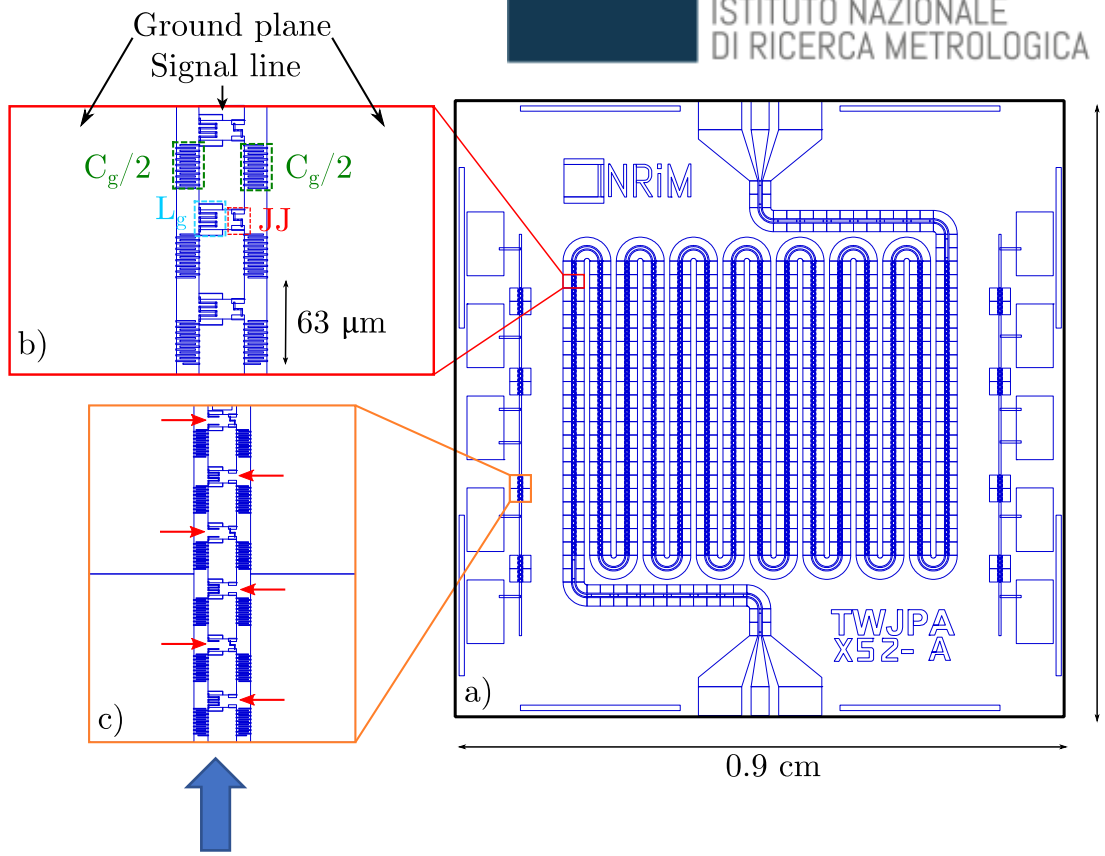
JTWPA: samples description

Design and production by the Istituto Nazionale di Ricerca Metrologica (INRiM, Turin, Italy)

Two designs of JTWPA have been realized:

gen.1 (X_52) is made by a repetition of N = 990 elementary cells, cell size 63 µm, total length ≈ 6.25 cm. Each cell is made by a parallel of a JJ and an inductor (RF SQUID).
Substrate: p-doped, 100 oriented, Si/SiO_2(300nm)
The geometry is defined by a single-step (EBL) process. (LONG PROCESS)
JJs: Al(30 nm)/Al-Ox/Al(80 nm) deposited by a ultra-low pressure electron beam evaporator, equipped with a tiltable sample holder that ensure the possibility to create exploiting the Niemeyer-Dolan technique.
Design parameters:

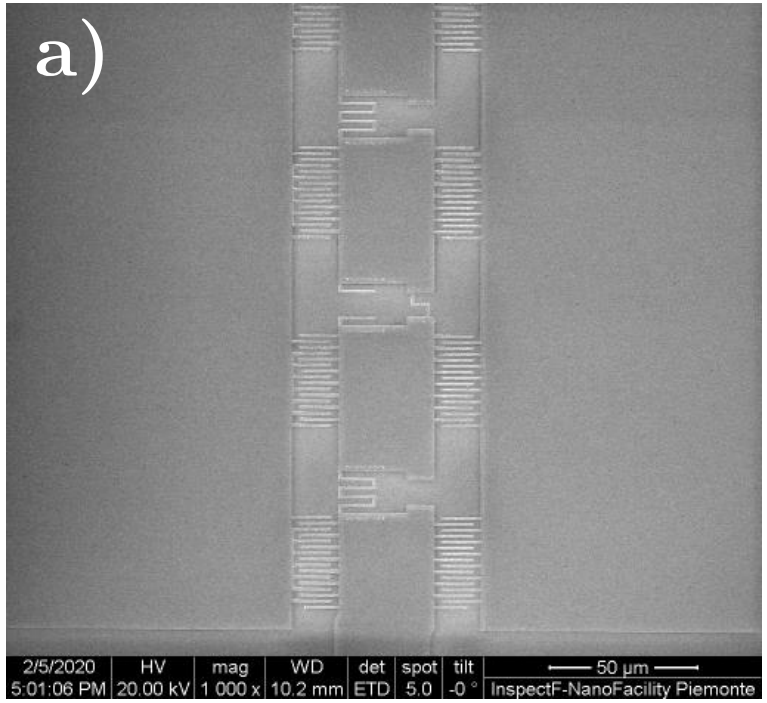
- Critical current of Josephson junctions: I_C = 2 µA
- Josephson junction capacity: C = 200 fF
- Inductance of the Josephson junction at the working point: L_J = 258.5 pH
- Geometric inductance: L_g = 120 pH
- Plasma frequency: ν_p = 38 GHz
- Resonator quality factor: Q = 100

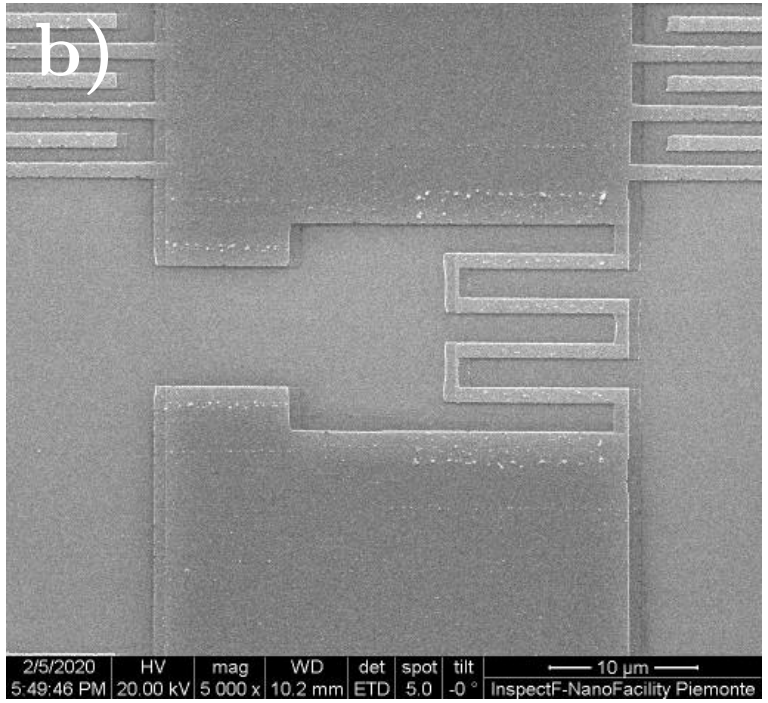


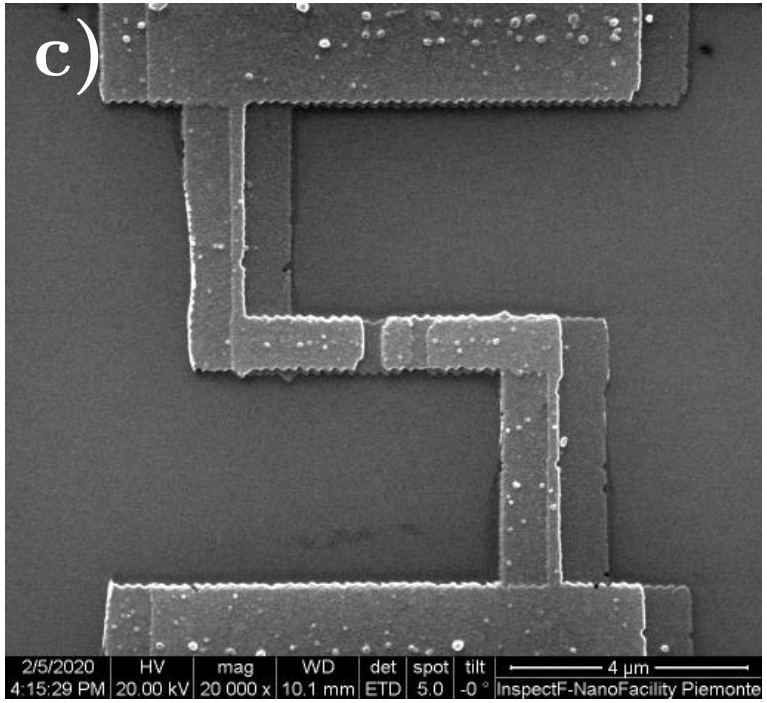
8 test units (PCU) are present on both sides of the chip for JJ characterization

JTWPA: sample fabrication process

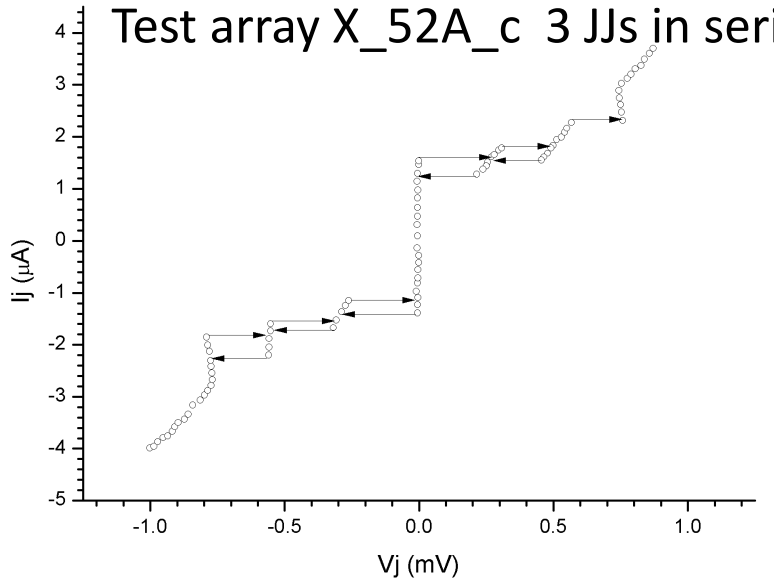
The **test units** present on the JTWPA chip X_52, figure a), reproduce the JTWPA cells but without the RF SQUID structure: in each cell is eliminated alternatively the JJ , figure b), or the inductor figure c).







DC Measurement Results



CHIP X_52

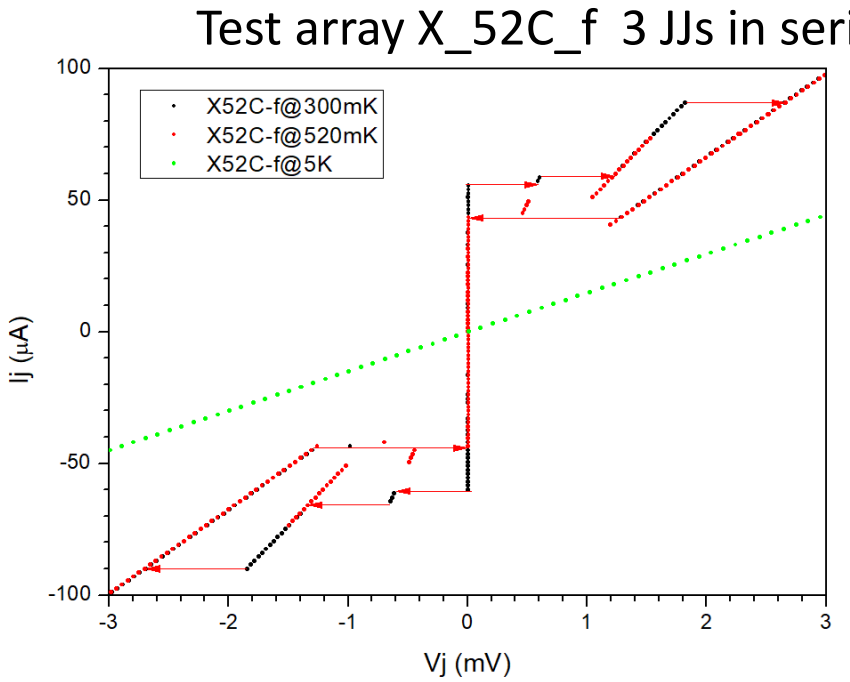
DC characterization of test structures

X_52A_c:

- T = 0.350 K
- I_c = 1.6 μA, 1.9 μA and 2.3 μA
- R_n = 237 Ω → 79 Ω/junction

X_52A_d:

- Short



X_52C_f:

- IV critical currents are too high at 300 mK, probable short in the tunnel barrier

The measurements of other test junction in the same chip give open or short circuits, due to damaged JJs. The damage of the JJs is most probably due to ESD discharges during the chip mounting procedure (bonding, chip and sample holder handling). **This procedure has to be revised to eliminate the problem**

JTWPA: samples description

gen 2 chips

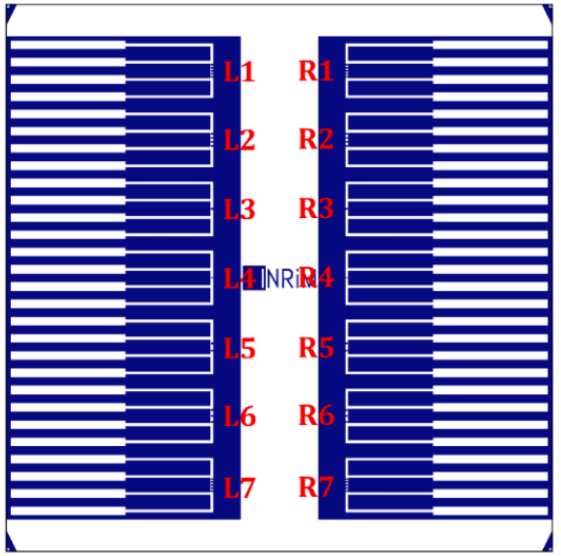
ID_013_01 JTWPA
Complete redesign of TW
Added lumped resonant structure for resonant phase matching
No EBL lithography (faster turnaoround)
Added Ti underlayer for base electrode to improve surface uniformity

SUB_02 Test chip

Test chip with several JJ arrays with 1 to 5 junctions
JJ resistance measured at MIB at room temperature

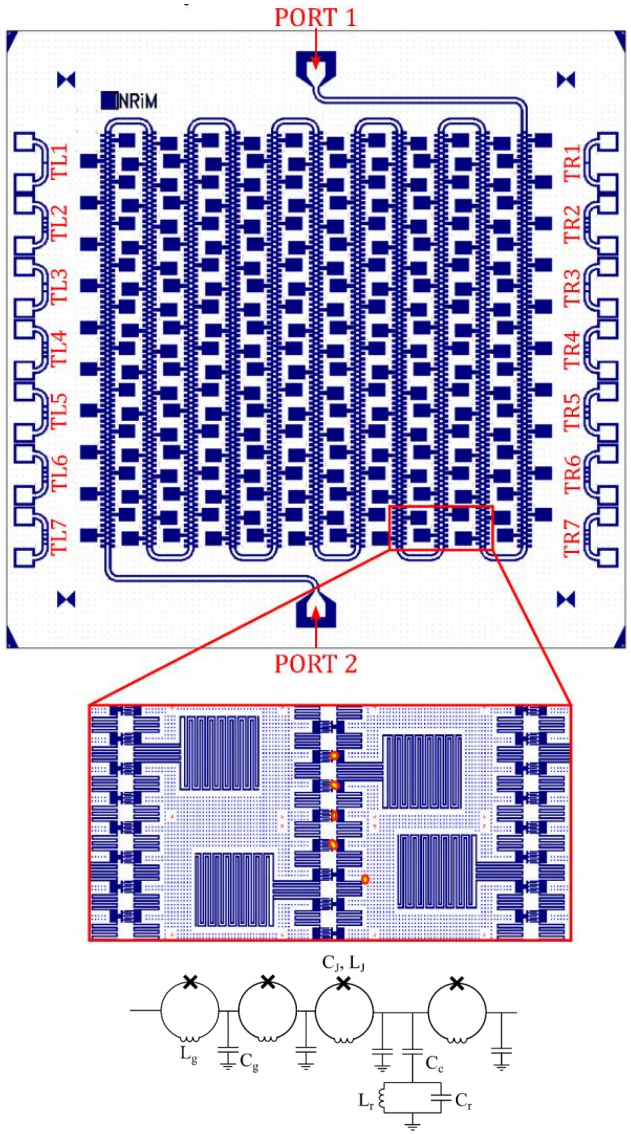
Chips delivered
ID_013_01_A JTWPA
ID_013_01_B JTWPA
SUB_02_F test JJ arrays
SUB_02_J test JJ arrays

SUB_02

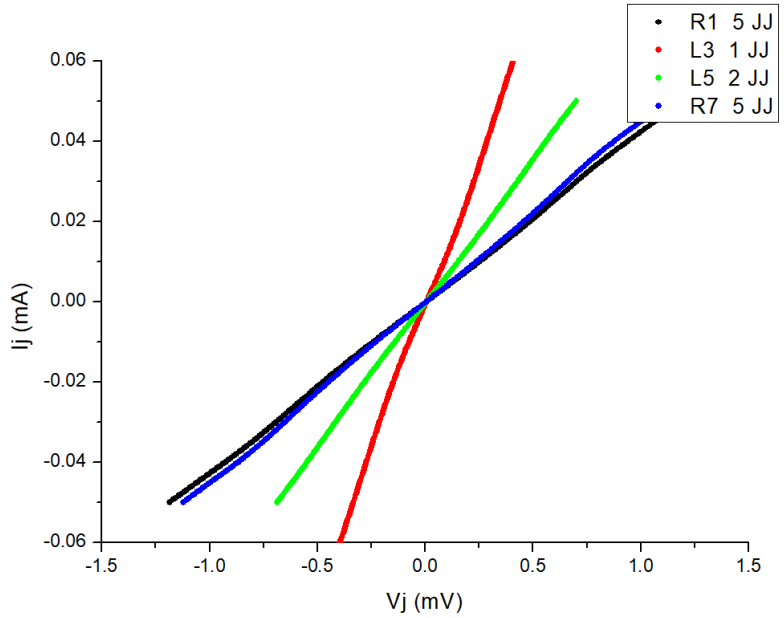


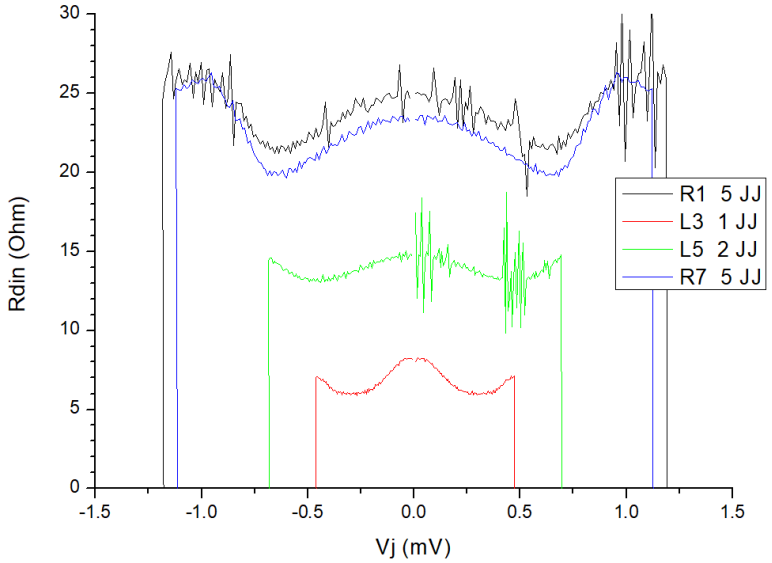
ID	Array	N° di JJs	Resistenza in stato normale [± 0.05 Ω]	Resistenza normalizzata sul numero di JJs [Ω]
Sub_02_F	L1	5	64.26	12.85
Sub_02_F	L2	4	52.68	13.17
Sub_02_F	L3	1	15.18	15.18
Sub_02_F	L5	2	28.10	14.05
Sub_02_F	L6	3	40.26	13.42
Sub_02_F	L7	5	66.34	13.27
Sub_02_F	R1	5	47.43	9.49
Sub_02_F	R2	4	39.02	9.76
Sub_02_F	R3	1	11.03	11.03
Sub_02_F	R5	2	21.15	10.58
Sub_02_F	R6	3	29.36	9.79
Sub_02_F	R7	5	46.58	9.32

ID_013_01



DC Measurement Results





chip SUB_02F
The I-V curves show signatures of superconducting gap (see dV/dI plots)
No critical current visible.

At T = 400 mK one at least of the junction electrodes is still in the normal state.

This is most probably due to the bilayer Ti(5nm)/Al(25nm) used as base electrode which has decreased its Tc below 400 mK

Therefore it is not possible to test the RF properties of JTWPA

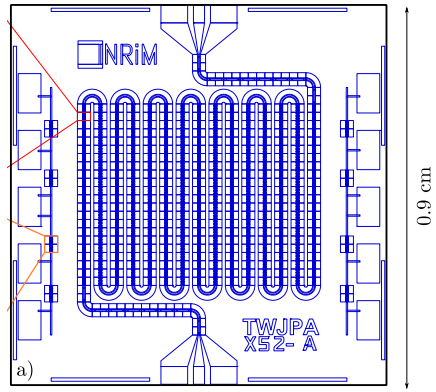
Conclusions

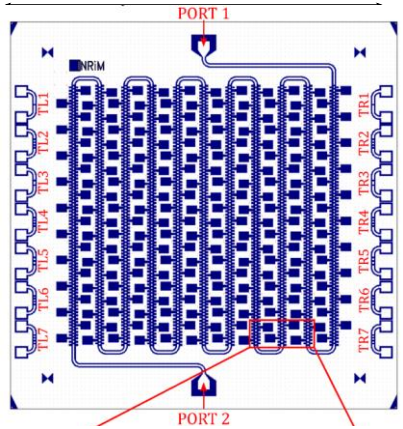
We have tested 2 types of JTWPA: X_52 and ID_013_01 and a test chip: SUB_02

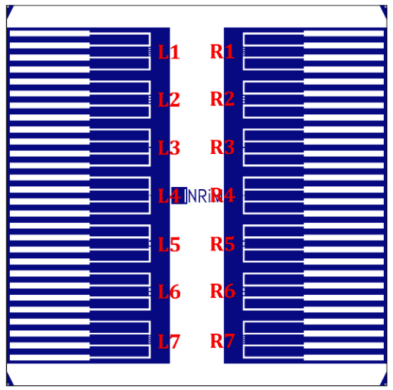
The cryogenic setup works down to 300 mK but we are facing thermal stability problems at the base temperature, that will be addressed.
The RF setup works and we have performed a basic characterization

The DC measurements of the 1° generation JTWPA (X_52) show JJ with critical current in the correct range, but with a relatively high dispersion.
The chip is **very** sensitive to ESD and a more accurate handling procedure is necessary

The 2° generation chips (both ID_013_01 and SUB_2) do not show critical currents down to 350 mK. The opening of superconducting gap is evident at 400 mK but at least one of the electrodes is still in the normal state.
After discussion with colleagues at INRIM, we have concluded that this is due to the presence of a bi-layer Ti/Al as base electrode in the 2nd generation chips, which strongly decreases its critical temperature. Such bilayer will be eliminated in next chips







The Salerno group