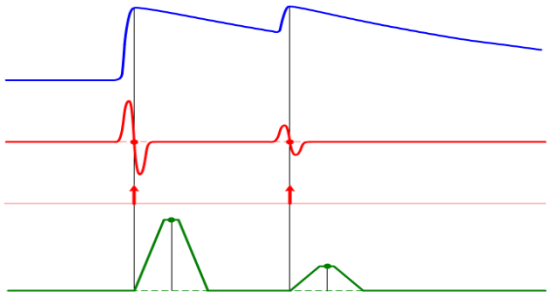
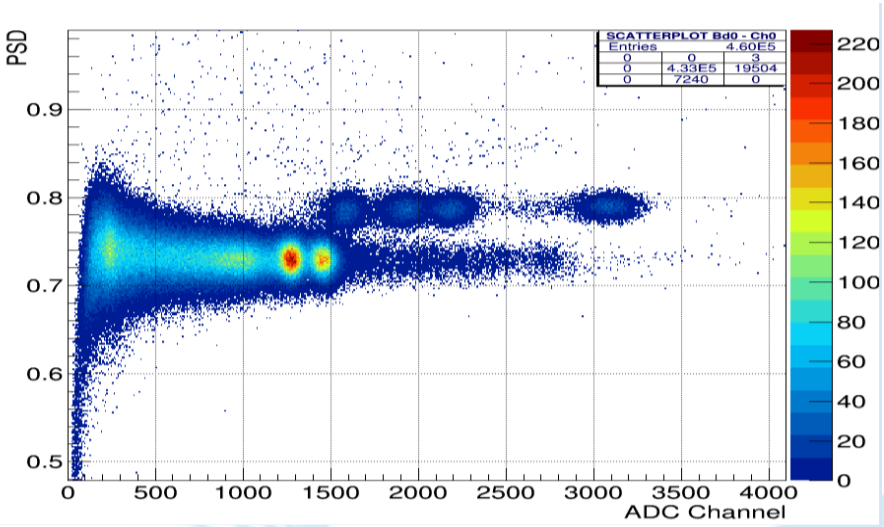
CAEN
Tools for Discovery



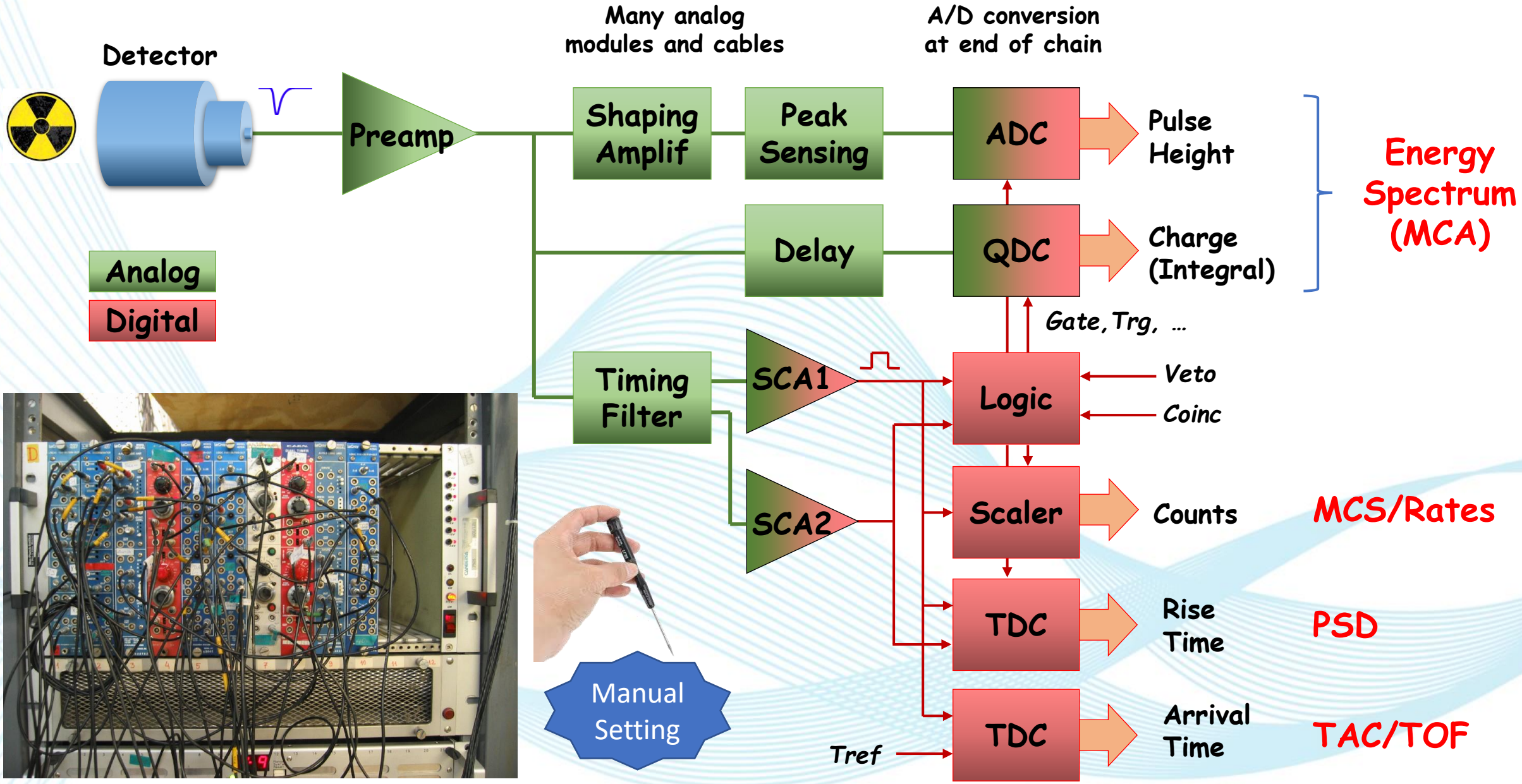
DPP PSD | DPP PHA | DPP QDC



Digital Multi-Parametric Detector Readout Systems

Alessandro Iovene (a.iovene@caen.it)

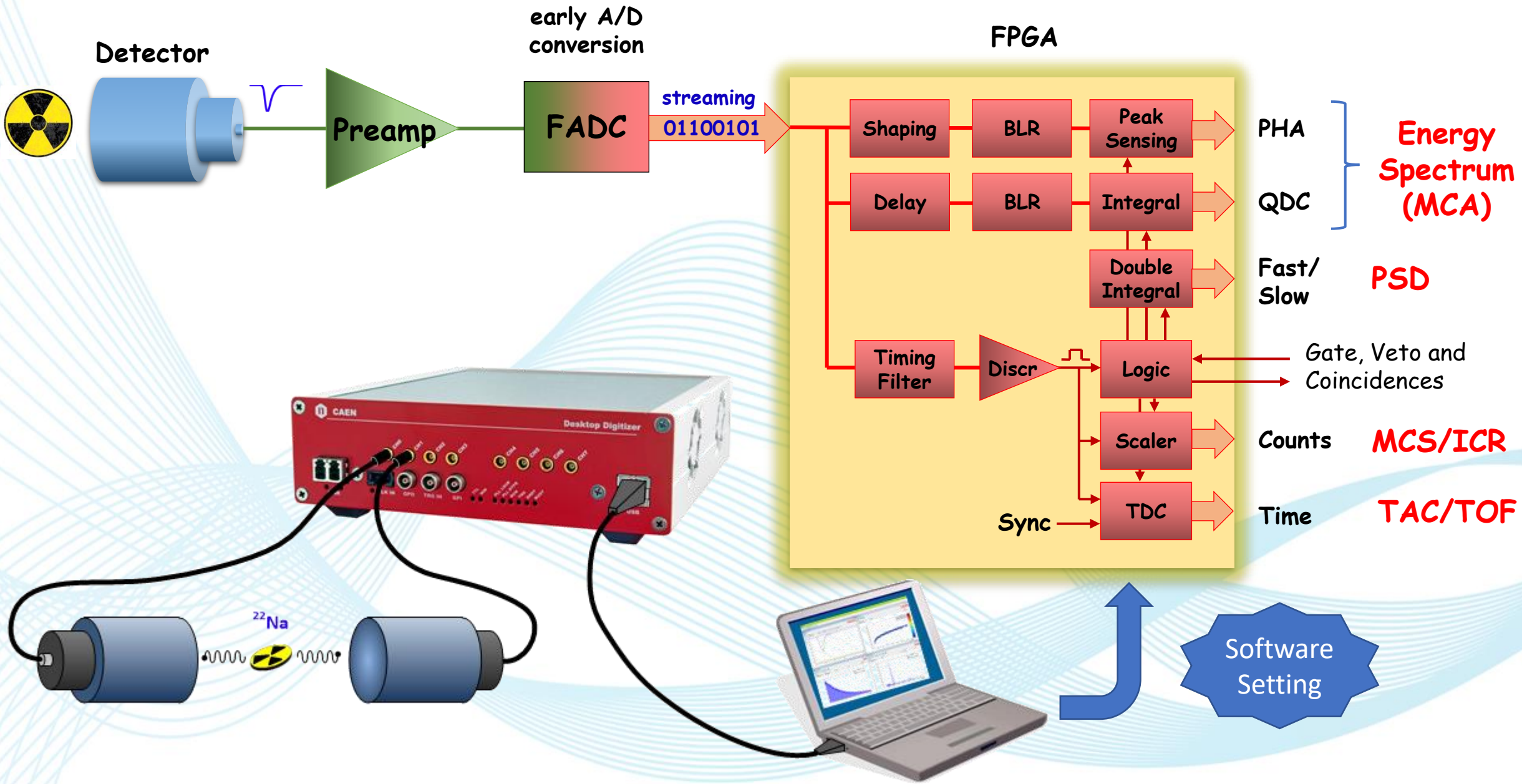
Traditional readout system



Digital Readout: all-in-one

DPP PSD | DPP PHA | DPP QDC

CAEN Tools for Discovery



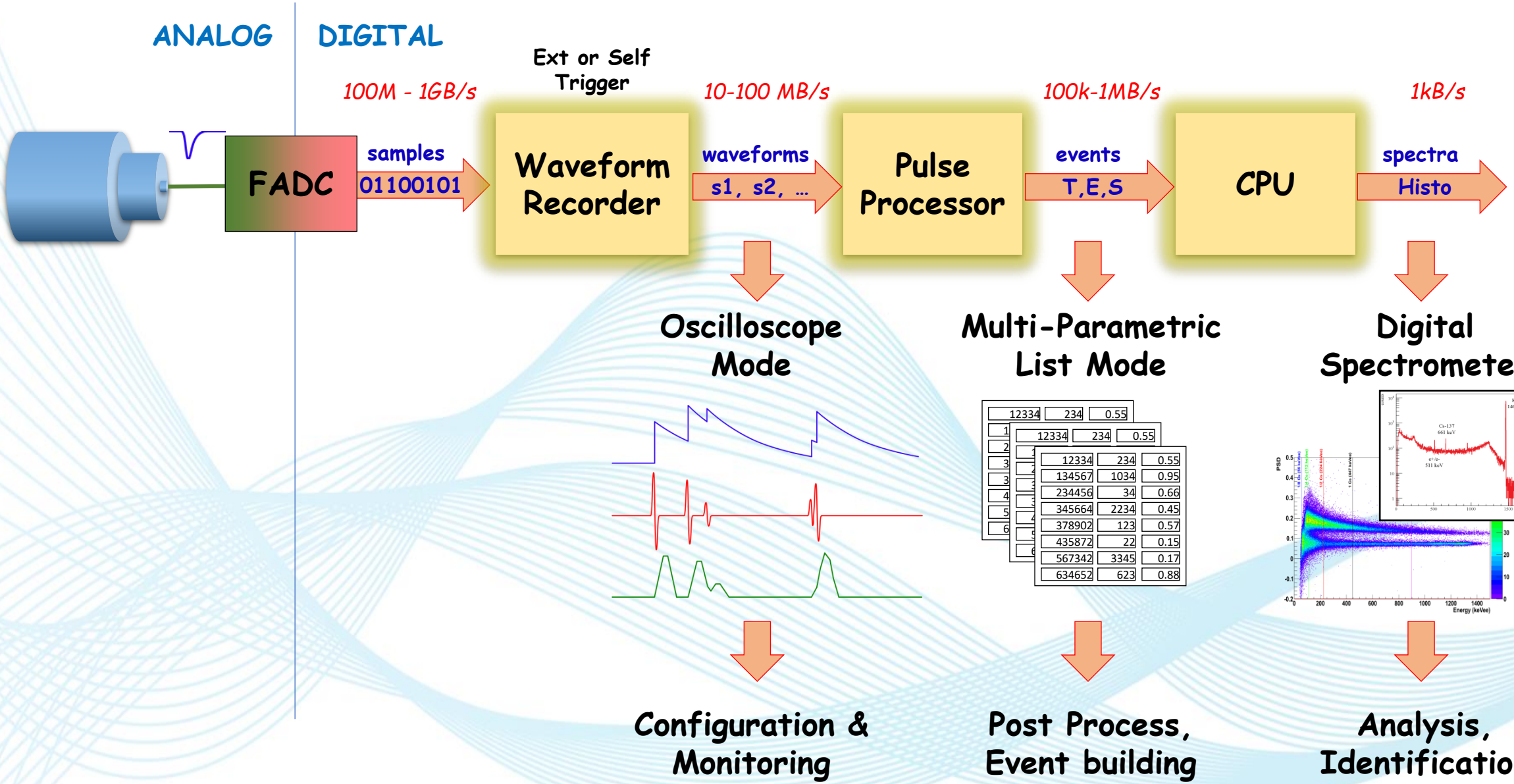
Analog vs Digital readout systems

- **Conventional readout electronics**: several interconnected modules, mainly analog processors (amplifiers, shapers, discriminators) followed by an ADC that converts the parameter of interest and builds the spectrum
- No flexibility: functions hard-coded in electronic circuits!
- **Digital readout: an all-in-one, multi-parametric acquisition system**
- Provides Time Stamps (Discriminator + TDC), Energy (PHA, QDC), PSD, Counts and Waveforms
- Signals from detectors continuously digitized and processed on-line by reprogrammable FPGAs
- Digital algorithms (filters) take the place of the conventional analog processors
- Software controlled Settings
- Embedded oscilloscope for signal inspection
- **Advantages**: flexibility, size and weight, stability, scalability, performances

Benefits of the digital readout

- Analog signals coming from the detectors are digitized (A/D conversion) at a very early stage
- Minimal analog conditioning: no signal shaping, no discriminators, no delay lines
- Dead-timeless signal capture (no conversion time) → preserve signal information
- Multi-parametric (**Energy, PSD, Timing**) acquisition: on-line digital DPP algorithms applied to waveforms to extract the quantities of interest
- Three acquisition modes:
  - **Waveform Mode** (digital oscillocope): mainly used for system monitoring and configuration
  - **List Mode**: read list with time stamp, energy, PSD, etc…
  - **Histogram Mode**: read spectra (Energy, TAC, PSD). Histograms are built in PC in most cases.
- Embedded Logic: Coincidence, Anti-coincidence, Veto, trigger propagation
- Typ. Throughput (assuming 10 kcps/ch): > 10 MB/s/ch in waveform mode, 100 KB/s/ch in list mode, < 1KB/s in Histogram mode.

Digital Acquisition Chain



Scalable systems

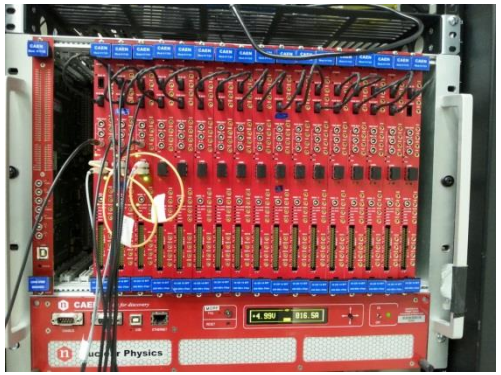
Desktop / Handheld

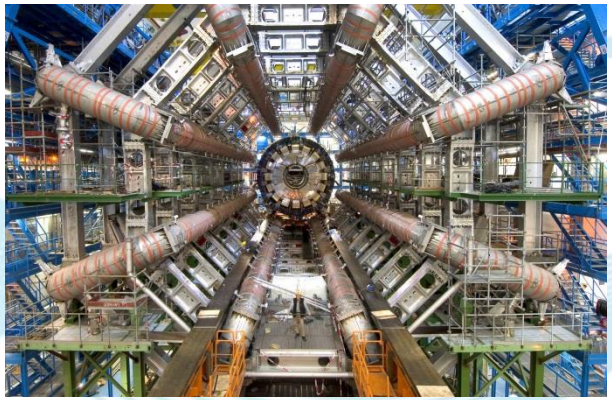
1-10 ch.

Mini crates / enclosures

10-100 ch.

Crates / Racks





100-10000 ch.

Models and Algorithms

Model	# channels	MS/s	# bit	HV	LV	Wave	PHA	PSD	CFD	QDC	Histo	Notes
V1730 / DT5730	16 / 8	500	14	-	-	√	√	√	√	√		Waveform recorder + Pulse Processor
V1725 / DT5725	16 / 8	250	14	-	-	√	√	√	√	√		Waveform recorder + Pulse Processor
V1751 / DT5751	8 / 4	1000	10	-	-	√		√	√	√		Waveform recorder + Pulse Processor
V1724 / DT5724	8 / 4	100	14	-	-	√	√					Waveform recorder + Pulse Processor
V1720 / DT5720	8 / 4	250	12	-	-	√		√		√		Waveform recorder + Pulse Processor
V1740 / DT5740	64 / 32	62.5	12	-	-	√				√		Waveform recorder + Pulse Processor
V1742 / DT5742	32 / 16	5000 (1)	12	-	-	√						Waveform recorder
V1743 / DT5743	16 / 8	3200 (1)	12	-	-	√						Waveform recorder
DT5780	2	100	14	2	2	√	√					MCA (no histo memory, List readout)
DT5781	4	100	14	-	-	√	√					MCA (no histo memory, List readout)
DT5790	2	250	12	2	-	√		√		√		Pulse Processor
DT5770	1	100	16	-	1	√	√				√	MCA
Hexagon	1 or 2	100	16	2	2	√	√				√	MCA with Embedded PC
GammaStream	1	62.5	12	1	-	√	√				√	Tube base MCA with Embedded PC

(1) switched capacitor ADC: fast sampling, slower A/D conversion (=> dead time)

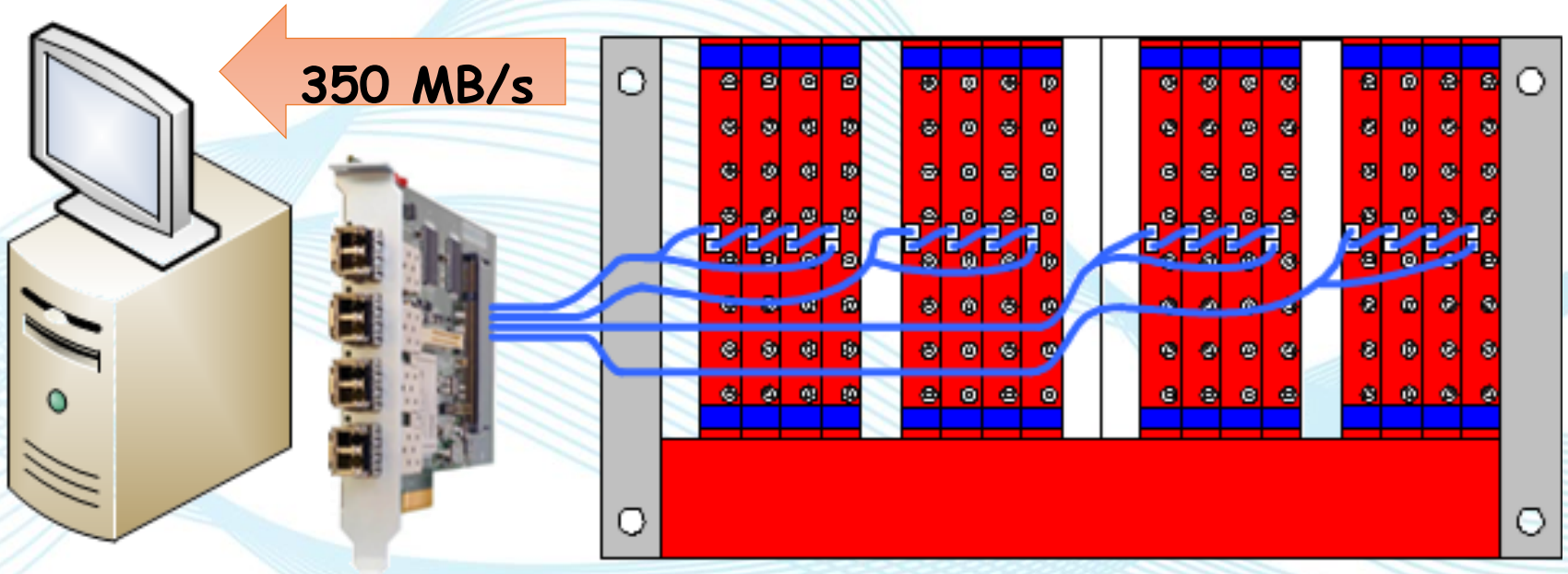
Readout interfaces

- Optical Link (CONET 2)
  - Requires a PCIe card in the host PC (A3818); can read up to 32 boards (up to 2048 channels)
  - 80 MB/s per board → aggregate bandwidth = 320 MB/s
- USB
  - No external hardware required, plug and play
  - 30 MB/s per board.
- Ethernet
  - Only supported by MCAs (DT5770, Hexagon, Gamma-Stream)
  - Will be supported (up to 10 Gbps) in the next generation digitizers
- VME
  - up to 200 MB/s in 2eSST mode (Bandwidth shared between boards in the crate)
  - SBC required for 2eSST; PCI bridges A3818/V2718 support BLT/MBLT only (up to 80 MB/s)

NOTE: The use of the VME bus for communication is discouraged. Front panel readout is backplane independent. VME used for power supply, ventilation and mechanics

Multi-Board Readout example (Xmass)

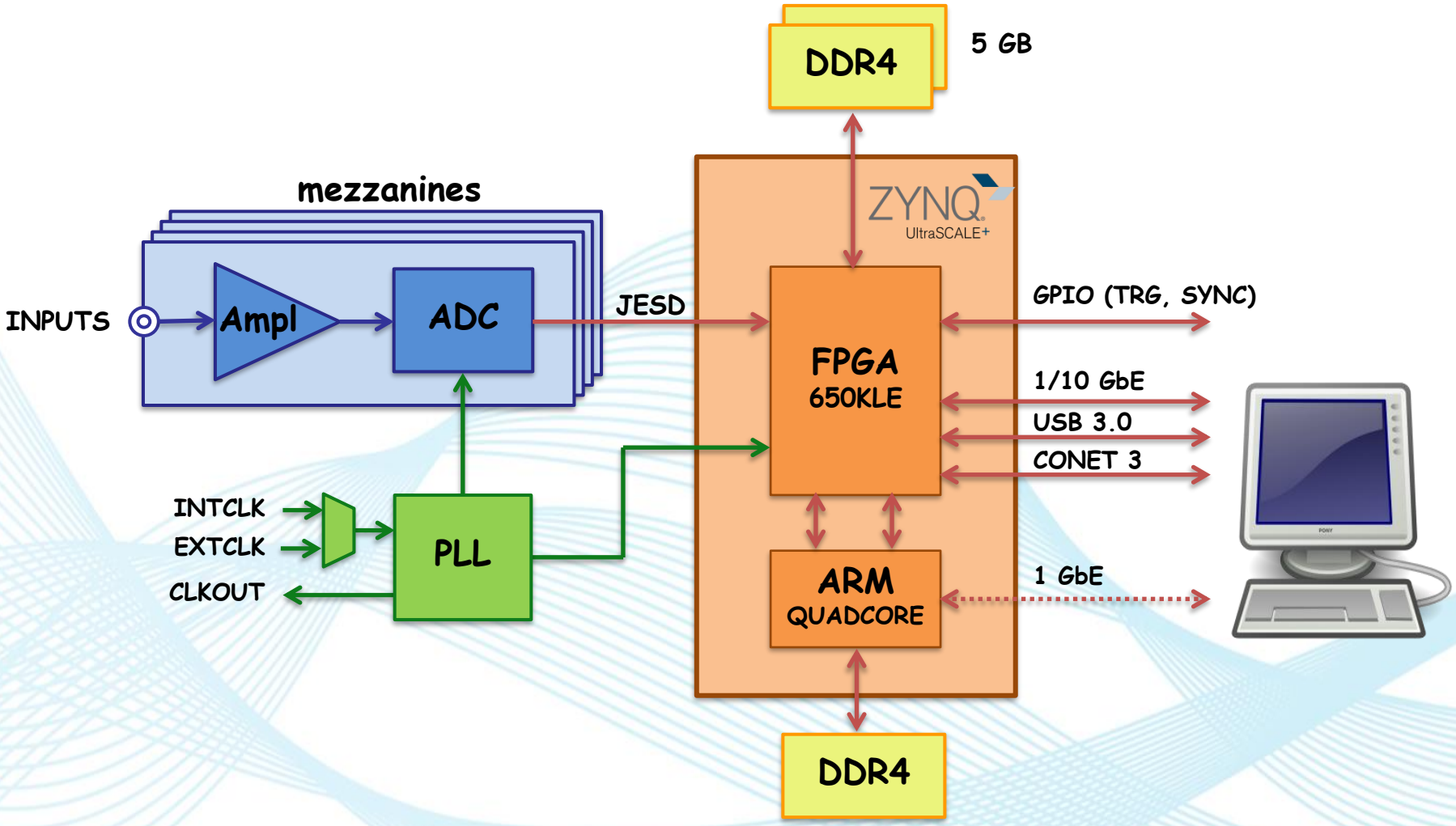
- 16 digitizers in one VME crate read out by 1 computer @ 350 MB/s
- One 4 link A3818 PCIe card. Each link reads 4 digitizers in daisy chain
- ~22 MB/s per digitizer (can be 4 times higher in a P-to-P topology)
- VME crate just for power and mechanics (no backplane communication)



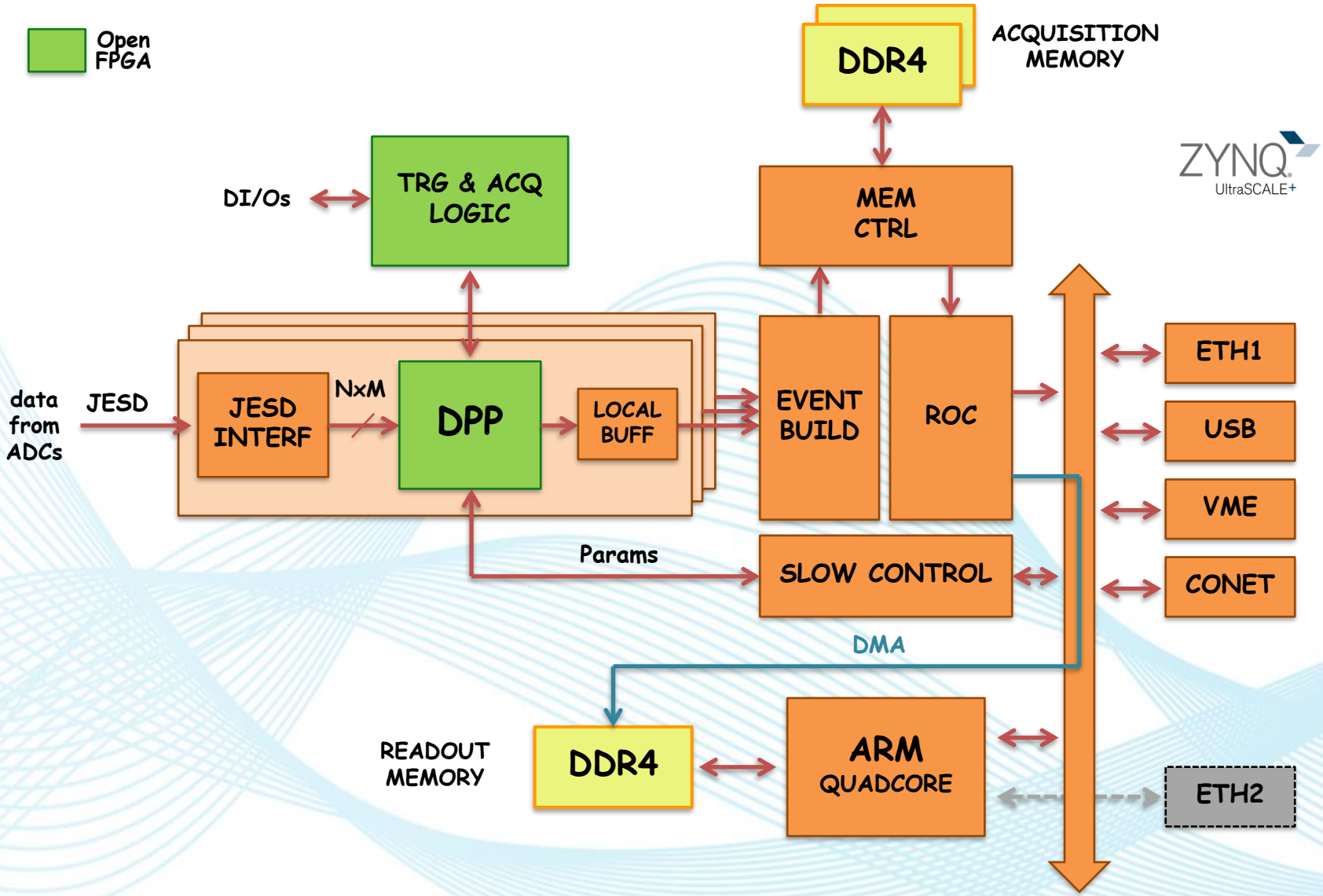
Digitizers 2.0: highlights

- **Communication**
  - **1/10 GbE**, Copper or Fiber
  - **CONET 3** daisy chainable optical link (expected ~300MB/s)
  - **USB 3.0**
  - Legacy VME interface
- **Memory buffers**
  - Acquisition Memory (FPGA): DDR4, 5 Gbytes, 384 Gb/s
  - Readout Memory (ARM): DDR4
- **Models (preliminary)**
  - 16 channel, 14 bit, 1 GS/s (replace x751)
  - 16 channel, 14 bit, 500/250 MS/s (replace x730/x725/x720)
  - 16/32 channel, 16 bit, 100-125 MS/s (replace x724)
  - 64 channel, 14 or 16 bit, 100 MS/s (replace x740)
- **Firmware**
  - Single FPGA architecture; 650 kLE (Zync US+ XCZU11EG)
  - ARM (Quad Cortex, 1.5 GHz)
  - DPP modes: PSD/PHA/QDC/CFD
  - Raw Waveform mode with zero suppression capabilities (ZLE/DAW)
  - **Open FPGA** (template projects and kits for custom developments)

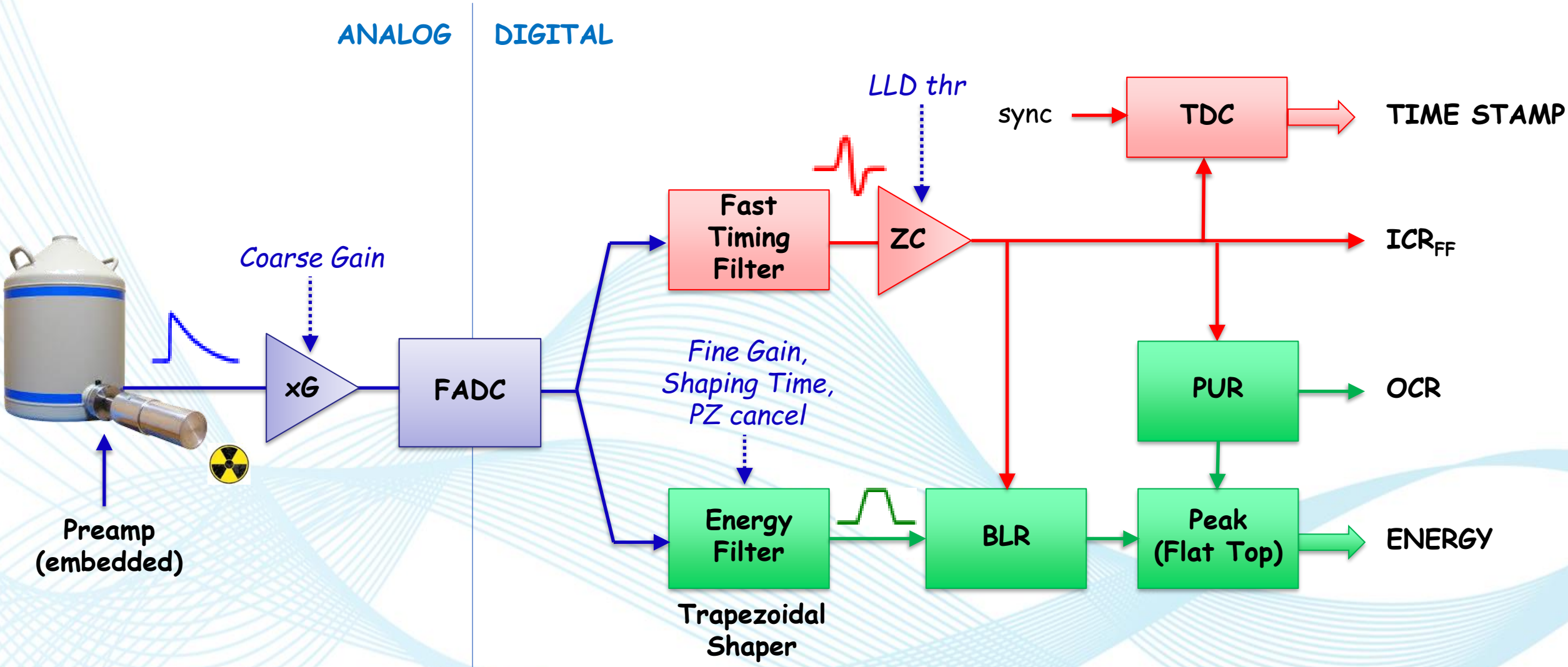
Digitizers 2.0: architecture



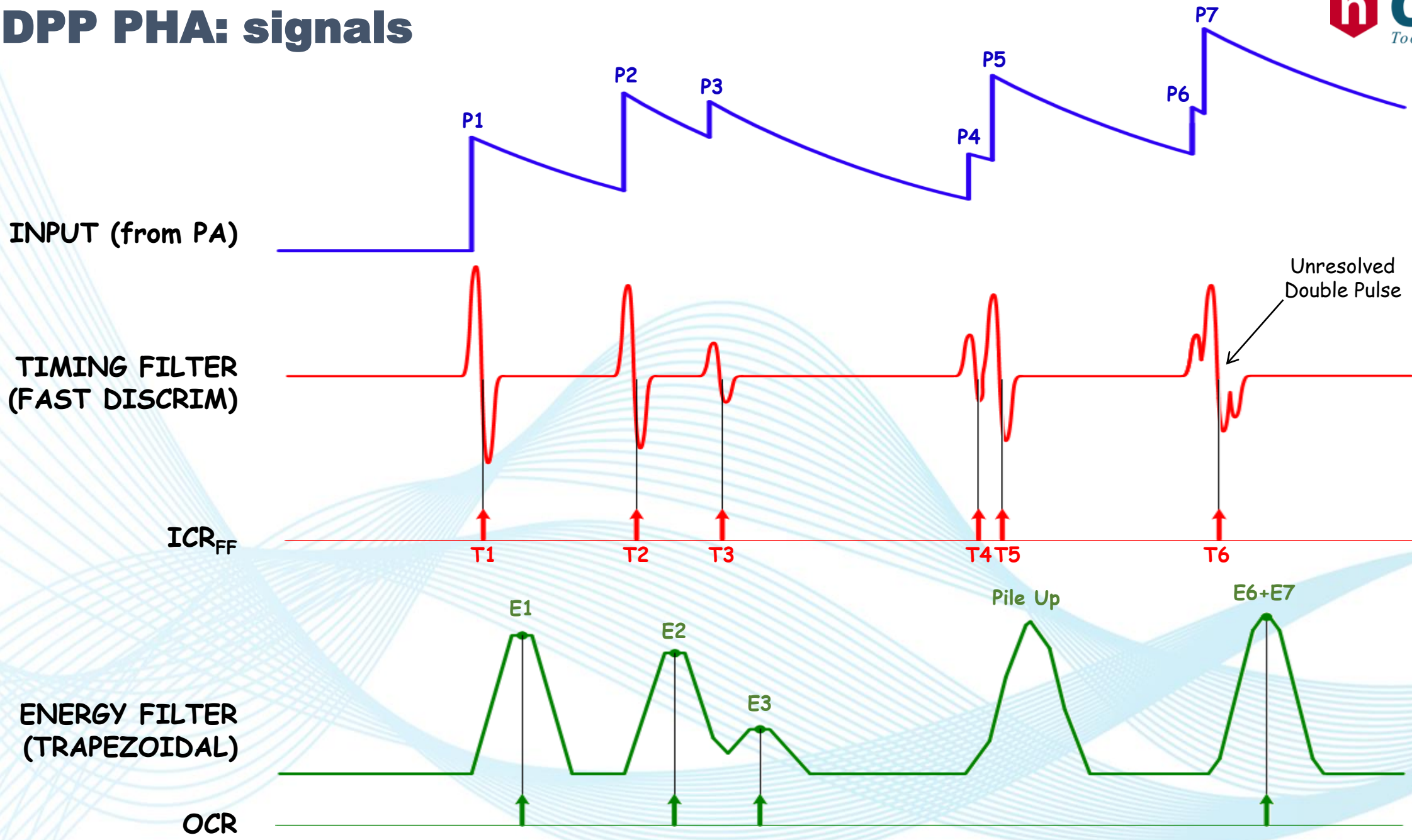
Digitizers 2.0: FPGA Block Diagram



DPP PHA: Block Diagram



DPP PHA: signals



DPP PHA: Pile-up Rejection and Dead Time

The waveform digitizer operates continuously => No dead time in A/D conversion.
Dead time due to algorithms (pulse processing), not to electronics

Energy Filter:

- T5-T4 < Trapez(Rise+Flat) => pile-up => Get time stamps (ICR_{FF}), no energies (OCR)
  *$DeadTime_{TRAPEZ}$ (%) = 100 * (ICR_{FF} - OCR) / ICR_{FF}*
- T3-T2 < Trapez(Rise+Flat+Fall) => no pile-up (get T and E), but no fresh baseline for E3 => worse resolution.
  It is possible to extend the PUR window and allow BLR to recover for every pulse ("*Peak Hold-off*")

Fast Timing Filter:

- T7-T6 < Double Pulse Resolution (Typ. 300-500 ns) => summed pulses => get single T, E (=E6+E7)
  Sum peaks in the energy spectrum.
  Dead time (paralyzable) corrected on statistical base:
  $ICR_{FF} = ICR * exp (- ICR * T_{DPR})$ where T_{DPR} is the double pulse resolution (i.e. resolving time)

DPP PSD/QDC: Block Diagram

ANALOG

DIGITAL

ANODE SIGNAL

FADC

BLR

Timing Filter

Discr

CFD/LED

Threshold

sync

TDC

TIME STAMP

ICR

Coinc/Veto

OCR

Width

PUR

Gate Generator

SHORT

LONG

Coarse Gain (= Qsens)

Delay

QDC_L

ENERGY

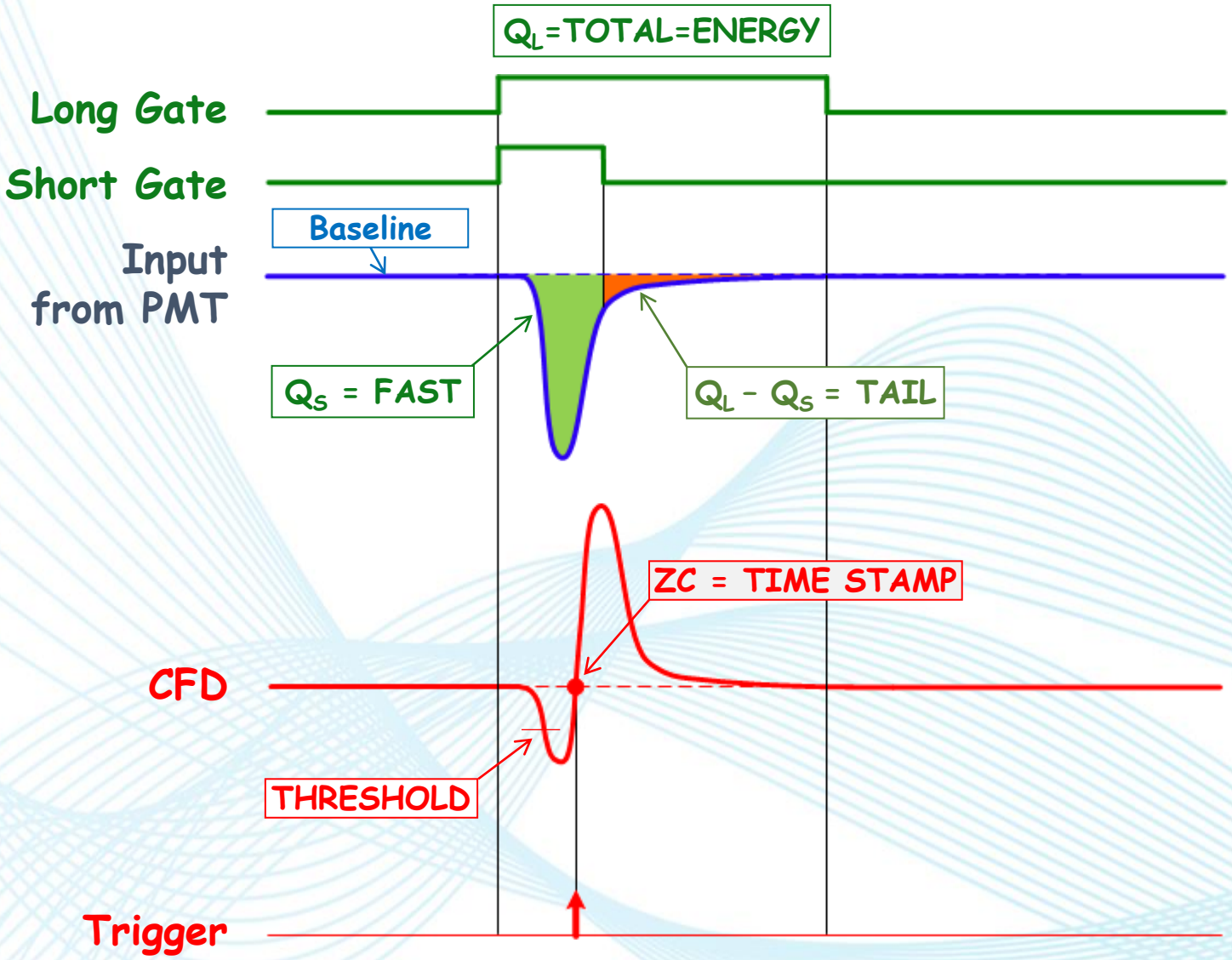
PreTrigger

QDC_S

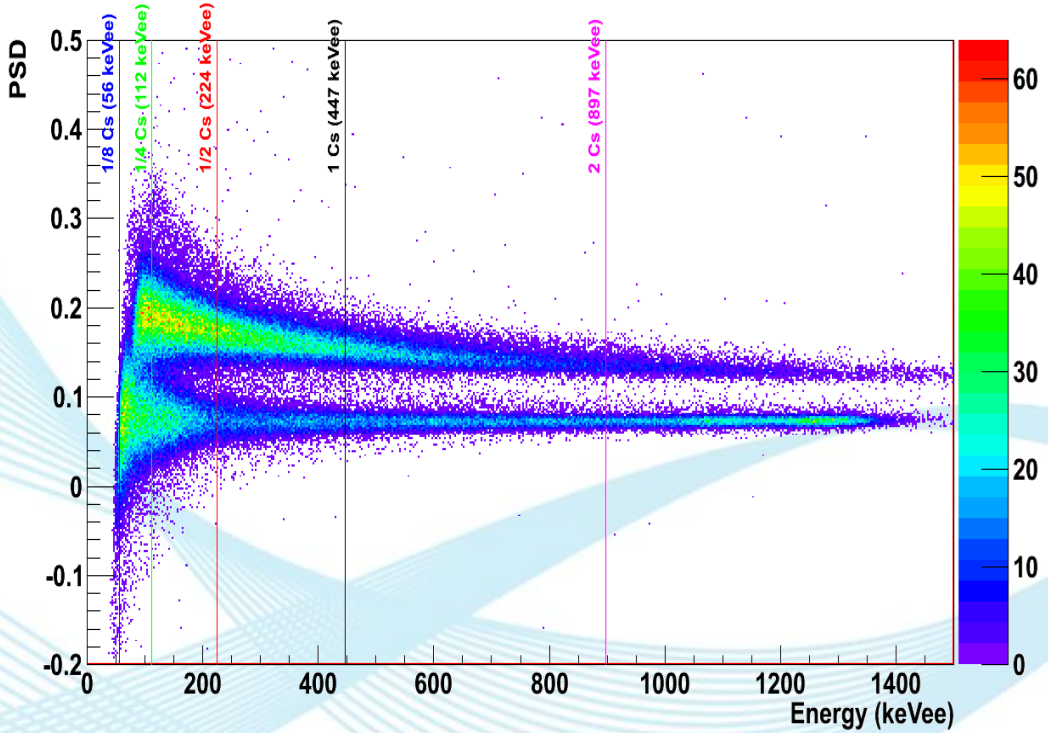
Ratio

PSD

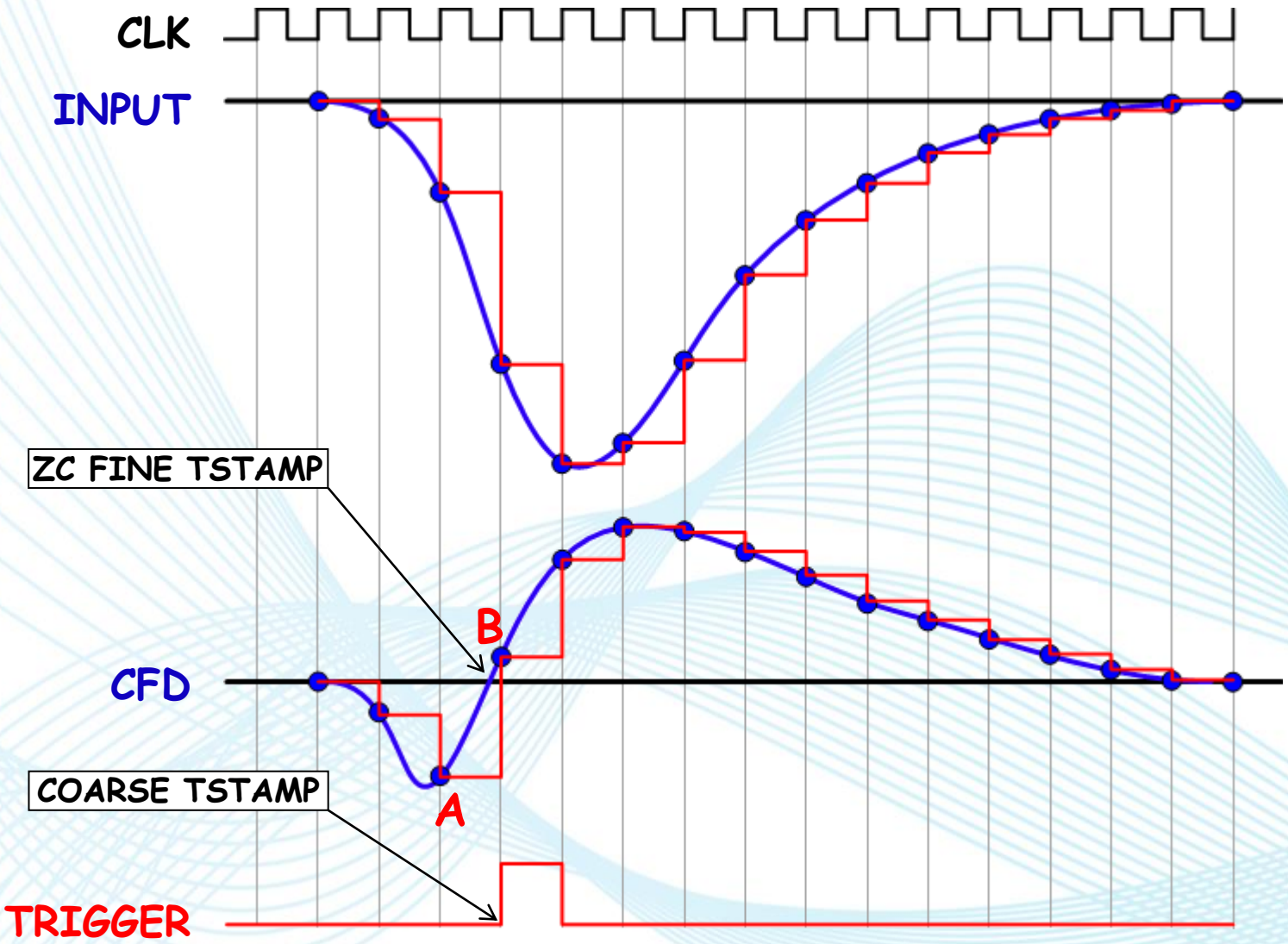
DPP PSD/QDC: signals



$$PSD = \frac{TAIL}{TOTAL}$$



Digital CFD + TDC



digital CFD: same principle as analog

$\mathbf{CFD_{N+1} = f * S_N - S_{N-D}}$ f=Fraction, D=delay

Linear interpolation A-B:
good curve fitting if LeadingEdge > 3-5 T_{SAMPLE}

Faster signals produce artifacts and bad timing resolution

ZC calibration algorithm corrects interpolation errors for signals as fast as ½ T_{SAMPLE}

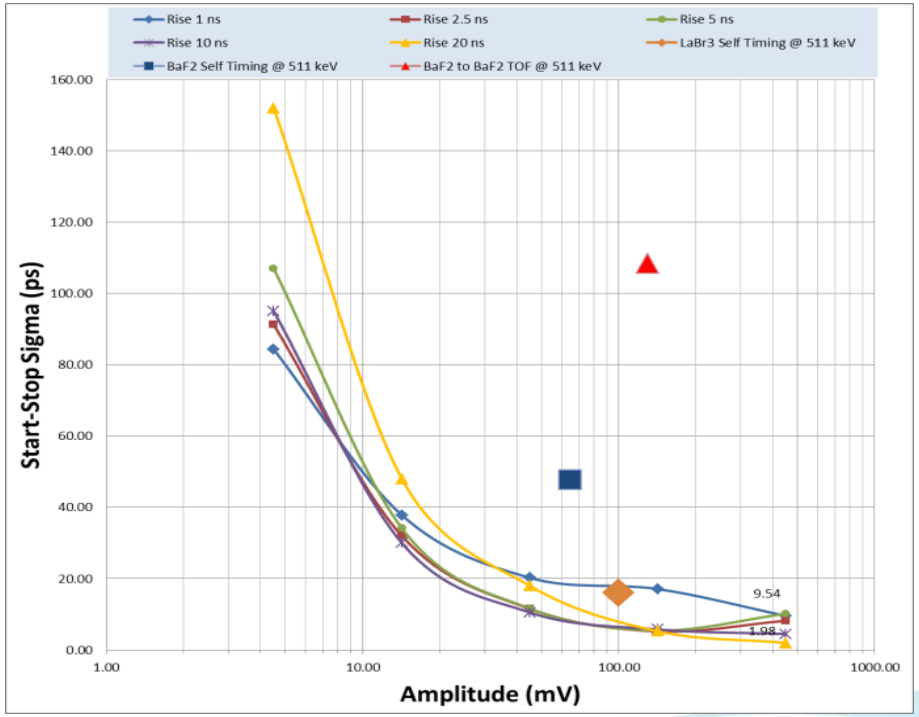
~10 ps RMS for 1 ns rising edge @ 500 MS/s

COARSE TSTAMP = T_{CLK} * Clock Counter

FINE TSTAMP = - T_{CLK} * B/(B-A)

Digital CFD: results

Test	Rise Time	Amplitude	ZC corr	Start-Stop Resolution	
				RMS	FWHM
Pulse Generator	1 ns	450 mV	✓	9.5 ps	22 ps
Pulse Generator	5 ns	450 mV	✓	10.1 ps	24 ps
Pulse Generator	20 ns	450 mV	✓	1.9 ps	4.5 ps
BaF_2 to BaF_2	1.3 ns	130 mV	✓	120 ps	280 ps
BaF_2 to BaF_2	*1.3 ns*	*130 mV*	✗	*538 ps*	*1.3 ns*
BaF_2 to $LaBr_3$	1.3/15 ns	130/200 mV	✓	186 ps	437 ps
NaI to NaI	20 ns	100 mV	✓	1.02 ns	2.40 ns



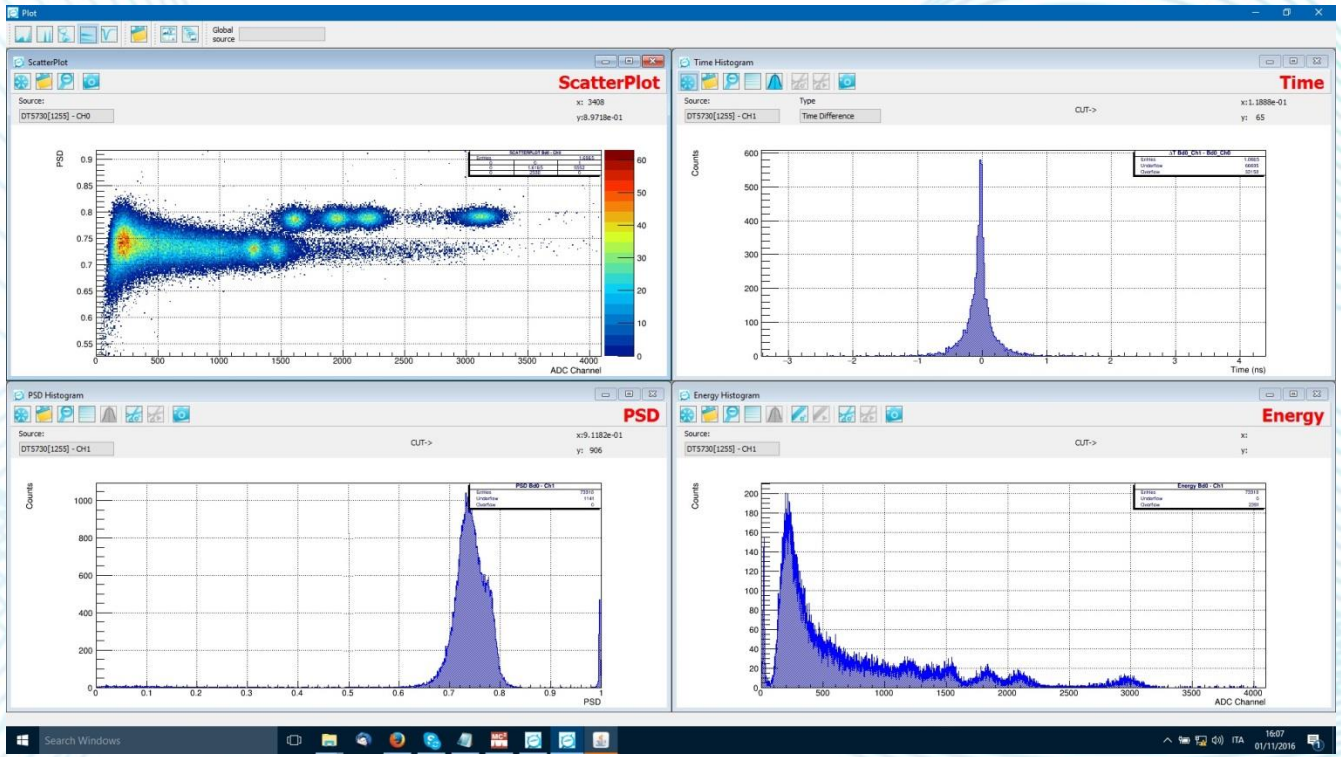
Single Detector Resolution				
Detector Type	Size	PMT	T_{RES} (FWHM)	Notes
BaF_2	1"	H3378-51	200 ps	
$LaBr_3$	2"	R6231	~ 400 ps	extrapolated from BaF_2 to $LaBr_3$ Timing
NaI (Tl)	2"	ETL 9266	1.7 ns	

Compass: root based DAQ

- Multi-board, multi-channel, multi-parametric: **Energy, Time, PSD**
- **Root** data format: T-tree, 1-D and 2-D histograms
- Coincidences (HW or SW), veto/gate, cuts and event selection
- Acquisition mode: live (from boards) or off-line (from data files)

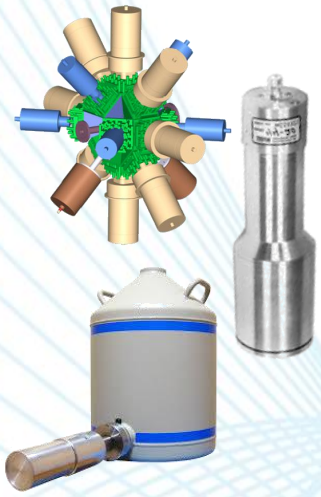
Supported Boards & FW:

- x724/x781 PHA
- x725/x730 PHA
- x725/x730 PSD
- x751 PSD
- x720 PSD/CI



COMPASS

Compass: block diagram



COMPASS

Scan

Configuration GUI

Config File

Config

HW

Readout Server

Sort

Select

ROOT

T-tree

Spectra

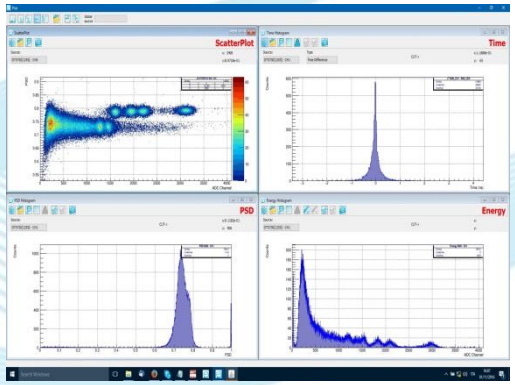
Plots & Stats

Output Socket

Raw Data

Sorted List

E,T,PSD Spectra



Case History (experiments)

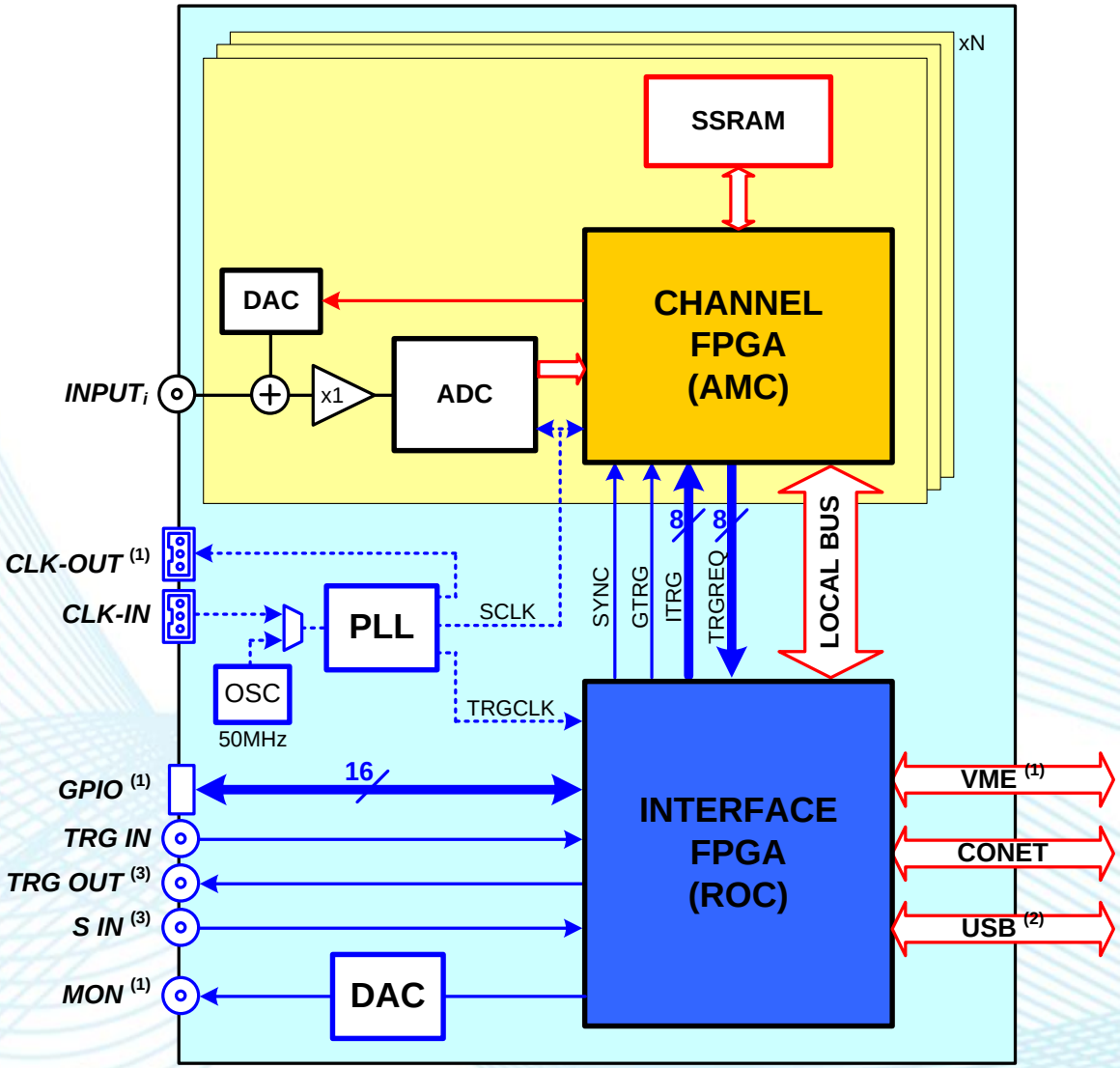
- **XMASS (Kamioka)**: 85 V1751 (ZLE)
- **ELI-NP (Romania)**: 36 V1725 (PHA) + 2 V1730 (PSD)
- **Dance (LANL)**: 12 V1730 (PSD, PHA)
- **Xenon (LNGS)**: 25 V1724 (Custom FW)
- **Deap (Snolab)**: 32 V1720 + 5 V1740 (Raw Waveforms)
- **Mini Clean (Snolab)**: 8 V1720 (Raw Waveforms)
- **DHRUVA (BARC)**: 4 V1724 (PHA) + 1 V1720 (CI) + 1 V1730 (PSD)
- **Exill (ILL)**: 10 V1724 (PHA) + V1751
- **Dark Side (LNGS)**: V1720 (Raw Waveforms)

and more…

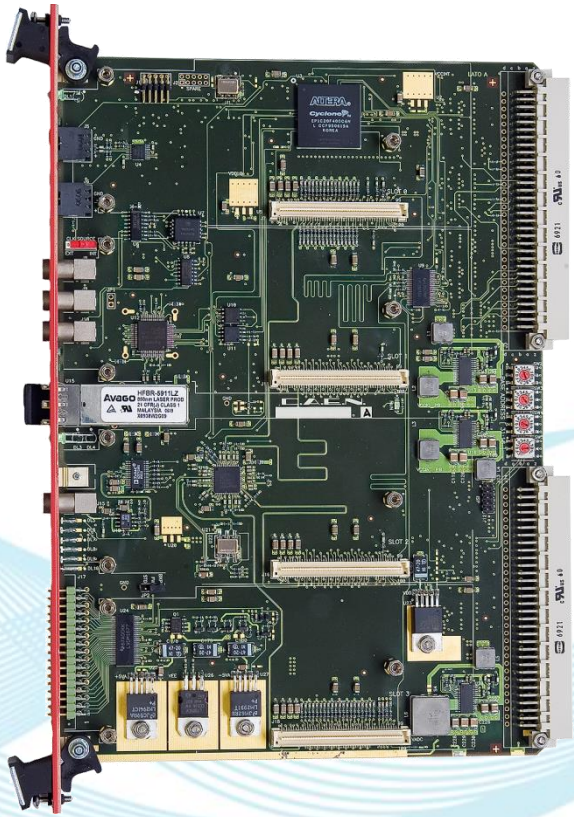
Thank You!

BACKUP

General Architecture



(1) VME boards only
(2) Desktop/NIM boards only
(3) for Desktop/NIM baords, TRG-OUT = GPO, S-IN = GPI



Synchronization: goals

ADC sampling clock

- all channels/boards must have the same ADC sampling clock
- On-board programmable PLL: lock with almost any external frequency (typ. 62.5 MHz)
- front panel clock IN-OUT: Fan-Out or Daisy-Chain distribution
- 1st board in the chain can act as clock master (no external reference required)
- Clock skew due to propagation delay can be tolerated (calibration in SW) or compensated in PLL

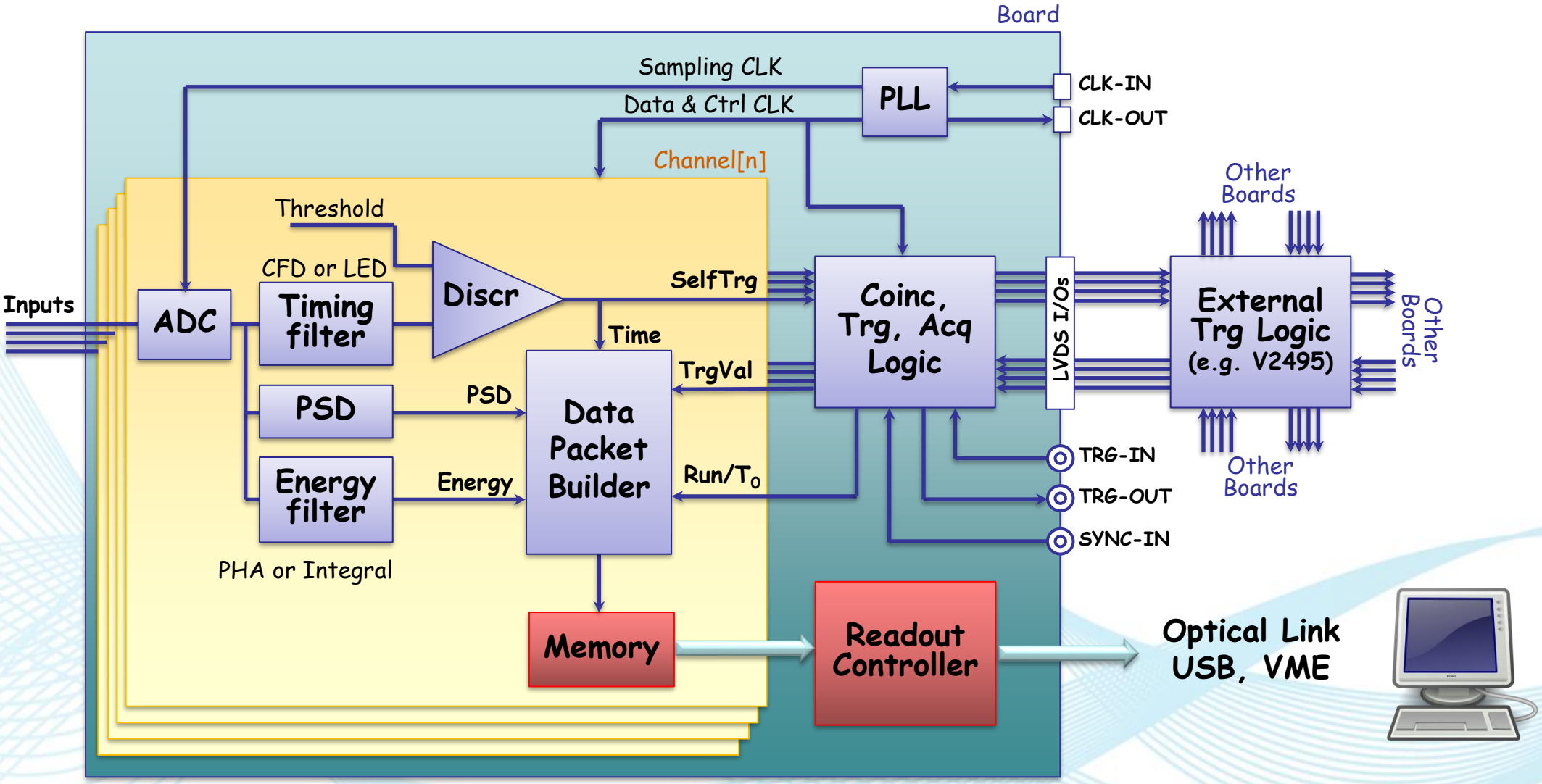
Time Stamp

- all channels/boards must have the same zero for the time stamp
- T=0 @ Start of Run: propagated in daisy chain via front panel I/Os
- Option to use the 1st trigger as a Start of Run

Data

- Each channel/board asserts the Busy signal when its memory buffer is full
- OR of busy signals from all channels/boards must be used to inhibit acquisition (VETO)
- Options on LVDS I/Os to propagate Busy and Veto across boards

Synchronization and Trigger Logic



ZLE/DAW firmware for x725/x730

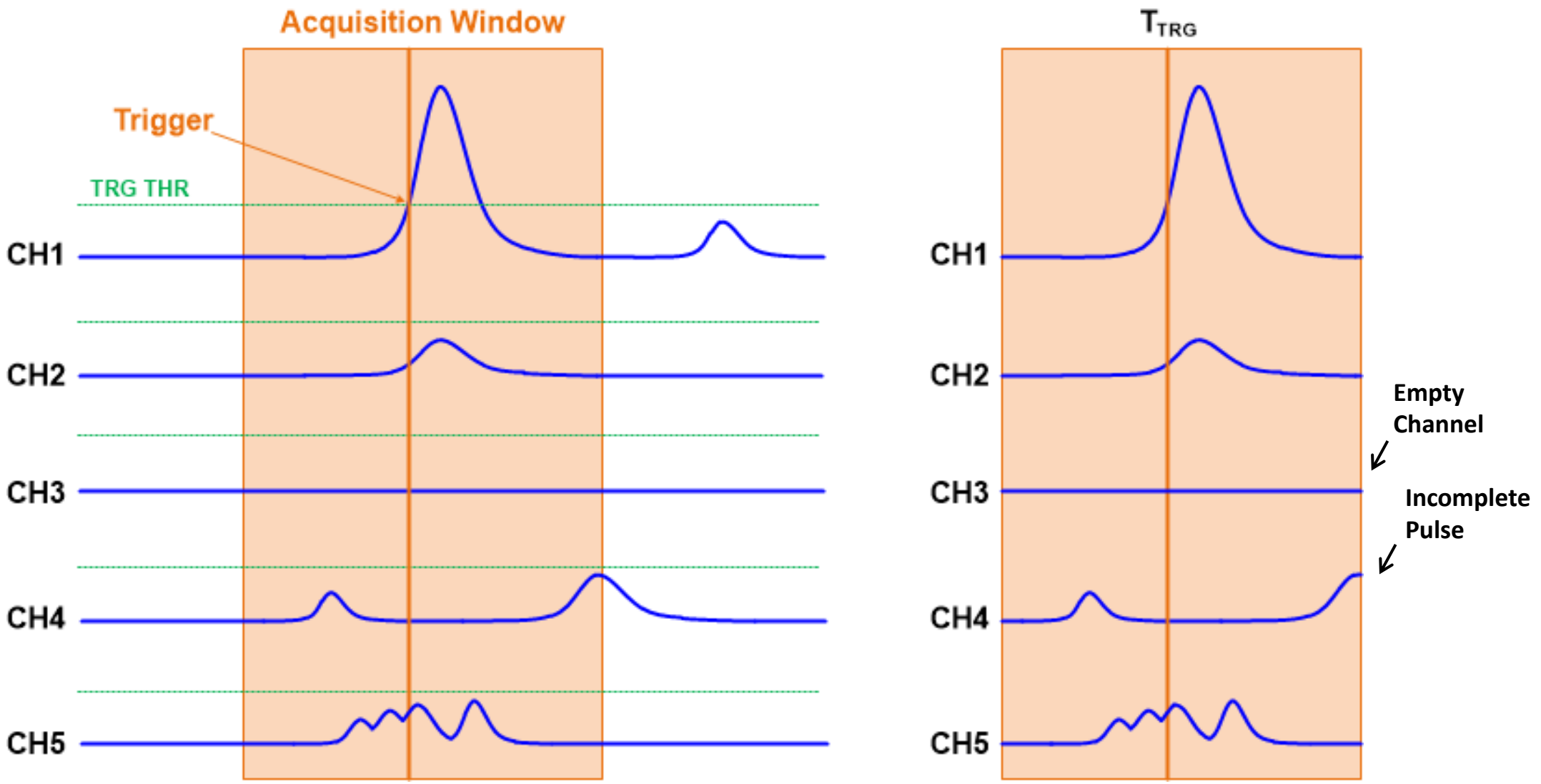
ZLE

- Raw Waveform acquisition with zero suppression: extraction of chunks from a fixed size window
- **Common trigger** (simultaneous acquisition on all channels)
- Channel self-triggers (digital discriminators) can generate the common trigger (masked OR)
- Baseline subtraction
- Max 16/32 µs acquisition window for x730/x725 respectively
- Separate thresholds for trigger and ZS: typically high threshold for triggering (well above noise, to prevent false triggering), lower threshold for zero suppression (to acquire small pulses at the noise level)
- Event Building in HW (1 trigger => N channels)

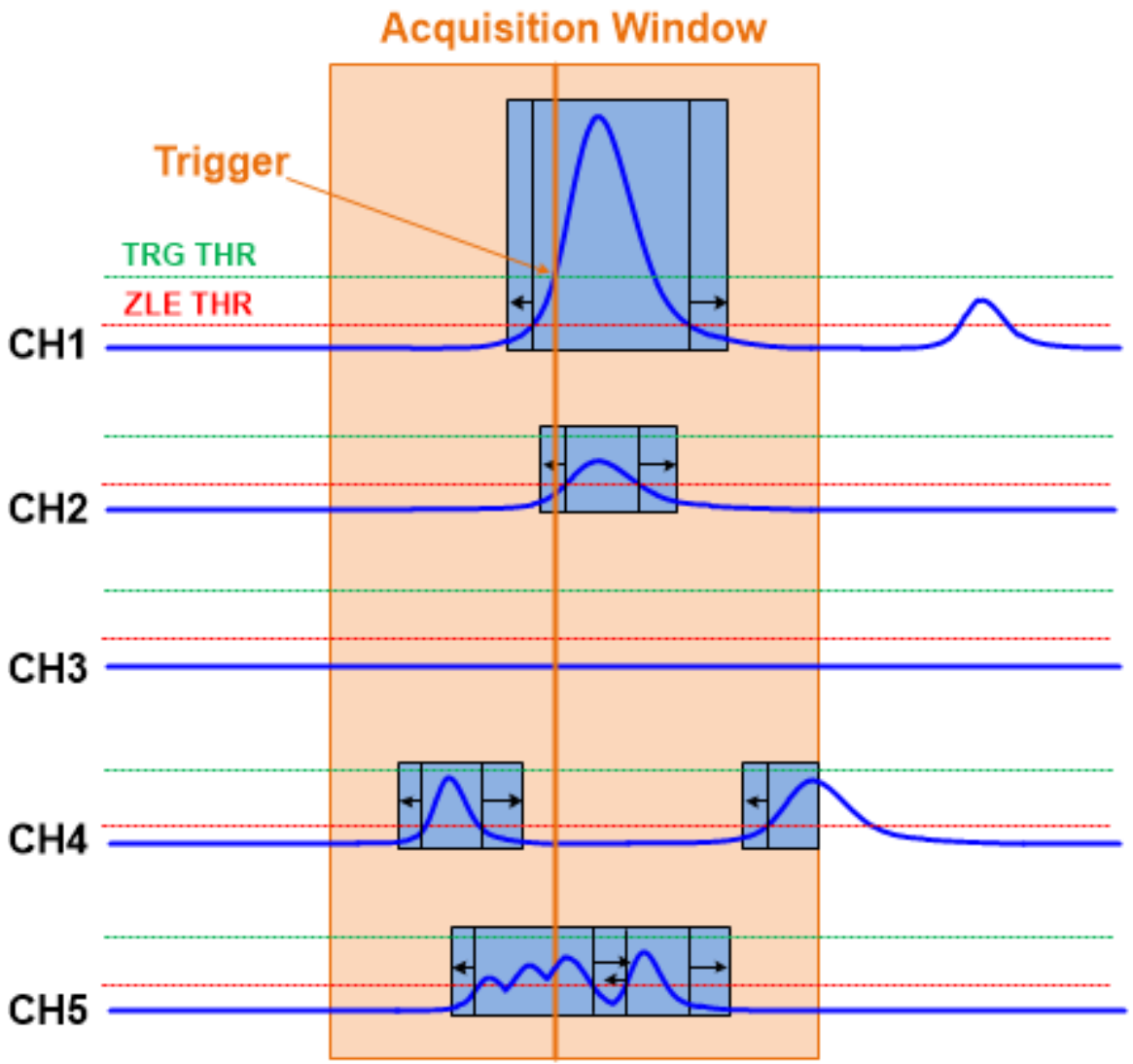
DAW

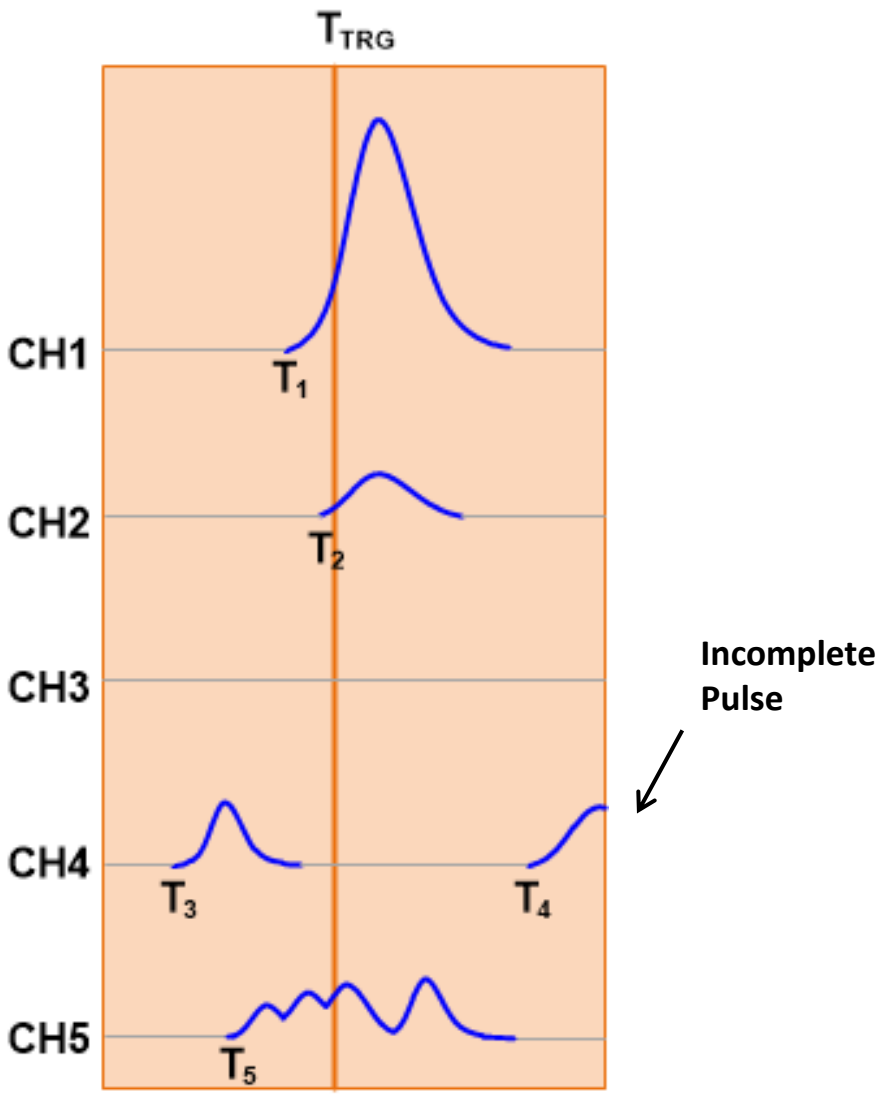
- Raw Waveform acquisition with **independent self-triggering** channels
- Acquisition window dynamically adapted to the pulse width
- Baseline subtraction
- “Unlimited” acquisition window
- Event Building in SW by time stamp sorting

STD firmware

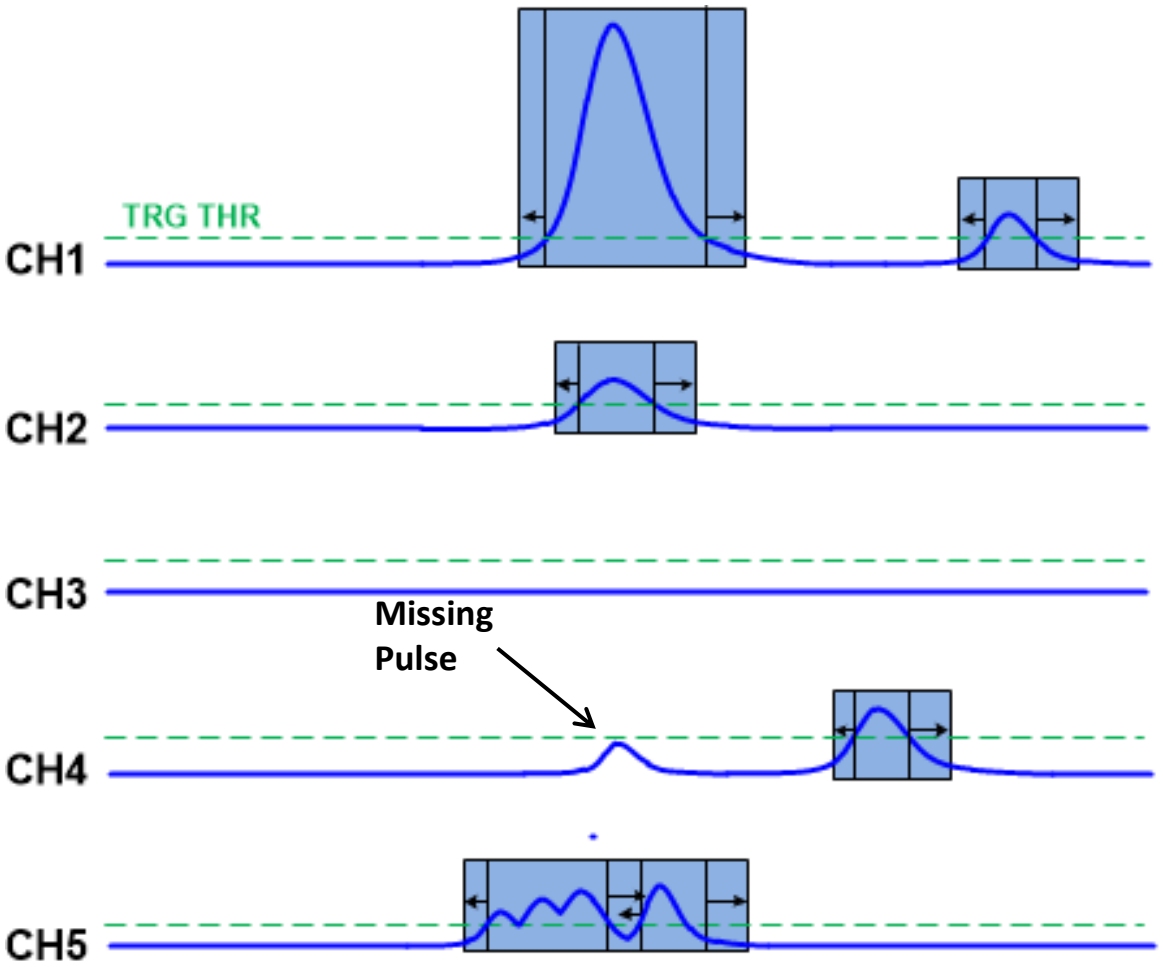


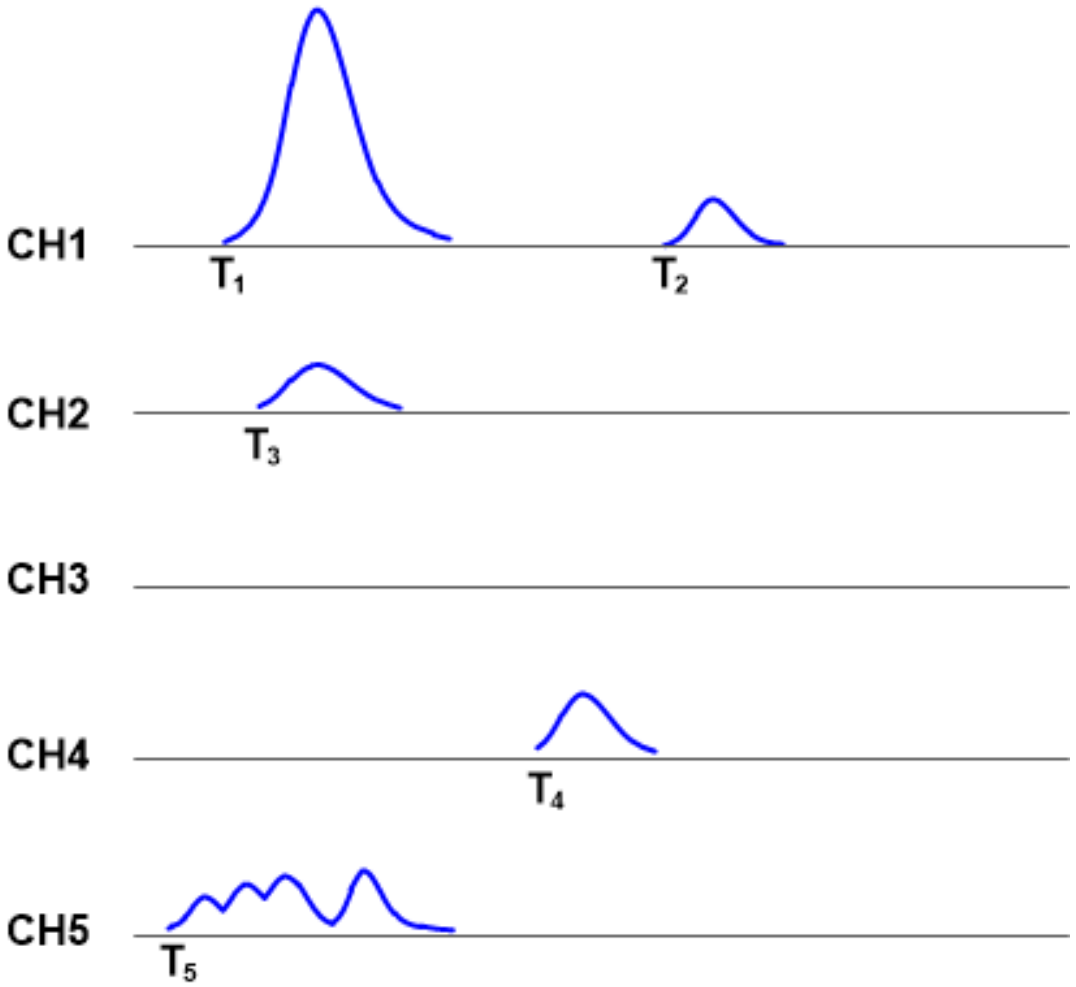
ZLE firmware





DAW firmware





DPP firmware