



Istituto Nazionale di Fisica Nucleare
Sezione di PISA

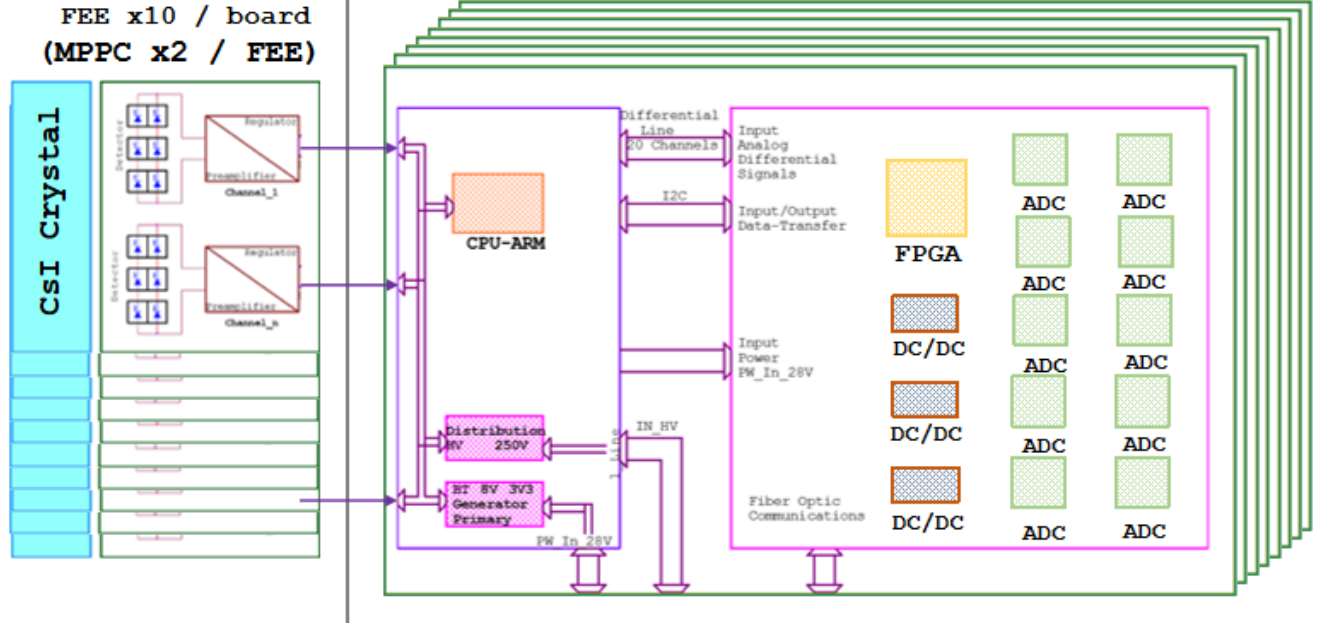
Status report DIRAC board

F.Spinella, E. Pedreschi, L. Morescalchi, A. Taffara

Calorimeter electronics scheme

Disks x2

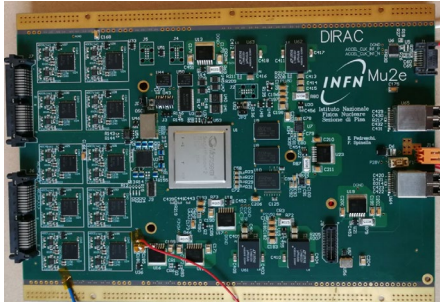
Crate x10



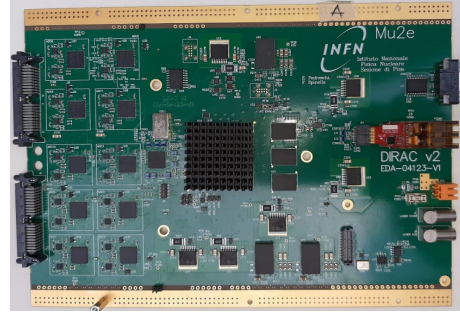
- 20 channels/DIRAC
- 200 MHz, 12 bit ADC
- fiber readout
- 28 volts

- 20 crates
- 136 DIRAC
- 4 TRAD (DIRAC + mezz)
- 160 schede prodotte
- 10% componenti spare

Dirac: versions



- V1
 - Smartfusion2 FPGA
 - Cotsworks transceivers
 - LTM8033



- V2
 - Polarfire FPGA
 - VTRX transceiver
 - LMTM33606



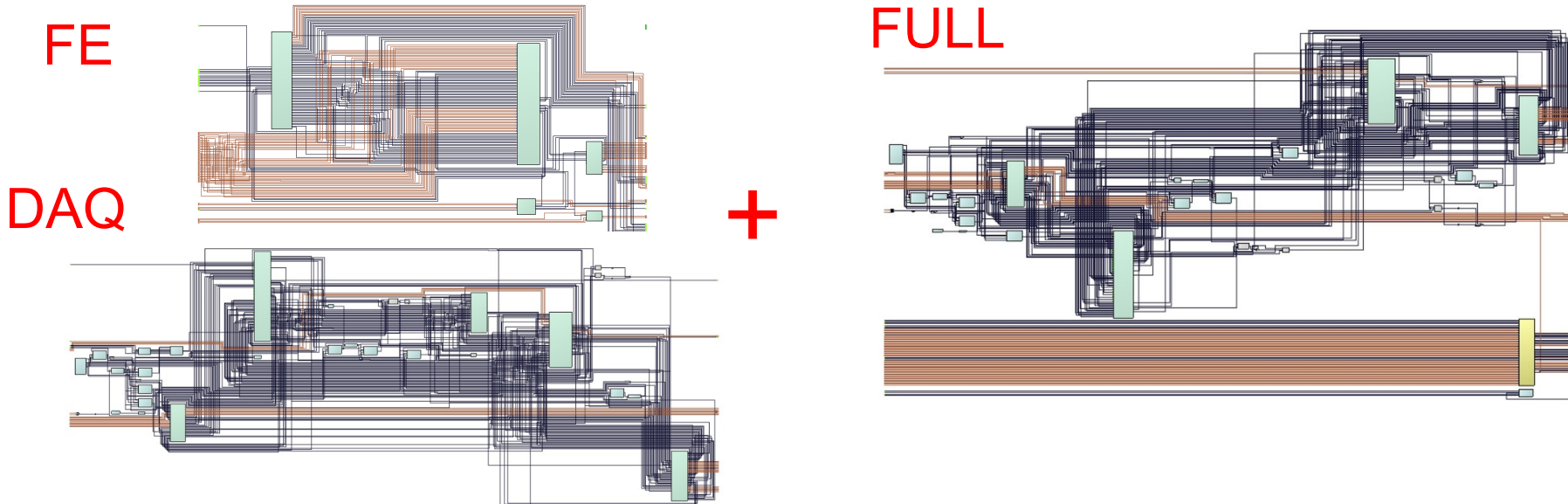
- V3
 - Similar to V2
 - Auto-reset toward mezzanine
 - Compatible with commercial transceiver (backup to VTRX see CERN reports)
 - Prototype under test since 4/2022

All versions functionally ok. Mods due to :

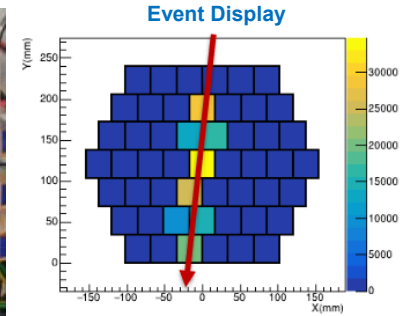
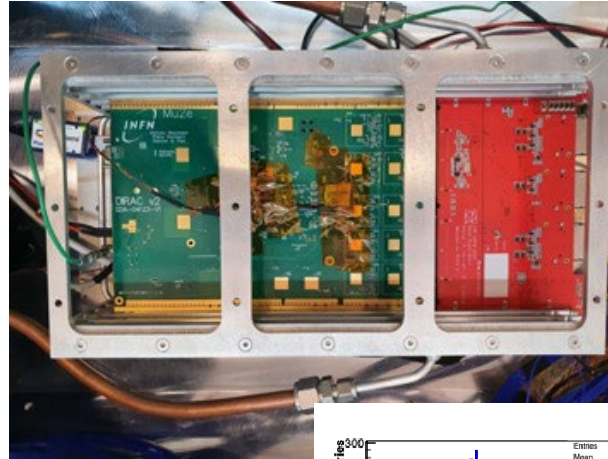
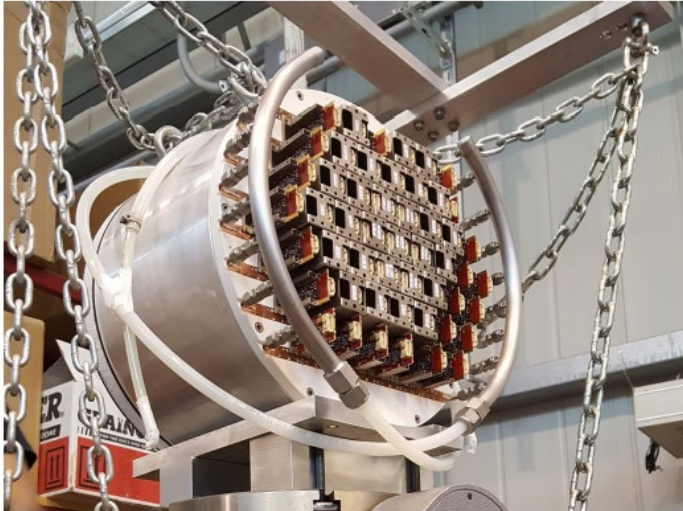
- **new specs from collaboration**
- **Issues due to the harsh environment (B, rad)**

Firmware

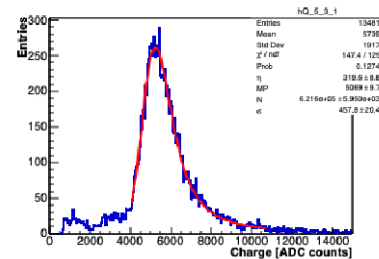
- Quite complicate ... huge amount of data, FPGA of medium performance
 - > forced solution due to radiation and cost
- Most of the firmware is written and tested
- 2 parallel designs: FE interface to ADC & data handling, compression and interface to DAQ, works fine at full speed -> fused recently, under test ..



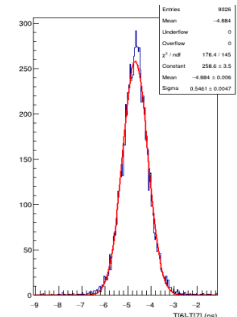
Test at M0



Time resolution of about 300 ps on MIP



MIP charge distributions
(MPV = 21 MeV)



Time difference of two SiPMs/Crystal

- Full electronics chain used for full Vertical Slice Test (VST)
- **Data collected in vacuum, at low T and with irradiated sensors for the last 10 months**
- **Acquisition of Cosmic Rays**
- Stable operation and reconstruction
- Data taking of CR events triggered with external scintillators

Production

- Bid for 160 boards + spare components assigned to DF electronics in 2020
- We asked to buy all parts except FPGA (due to firmware design in progress)
- All parts arrived and stored at their facility. DDR arrived recently.
- We asked to buy also FPGA in 2021 but we were hit by the famous semiconductors shortage crisis
- Current FPGA delivery is March 2023 (increasing ...)
- Following FPGA delivery production is supposed to be fast
- All the other Mu2e subD have same problem (or worse ...)

Qualification tests

- All board versions must be qualified against dose, neutrons, B, thermal dissipation in vacuum
- V2 was fully qualified, V3 is very similar to V2.
- Recently (2020) the collaboration is asking also SEU tests with high energy hadrons (protons)
 - > they provide access to Warrentville Hospital Hadron therapy facility (high flux of 200 MeV protons)

o Calliope @ENEA

- > Co60 source
- > Dose in function of distance: Max 2krad/h, requested 1krad/h
- > Full V1 board test



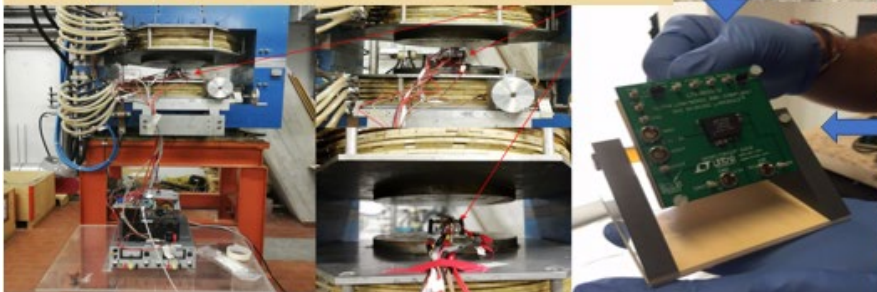
o YELBE @HZDR

- > γ from Bremsstrahlung ($0 < E < 14 \text{ MeV}$)
- > Estimated dose $\approx 20 \text{ krad/h}$ @ $600 \mu\text{A}$
- > Single components test



o LASA @INFN-Milano

- > 1 T magnetic field
- > Different orientations



o FNG @ENEA

- > 14 MeV neutrons from D+T
- > Total neutron flux of $1.2 \times 10^{12} \text{ n } 1 \text{ MeV (Si) / cm}^2$
- > Total neutron flux of $6 \times 10^{11} \text{ n } 1 \text{ MeV (Si) / cm}^2$

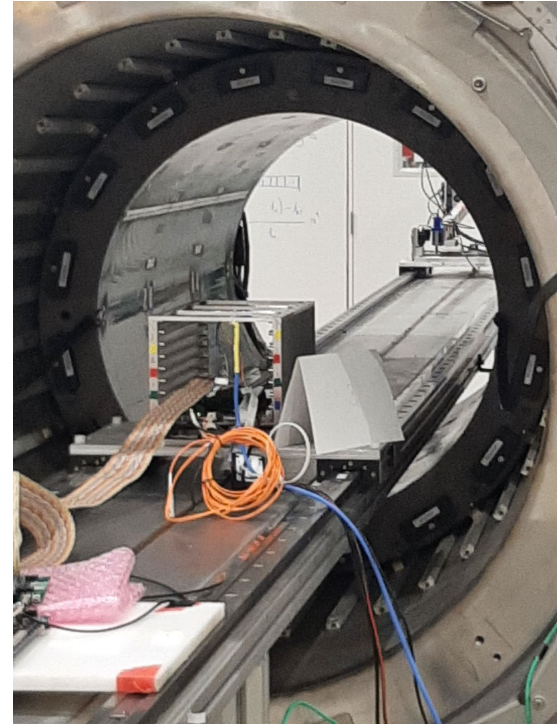


V3 qualification tests

- B field test -> **Done** (Argonne lab. 19 July 2022)
- SEU test -> **Done** (Warrenville Hospital, 21-22 July 2022)
- TID, neutrons, vacuum -> to be done next weeks

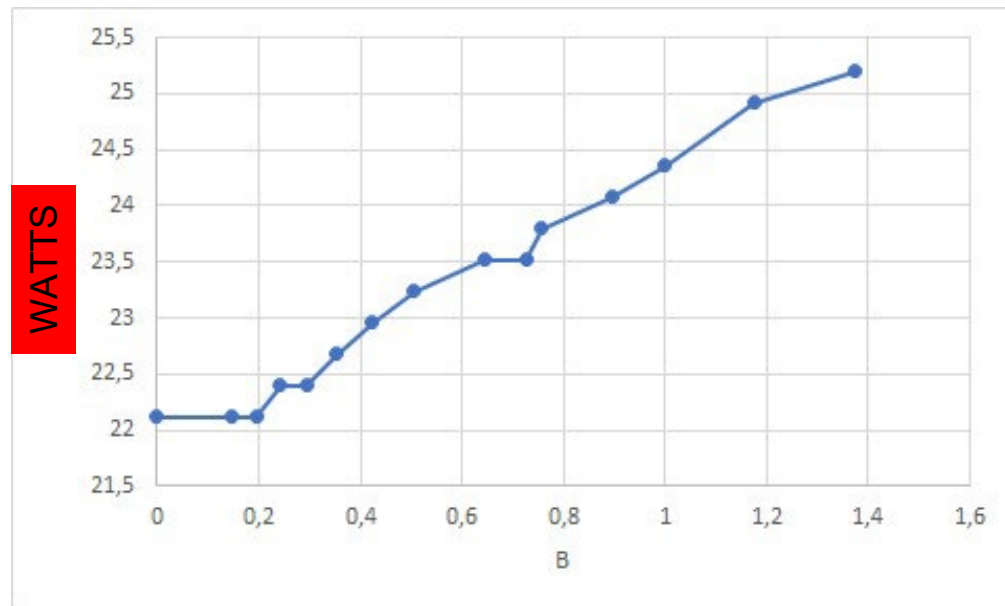
DiRAC V3 B field test

19 July 2022 B test @ Argonne National Laboratory (IL)



DIRAC V3 B field test

- Tested all directions. B ranging from 0T to 1.4T
- Slight power increase at 1T
~10% toward 0T in the
“Mu2e direction”
- Confirm previous results
- Test OK



DiRAC V3 Single Event Effect test

20 - 21 July 2022 SEU test @ North Western Medicine Proton Center Warrenville (IL)



DiRAC V3 SEU test

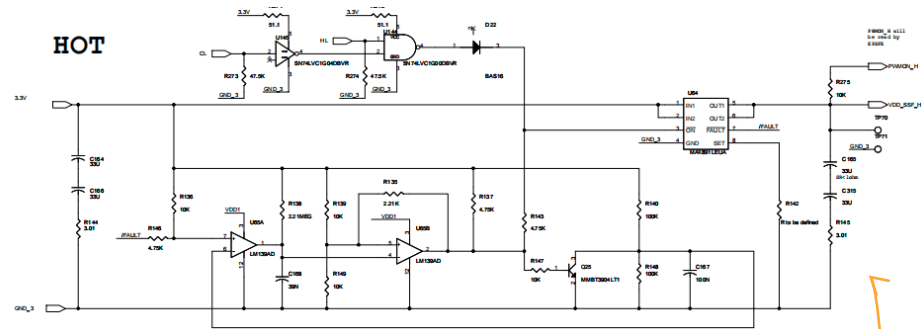
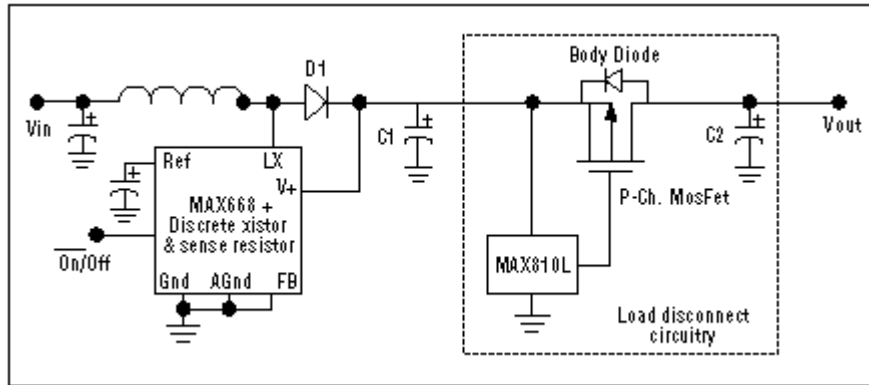
- First night of test:
 - Misunderstanding on the flux intensity ... we asked $1E10$ p/cm²sec uniform on the board and we got a raster beam of 1 cm² moving on the board. Instant intensity of $1E15$ p/cm²sec.
 - After few seconds dataflow stopped and I raised to 0.97A (normally 0.75A) ...smell of fire
 - We verified that the flash component fired (latch-up)
 - After replacing the flash (the day after) the board was again operative

DiRAC V3 SEU test 2

- It night, several hours of test with increasing fluxes, uniform beam all-over the board. Total fluence $\approx 1E10$ p/cm²
- **We saw 4 latch-ups**. Current limited to 0.8 A on the power supply. No damage. The board worked fine again after a power cycle. Current limit was ok to save the board.
- SEU analyses under study (not so important toward latch-up... no evidence at first seen)
- Latch-up is unexpected: almost all components tested at Warrenville by the tracker group
- Mu2e Montecarlo simulations: flux of $1E10$ hadrons/cm² with $E < 20$ MeV in 5 years (including safety factor)
- 1 board breaks every 5 years -> 136 boards -> one board every two weeks. Evaluating 200 MeV toward < 20 MeV
- We need to protect the board with a solid state fuse (SSF)

SSF

SSF: monitor current and shut down power for a short time if it goes over a given threshold



SSF2

- We are evaluating several solutions:
 1. Modify 9th crate board (power distributor)
 2. Add the SSF to the DIRAC (2/ board: one for DIRAC and one for mezzanine)
 - DIRAC v4
 - At the moment seems the preferred solution (9th boards already produced,
can't protect the mezzanine separately ...)

SSF3

- Add to DIRAC: several possibilities, we would prefer an integrated solution.
- e.g TPS26635, but must be qualified ...



TPS2663
SLVSE94F – SEPTEMBER 2018 – REVISED JUNE 2021

TPS2663x 60-V, 6-A Power Limiting, Surge Protection Industrial eFuse

- Rad hard components ... \$\$\$... CERN uses a similar part to TPS26635 but it is not suitable for us ...
- Surely we need to produce another version of the prototype ...

Budget requests

- Several solutions under study ...

prototipo scheda DIRAC V4, necessita di aggiungere circuito di protezione da latch-up dopo test di SEU con protoni 200 MeV	15.00	0.00
componenti aggiuntivi per produzione schede DIRAC V4, per la realizzazione del circuito di protezione 150 euro x (160 schede + 20 % spare) . SJ a test aggiuntivo con protoni 200 MeV e neutroni 14 MeV	0.00	25.00
estensione RAM a 4 Gbit per produzione DIRAC. SJ a reale necessita' se evidenziata da MC ulteriori	0.00	6.00
prototipo scheda TRAD V2, aggiornamento per aggiunta circuito di protezione, 1 K SJ per eventuale costo componenti aggiuntivi	3.00	1.00

- V4: we know with precision: 19K all inclusive. We already have some components in hands
- Production update: SJ to technical choice (100 euro/board + VAT as a first try)
- Same for TRAD (v1 needs some small mods anyway)
- Tracker recently doubled RAM buffer from 2 to 4 Gbit. ECAL could need the same. Waiting for new Montecarlo sim. PCB already compatible. SJ to MC