Power supply per Fisica delle Alte Energie: problematiche e soluzioni innovative

B.Allongue[1], G.Blanchot[1], S.Buso[2], F.Faccio[1], C.Fuentes[1,3], P.Mattavelli[2], S.Michelis[1,4], S.Orlandi[1], G.Spiazzi[2]

[1]CERN – PH-ESE

[2]Dept. Information Engineering, Padova University, Italy

[3]UTFSM, Valparaiso, Chile

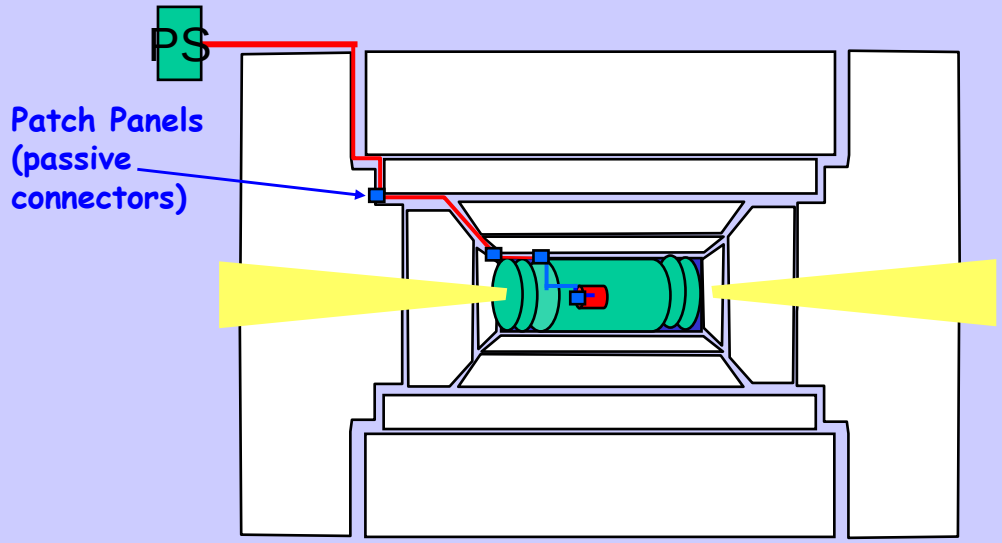
[4]EPFL, Lausanne

Outline

- Present power distribution architectures at LHC experiments
- Expected power supply requirements for the future LHC upgrade
- Serial powering
- Parallel powering: DC-DC converters based solution
  - DC-DC converter topologies for Point of Load (POL) converters
- Conclusions

Present Power Distribution Schemes in Trackers (ATLAS)

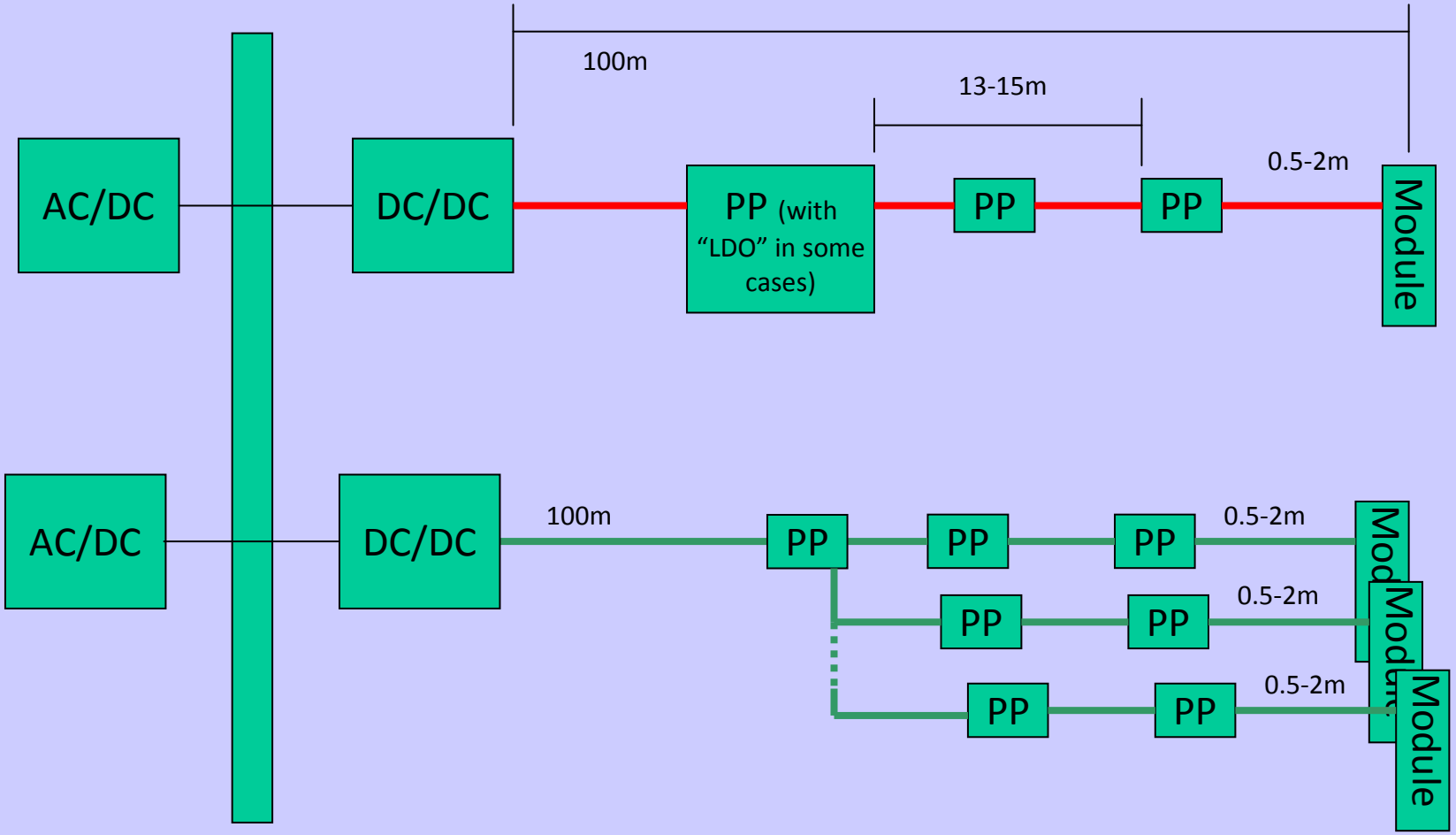
Typical low-voltage power distribution in LHC trackers:
No on-detector conversion. Low-voltage (2.5-5V) required by electronics provided directly from off-detector. Sense wire necessary for PS to provide correct voltage to electronics. Cables get thinner when approaching the collision point (strict material budget).



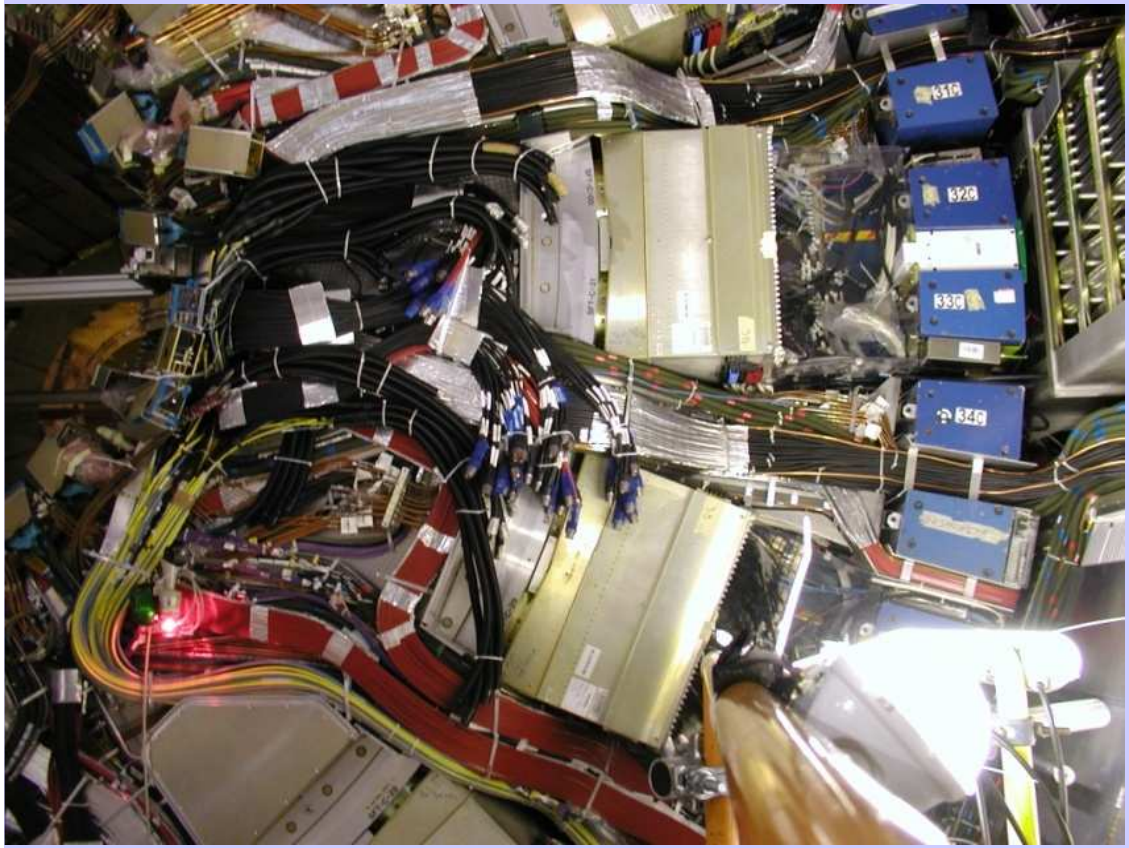
In view of SLHC:
-Scheme not easily scalable to the larger currents expected (see next slides)

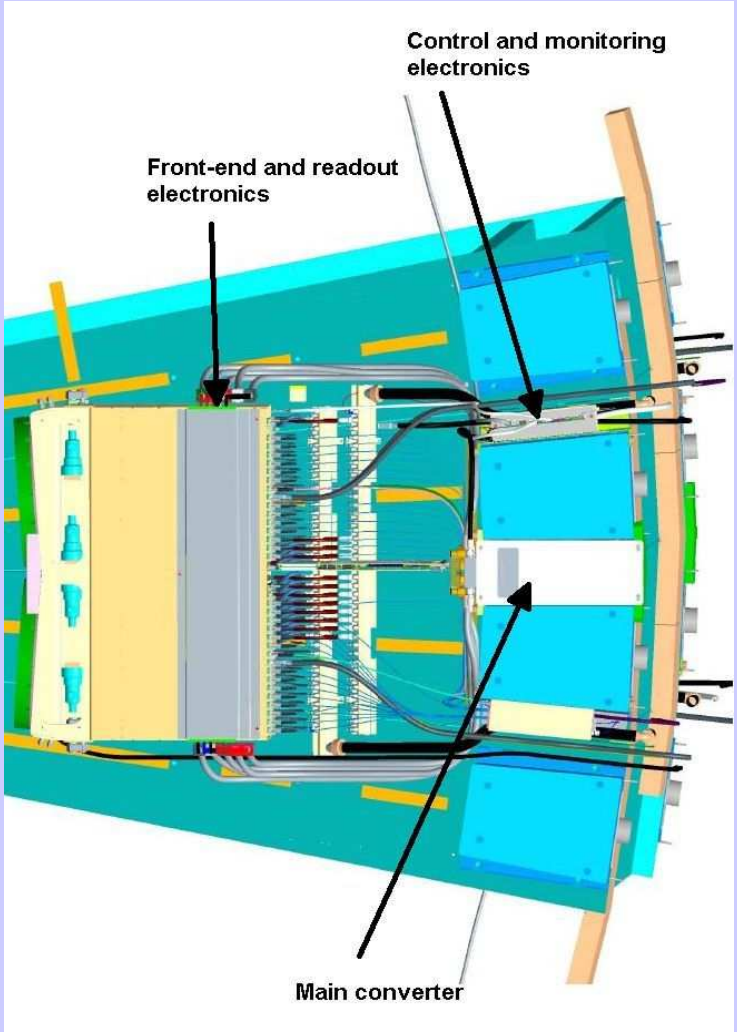
Present Power Distribution Schemes in Trackers (ATLAS)

1A/channel (analog or digital), round-trip cables, and sense to nearest regulation



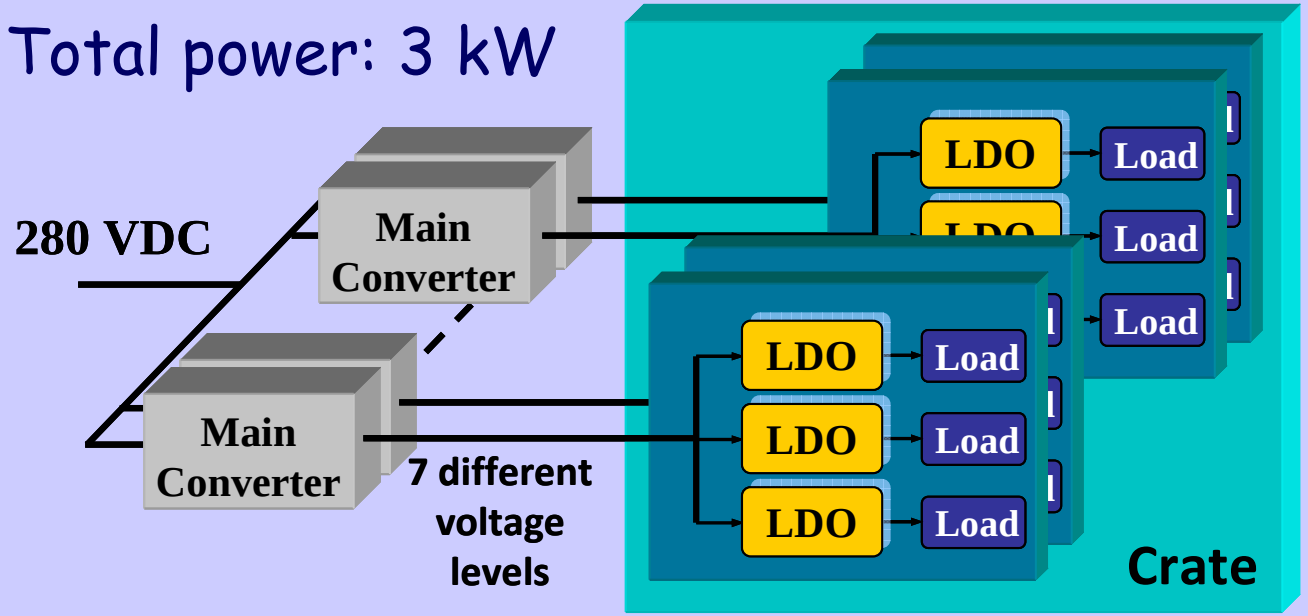
Example: LAr Calorimeter Power Supply





Example: LAr Calorimeter Power Supply

Total power: 3 kW

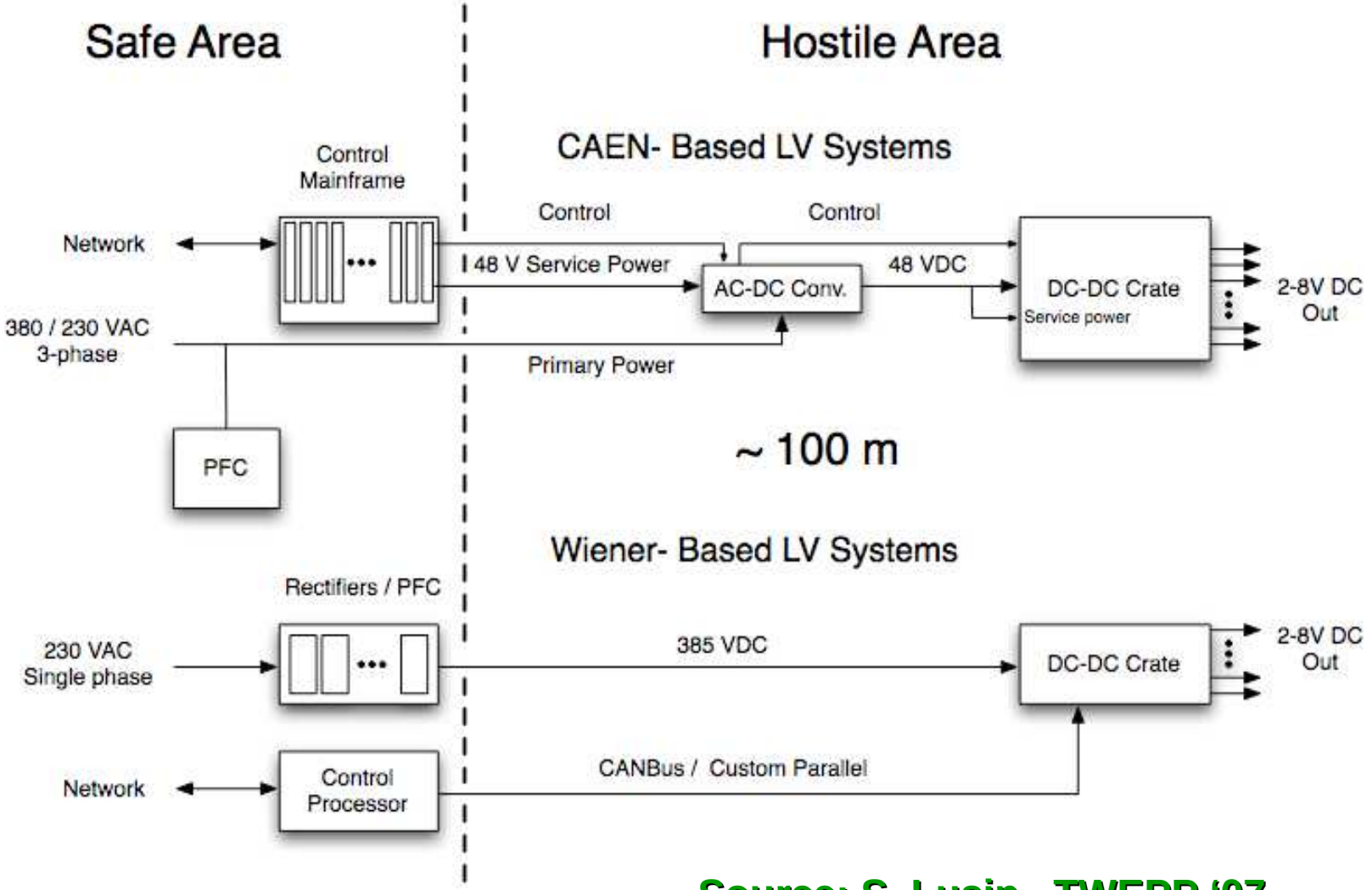


Output voltages:

V_{out1} = +6V – 100A
V_{out2} = +11V – 20A
V_{out3} = +7V – 160A
V_{out4} = +6V – 150A
V_{out5} = +4V – 130A
V_{out6} = -4V – 180A
V_{out7} = +7V – 15A

Low Drop-Out (LDO) regulators on board

Example: CMS Power Supply Architectures



Source: S. Lusin, TWEPP '07

Why independent powering fails at SLHC ?

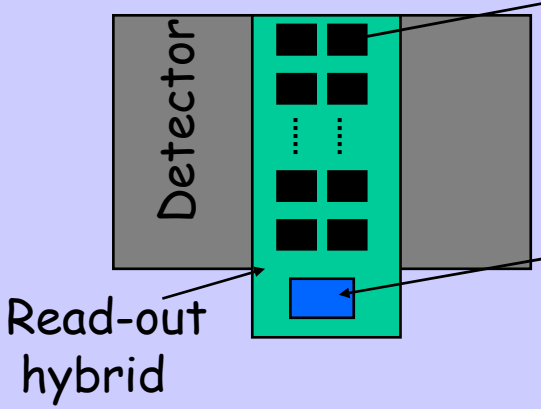
- Don't get 5 or 10 times more cables in
- Power efficiency is too low (50% ATLAS SCT ⇔ ~15% SLHC)
- Cable material budget
- Packaging constraints

Source: M. Weber, TWEPP '07

Example: ATLAS Tracker

All ASICs will be manufactured in an advanced CMOS (or BiCMOS) process, 130nm generation or below. Here we consider only CMOS ASICs.

Detector module



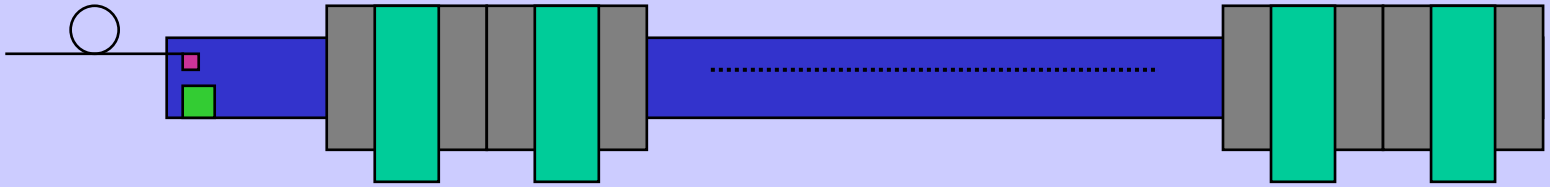
Front-End readout ASIC

- $I_{digital} \geq I_{analog}$ (for instance, current projection for ATLAS Short Strip readout is I_{analog} ~ 20mA, $I_{digital}$ ~ 60-100mA)
- 2 power domains: V_{an}=1.2V, V_{dig}=0.9-0.8V (as low as possible)
- Clock gating might be used => switching load

Hybrid/Module controller

- Ensures communication (data, timing, trigger, etc.)
- Digital functions only
- It might require I/Os at 2.5V

Rod/stave



Other than the rod/stave controller, optoelectronics components will also have to be used, requiring an additional power domain (2.5-3V)

Source: S. Michelis, TWEPP '07

Example: ATLAS Tracker

Summary

- 3 Voltages to be provided to minimize power consumption:
  - 2.5V for optoelectronics and (maybe) control/communication ASICs
  - 1.2V for analog circuitry in FE ASICs
  - 0.8-0.9V for digital circuitry in FE ASICs. This domain uses most of the current!
- Digital current might be switching in time (to really minimize the power)

Power and Current in LHC/SLHC

- Projection based on current estimate for ATLAS upgrade
- Only accounting barrel detector, power from Readout ASICs only
- SCT is LHC ATLAS Silicon Tracker detector, to be replaced (grossly) by Short Strip layers in present upgrade layout

	N of layers	Min and Max R (cm)	Barrel length (cm)	N of chips	N of hybrids	Active power (KW)	Load current (KA)
SCT barrel	4	30, 51	153	25,000	2100	11.6	2.75 (@3.5-4V)
SLHC SS layers, barrel	3	38, 60	200	173,000	8600	16.2 (@0.9-1.2V) 20.3 (@1.2V)	17.2 (@0.9-1.2V)

Large waste of power if $V_{an}=V_{dig}=1.2V$

Large current increase (Power on cables = RI^2)

Source: S. Michelis, TWEPP '07

Working Environment

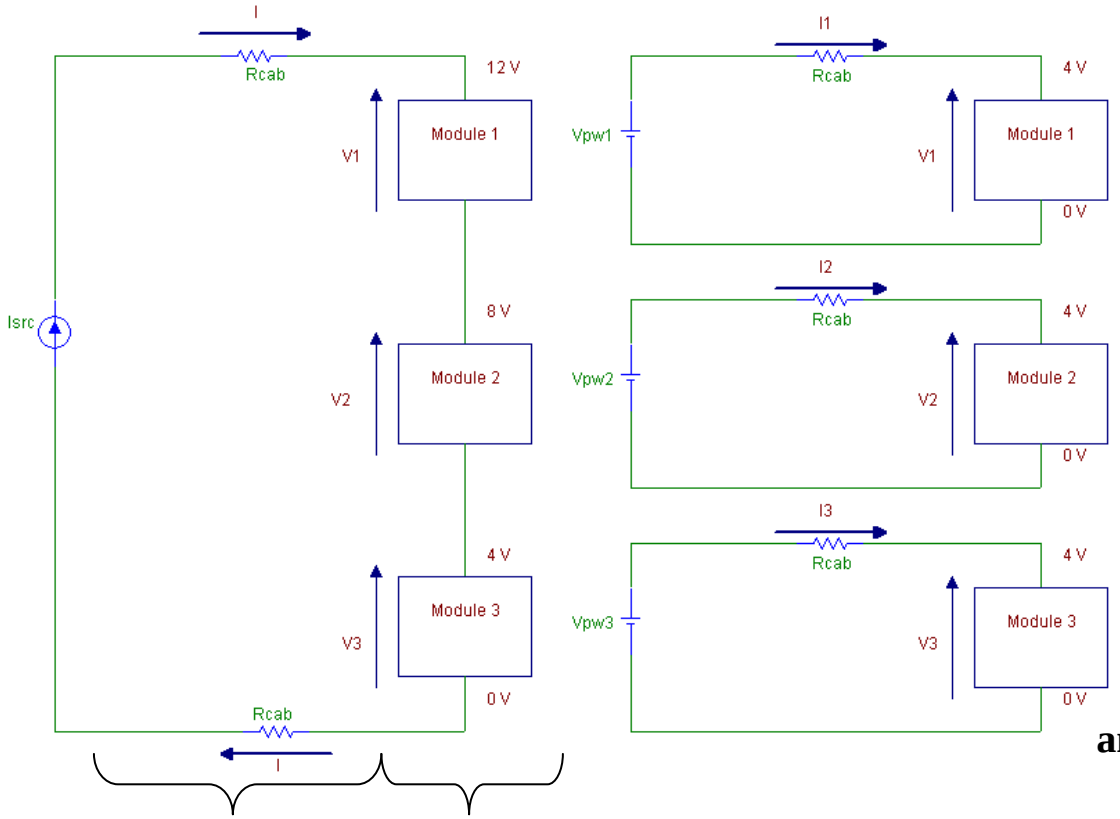
- High magnetic field (up to 4T in CMS, 2T in ATLAS)
- High level of radiation inside the detectors:
  - LHC doses probably increased x 5 – 10 so we can extrapolate to hundreds of Mrad in several Tracker location, decreasing to ten(s) in the outer Trackers

Power Distribution Schemes

- Serial Powering (SP)
  - Shunt regulators
- Parallel Powering (PP)
  - Inductor-based switching converters
  - Switched capacitor converters

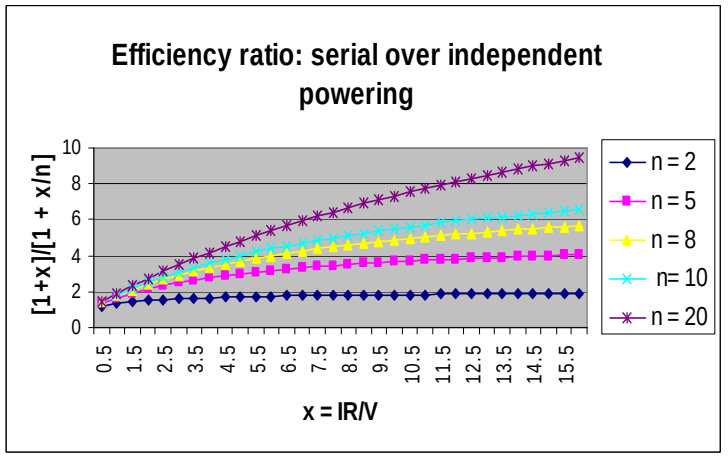
Serial Powering

Powering schemes comparison



$P_c = I_m^2 Rc$ $P_M = nI_mV_m$

Efficiency:= $\eta := \frac{P_M}{P_M + P_C} = \frac{1}{1 + \frac{I_m R_C}{nV_m}} = \frac{1}{1 + \frac{x}{n}}$

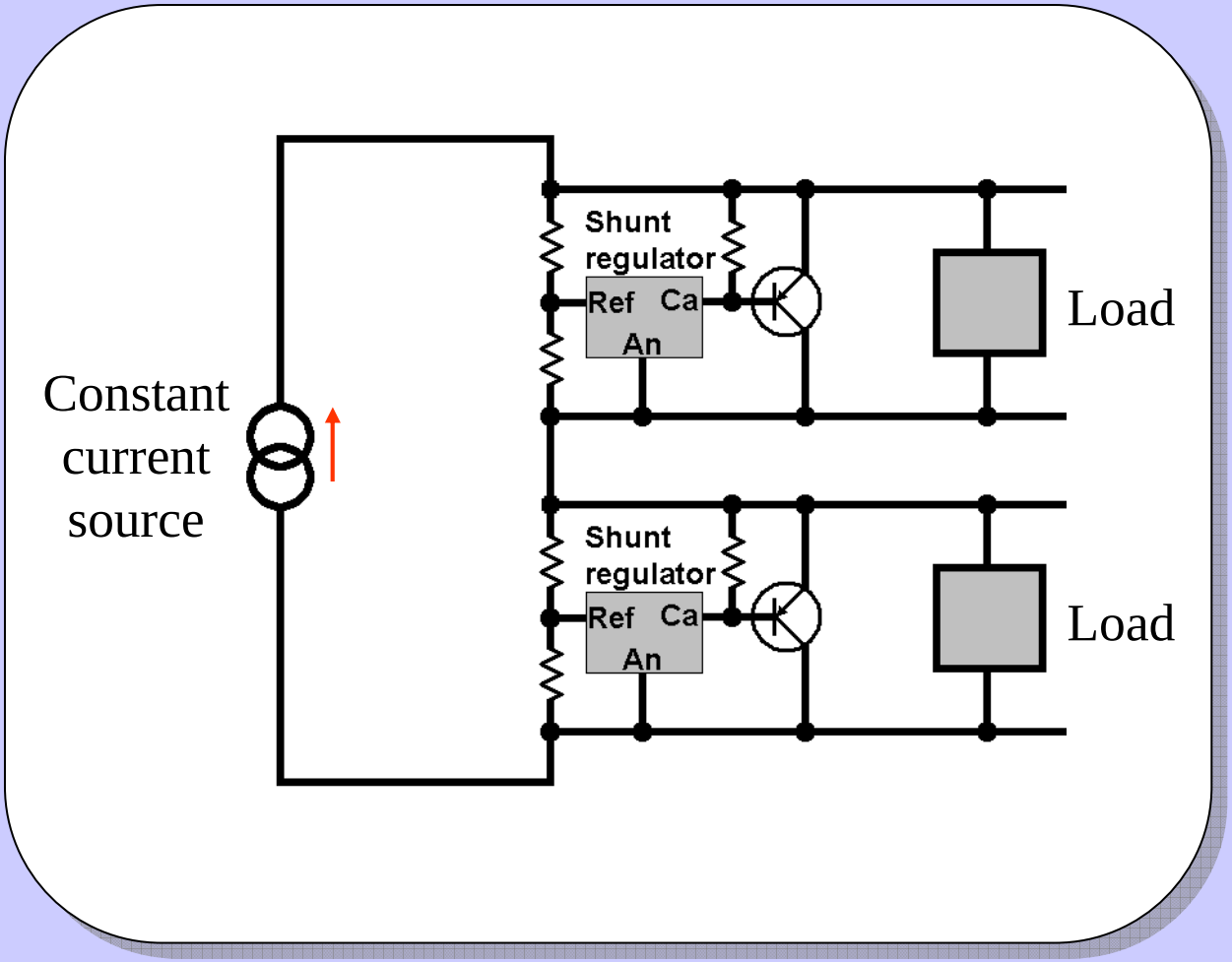


Example of efficiency plot vs. number of modules (n) and supply voltage (V) for I_m = 2 A R_c = 3 Ω for Serial Powering scheme

Source: G. Villani, TWEPP '07

Shunt Regulation in SP

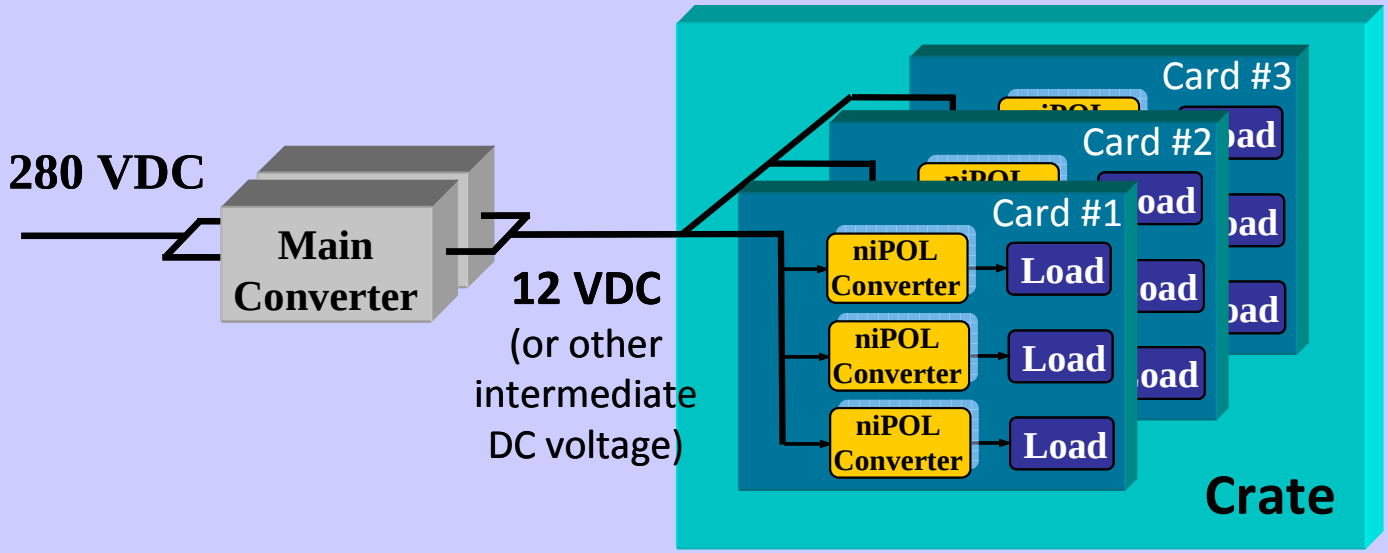
External shunt regulator + external power transistor



Source: G. Villani, TWEPP '07

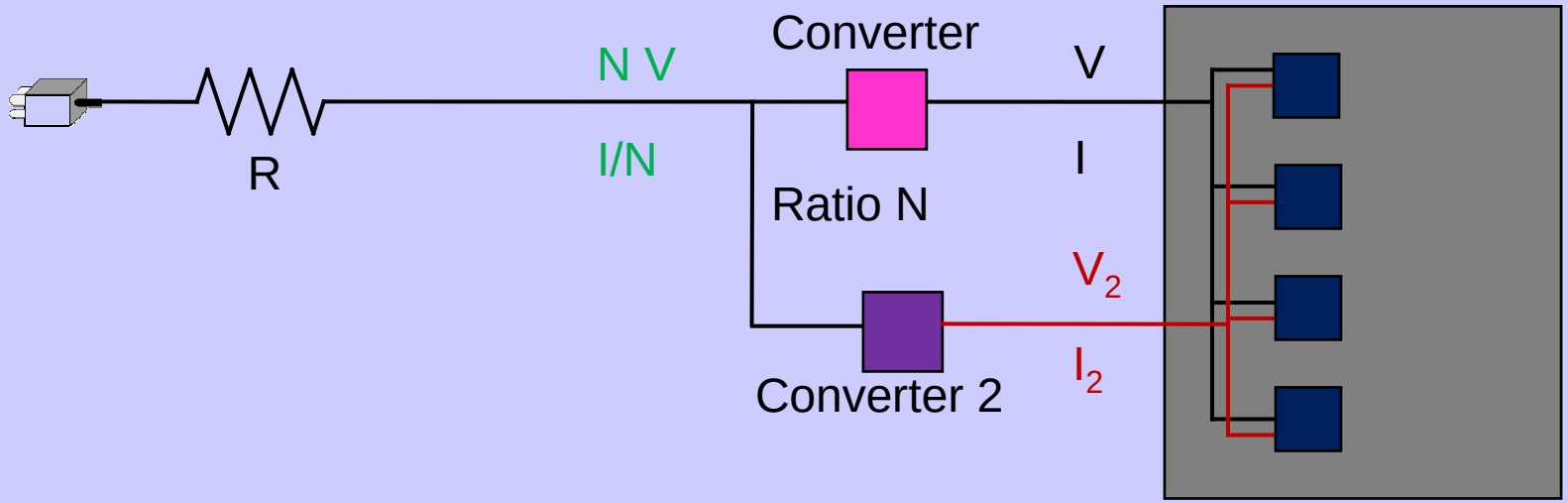
Parallel Powering

Example of LAr calorimeter power supply



niPOL = Non-Isolated Point of Load Converters

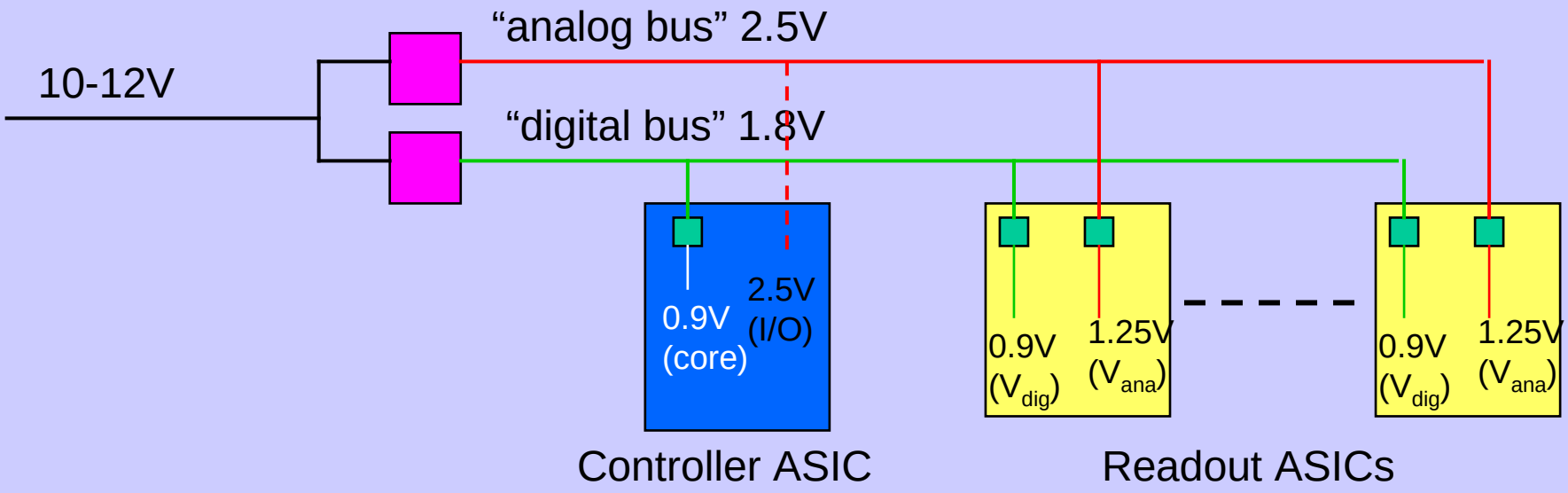
Reduction of Cable Power Losses



Solution without converter: ↓ Power losses on cable = RI^2

Solution with converter: ↑ Power losses on cable = $R\left(\frac{I}{N}\right)^2 = \frac{RI^2}{N^2}$

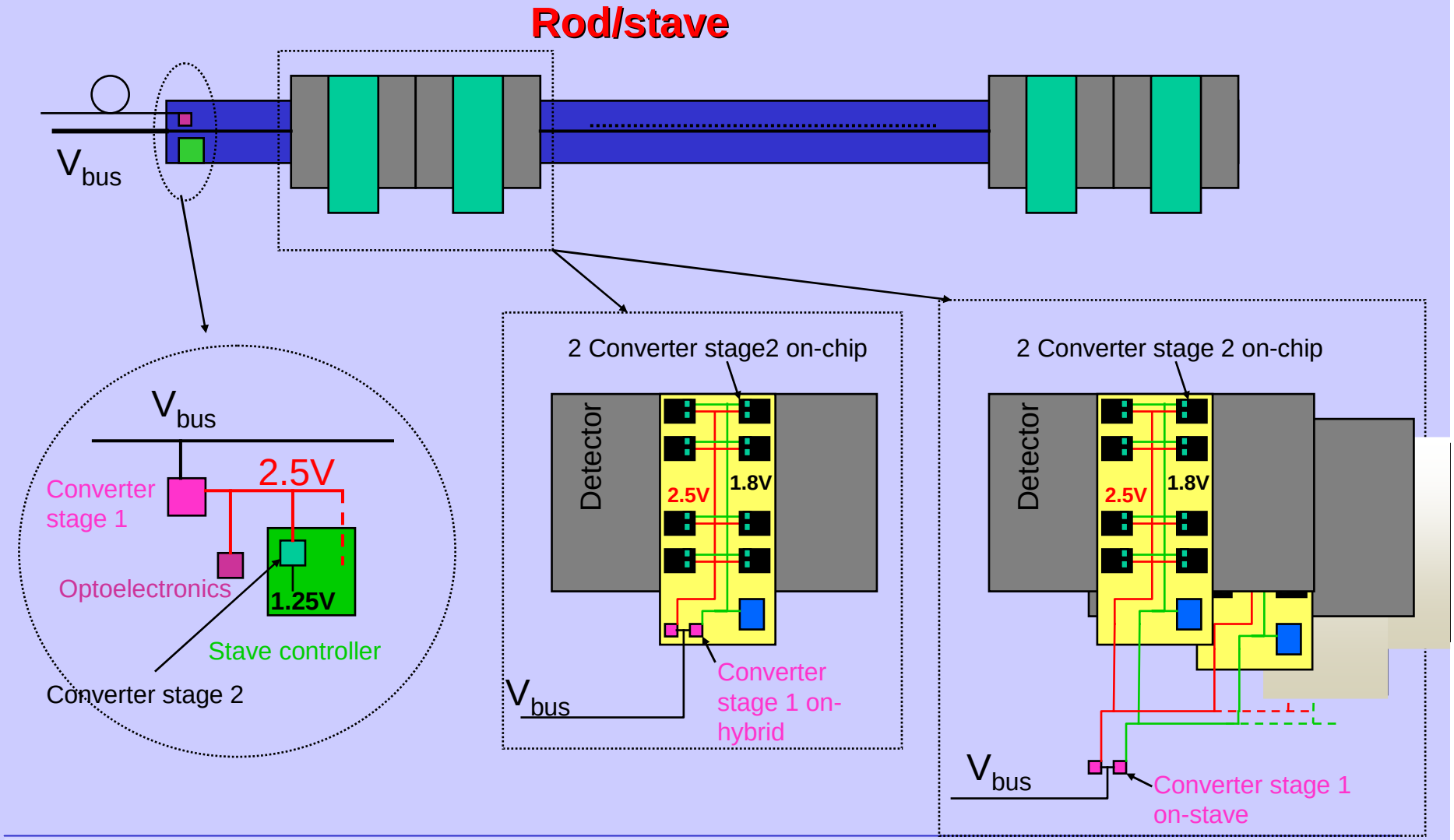
Proposed Power Distribution Scheme for ATLAS Trackers



Conversion stage 1 (ratio 4-5.5)
-Vin=10V => high-V technology
-Same ASIC development for analog and digital

Conversion stage 2 (ratio 2)
- Embedded in controller or readout ASIC
- Closely same converter for analog and digital (different current, hence different size of switching transistors): macros (IP blocks) in same technology

Implementation Example



Power supply for ATLAS Trackers

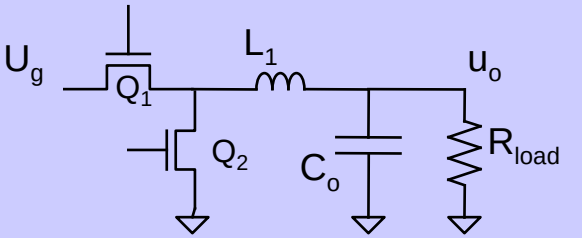
- The high magnetic field calls for coreless conversion stages
- Low-value air core inductors can be used with switching frequencies in the megahertz region
- Inductor-less conversion stages can also be used (switched capacitor converters)
- Switching noise is a big concern

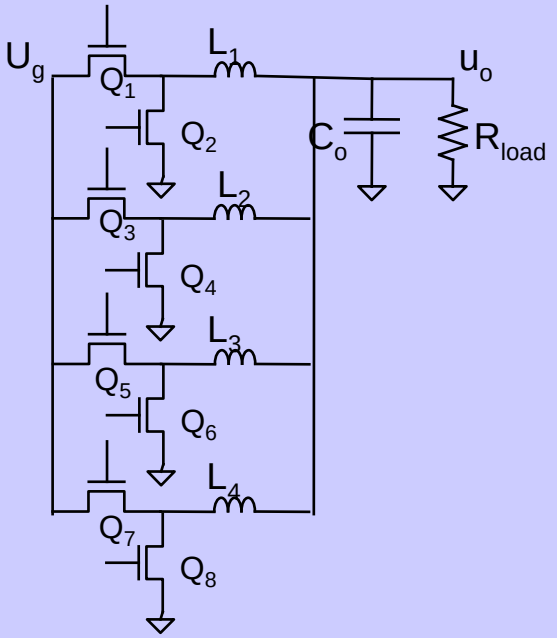
Soft-switching is a must!

Different Converter Topologies (1/3)

1. **Single phase synchronous buck converter**
   - ↑ Simple, small number of passive components
   - ↓ Larger output ripple for same C_o
   - ↓ RMS current limitation for inductor and output capacitance

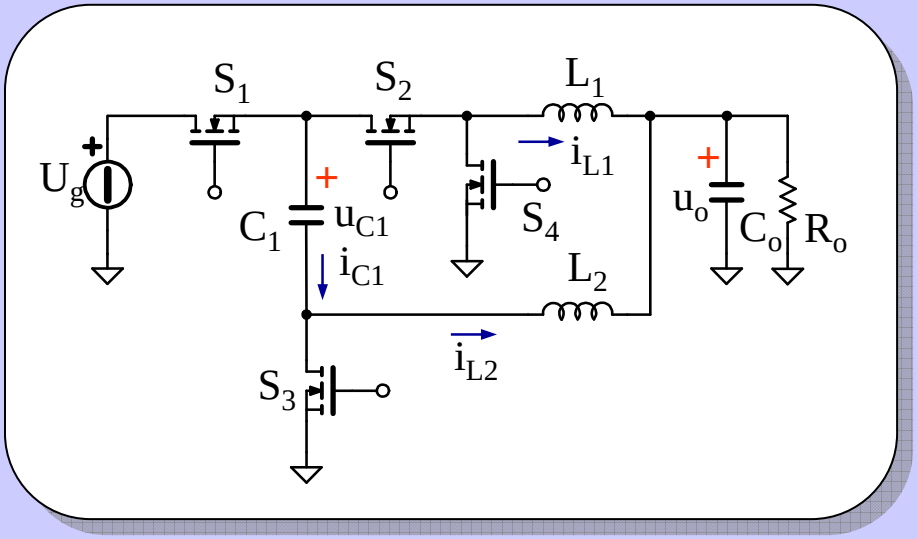
2. **4 phase interleaved synchronous buck converter**
   - ↑ Complete cancellation of output ripple for a conversion ratio of 4 (with small C_o)
   - ↑ Smaller current in each inductor (compatible with available commercial inductors)
   - ↓ Large number of passive components
   - ↓ More complex control circuitry



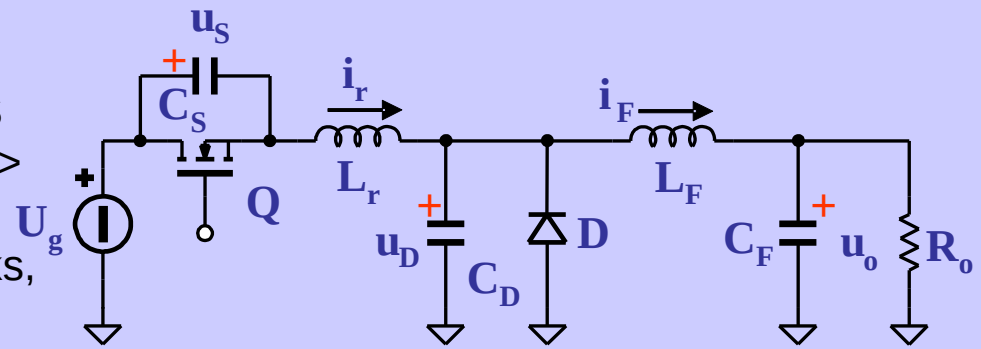


Different Converter Topologies (2/3)

3. **Two phase interleaved synchronous buck converter with integral voltage divider**
   - ↑ Complete cancellation of output ripple for a conversion ration of 4 (with small C_o)
   - ↑ Simpler control and smaller number of passive components than 4 phase interleaved
   - ↓ More components than the single-phase synchronous buck

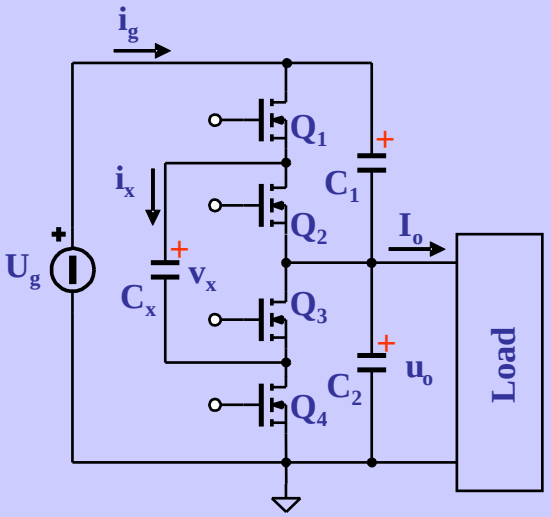


4. **Multi-resonant buck converter**
   - ↑ Very small switching losses (zero voltage and zero current switching)
   - ↓ To achieve resonance:
     - Current waveforms have high RMS value => large conduction losses => lower efficiency
     - Voltage waveforms have high peaks, possibly stressing the technology beyond max V_{dd}
   - ↓ Different loads require complete re-tuning of converter parameters



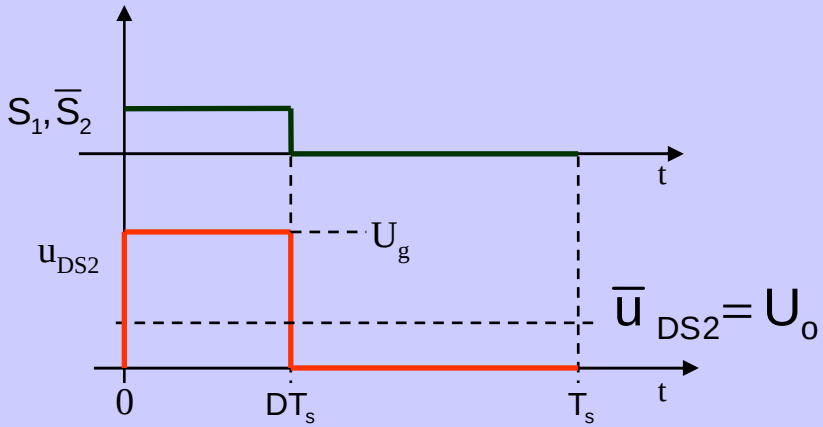
Different Converter Topologies (3/3)

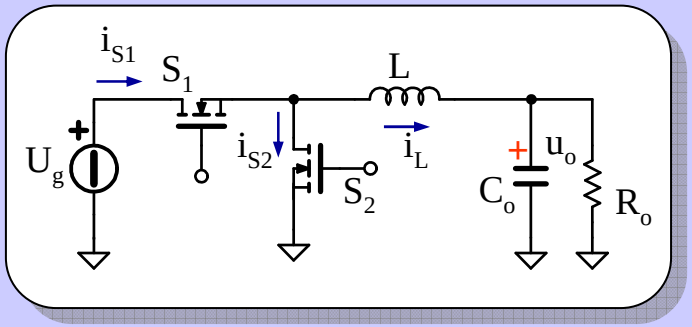
5. **switched capacitor voltage divider**
   - ↑ rather simple, limited number of passive components
   - ↑ lack of inductor => good for radiated noise and for compact design
   - ↓ No regulation of the output voltage, only integer division of the input voltage
   - ↓ Efficiency decreases with conversion ratio (larger number of switches)
   - ↑ Good solution for ratio = 2, for which high efficiency can be achieved



Single-phase Synchronous Buck Converter

Principle of operation

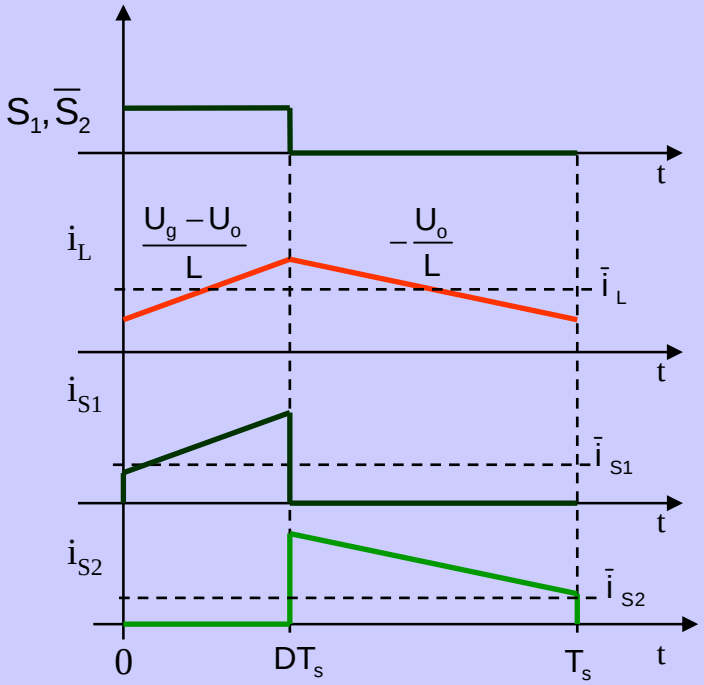


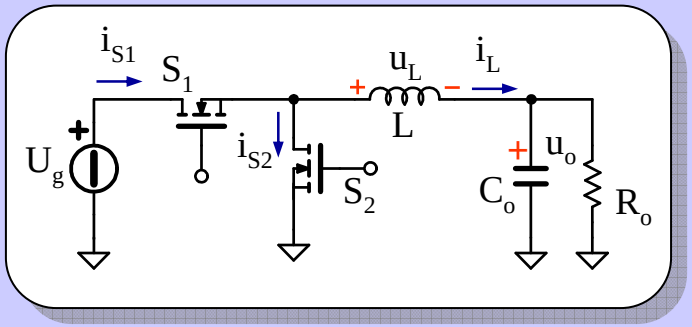


The 2°order L-C_o filter removes the switching frequency harmonics, making the output voltage DC component dominant

Single-phase Synchronous Buck Converter

- Hp: constant voltages



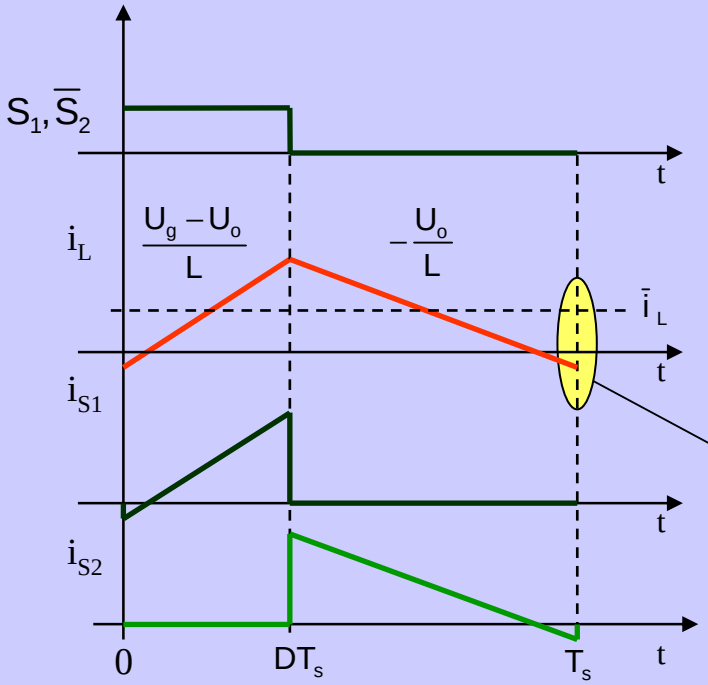


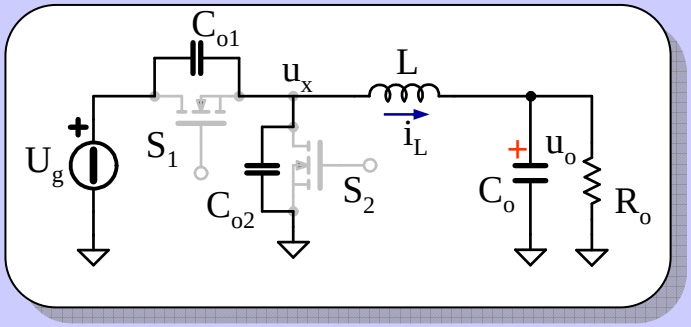
Inductor flux balance:

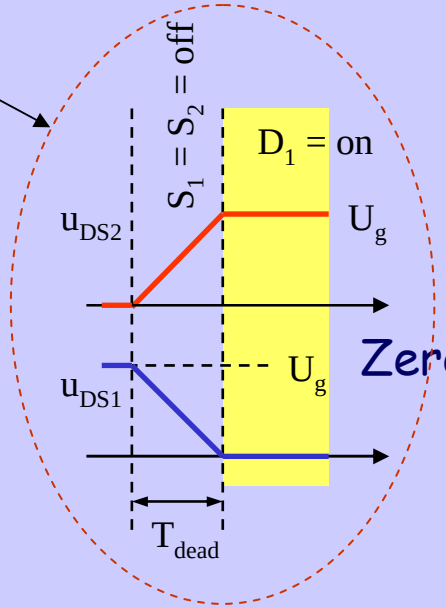
$$\bar{u}_L = 0 \quad \Rightarrow \quad (U_g - U_o)D - U_o(1-D) = 0 \quad \Rightarrow \quad M = \frac{U_o}{U_g} = D$$

Single-phase Synchronous Buck Converter

- Quasi-square wave operation



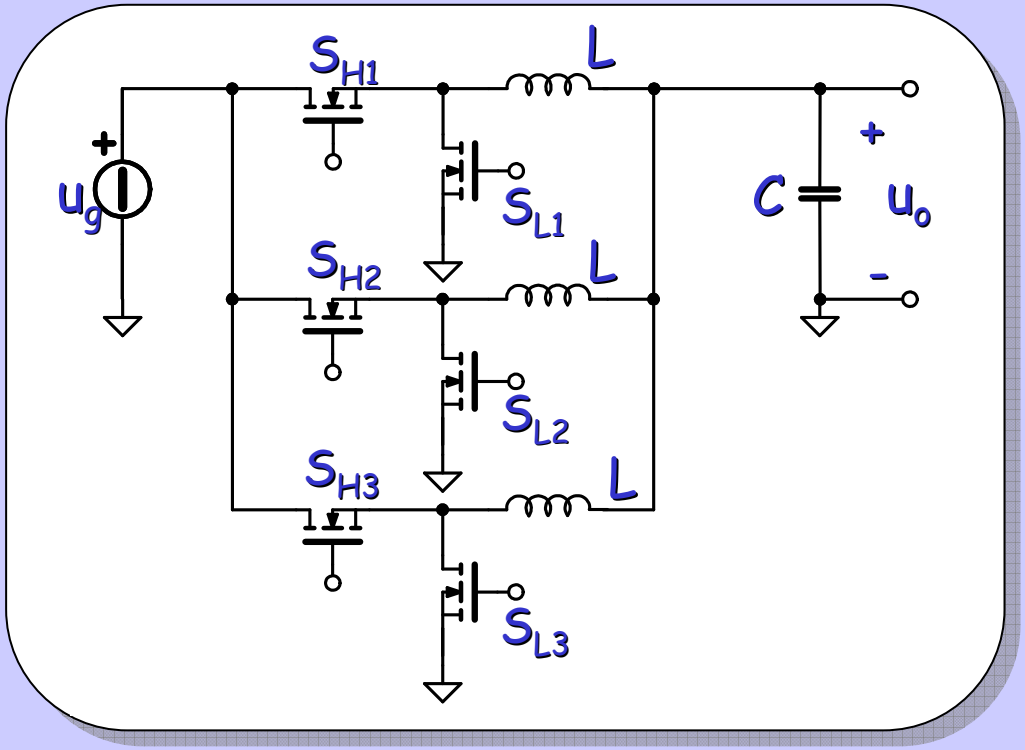




Zero Voltage Switching turn on

High current ripple

Multiphase Interleaved Buck Converters

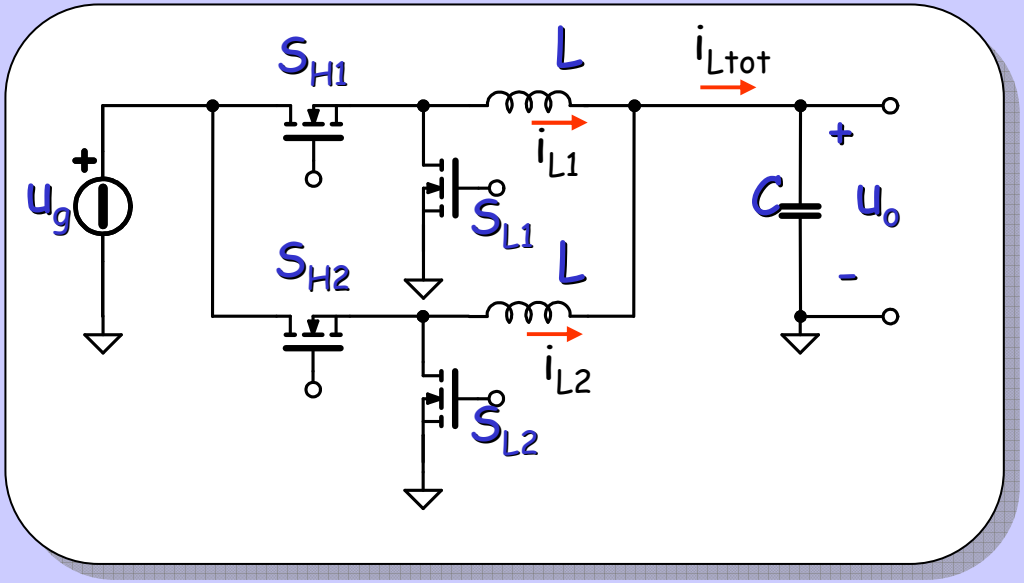


N = phase number

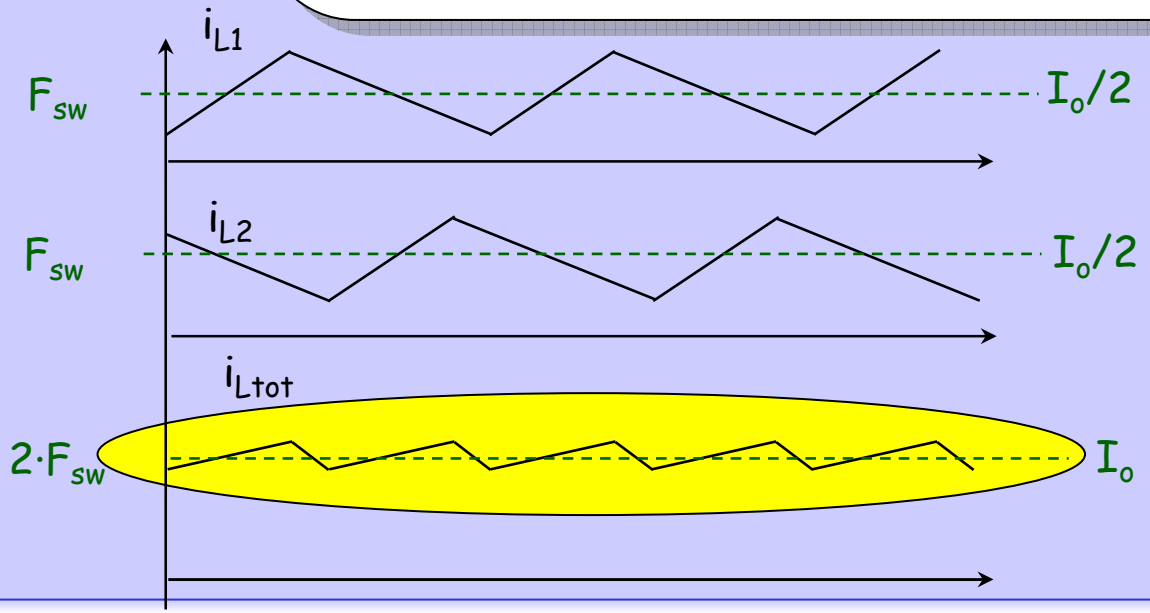
Same drive signal but phase shifted by T_{sw}/N

- Reduced current level per phase
- Reduced output current ripple
- Reduced input current ripple
- Increased bandwidth ($F_{eq}=N\,F_{sw}$)

Multi-Phase Interleaved Converters



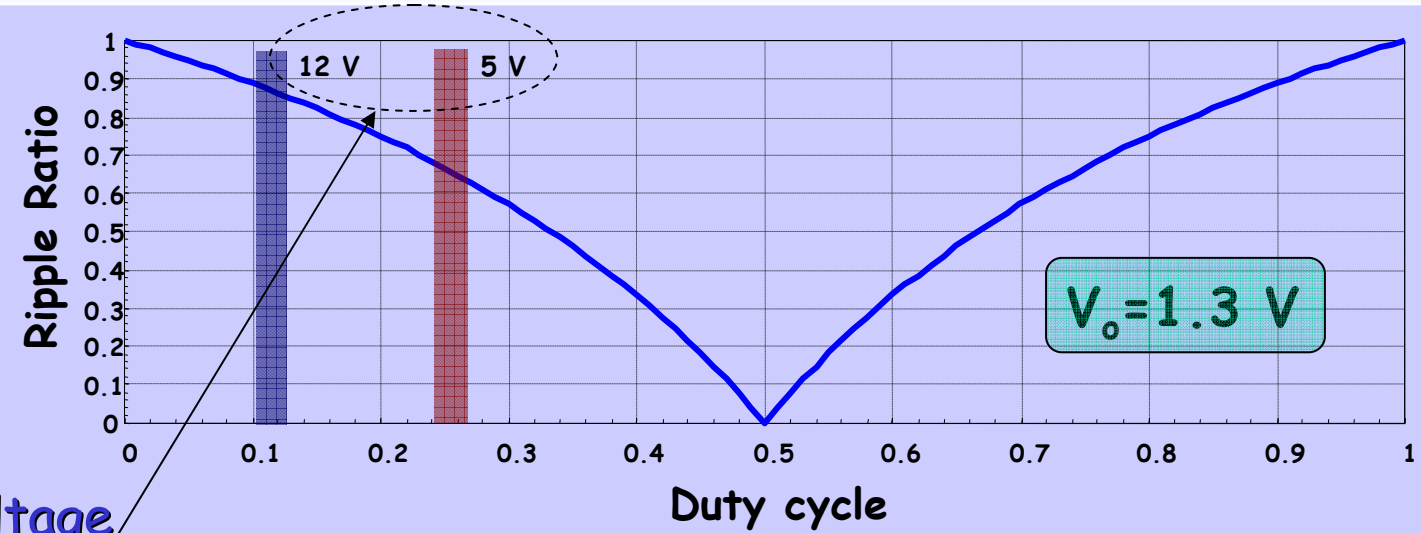
Example:
2 phases



Ripple reduction on output filter

Output Current Ripple Cancellation

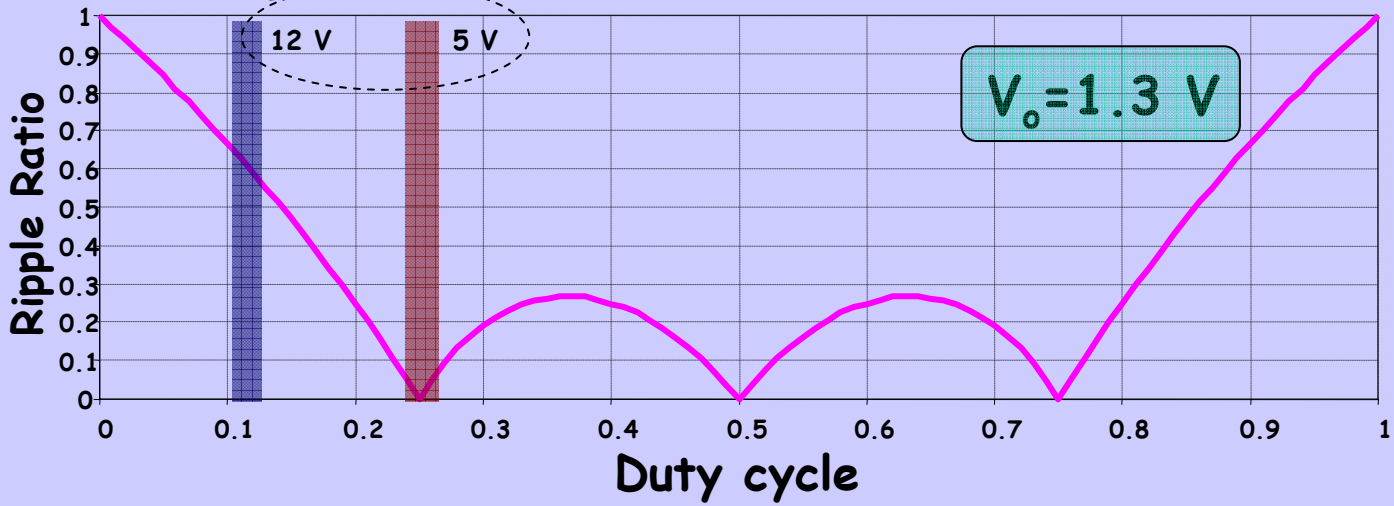
Two phases



Input voltage

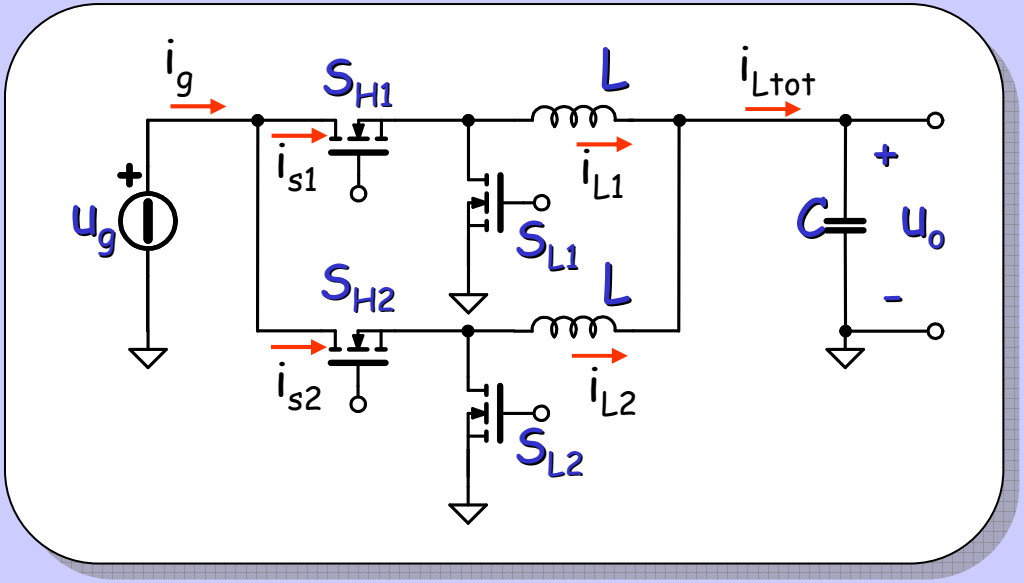
D=0.5 for the best cancellation effect

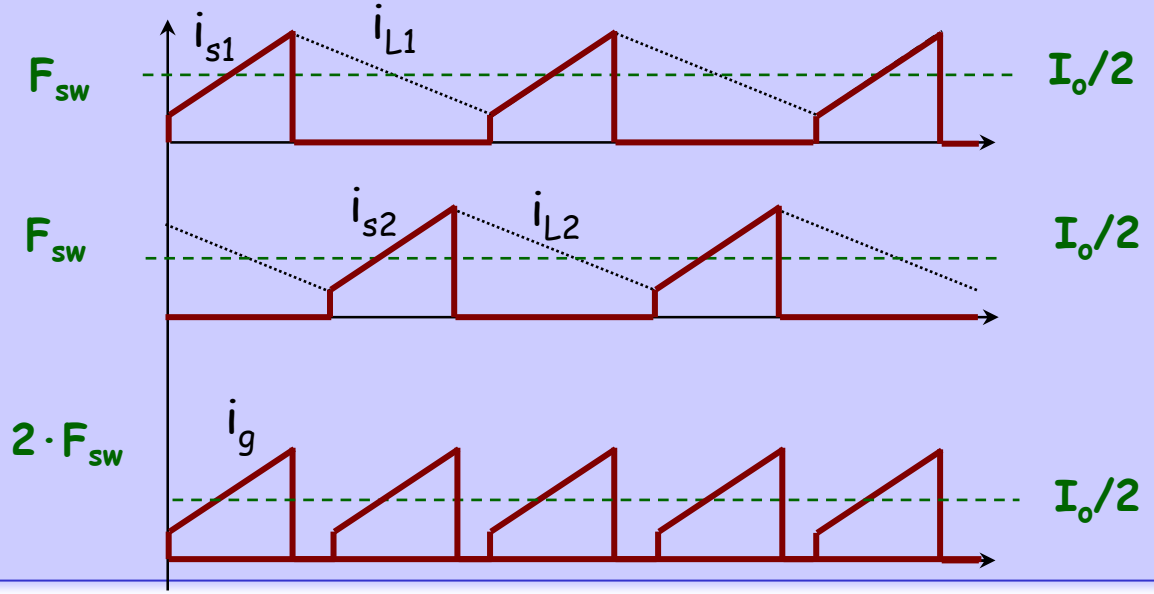
Four phases



D=0.25, 0.5, 0.75 for the best cancellation effect

Multi-Phase Interleaved Converters



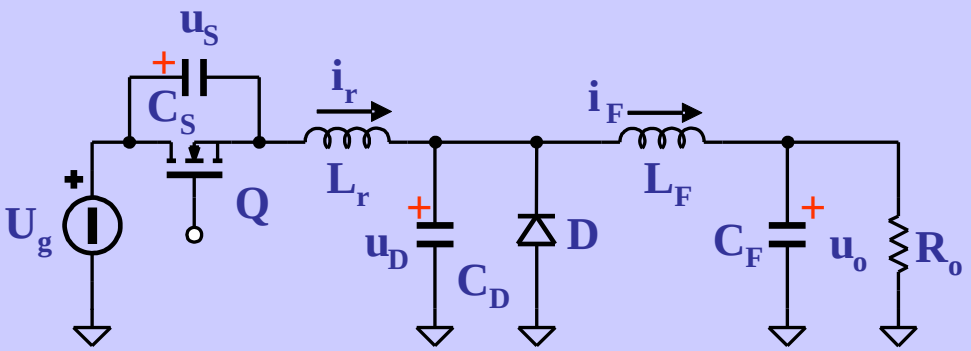


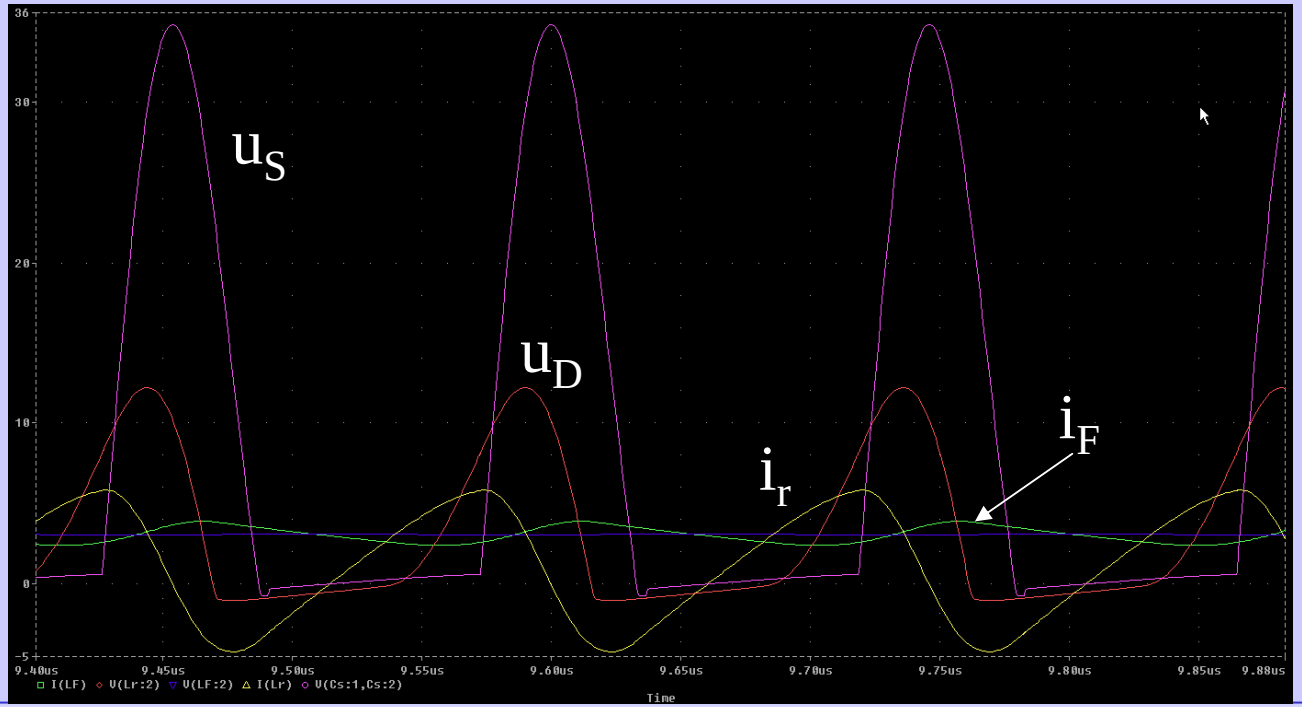
Ripple reduction on input current

Multi-resonant buck converter

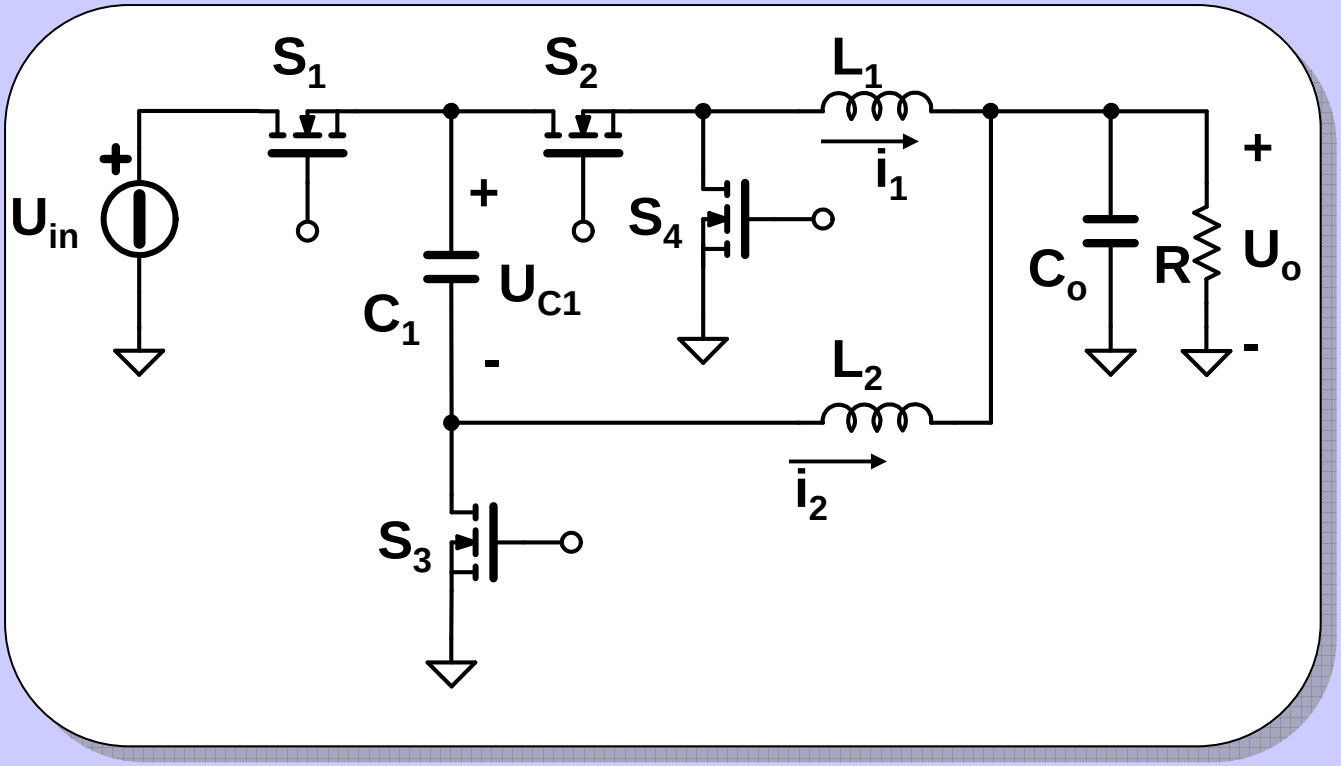
Example:

Input voltage:	$U_g = 12V$
Output voltage:	$U_o = 3V$
Output current:	$I_o = 3A$
Switching frequency:	$f_S = 6.4MHz$
Resonant inductance:	$L_r = 100nH$
Switch capacitance:	$C_S = 3nF$
Diode capacitance:	$C_D = 9nF$



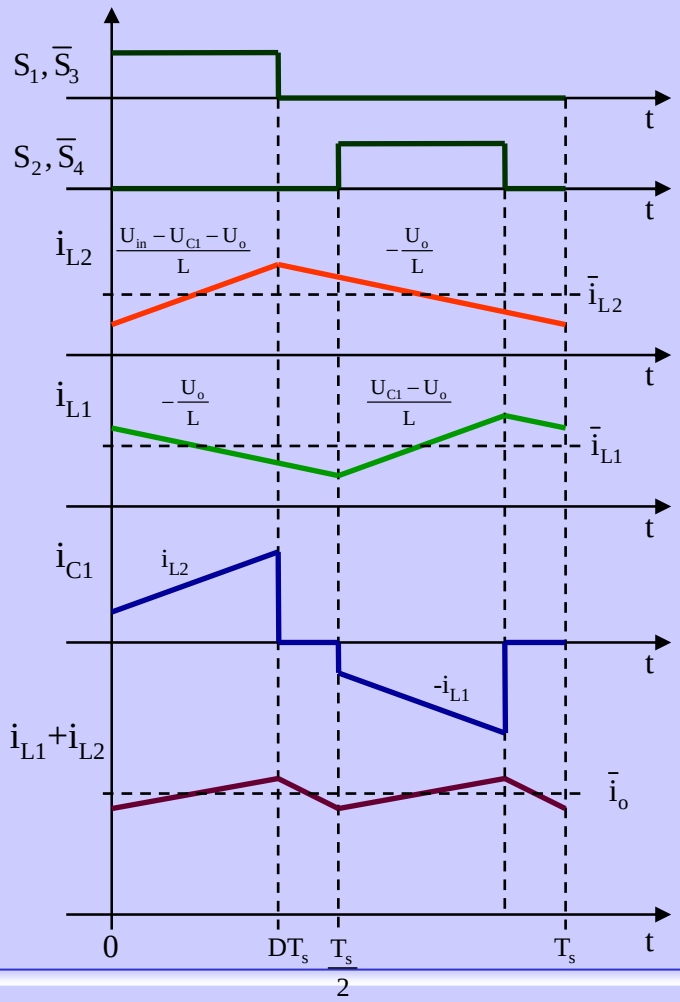


Two-Phase Interleaved Buck with Voltage Divider

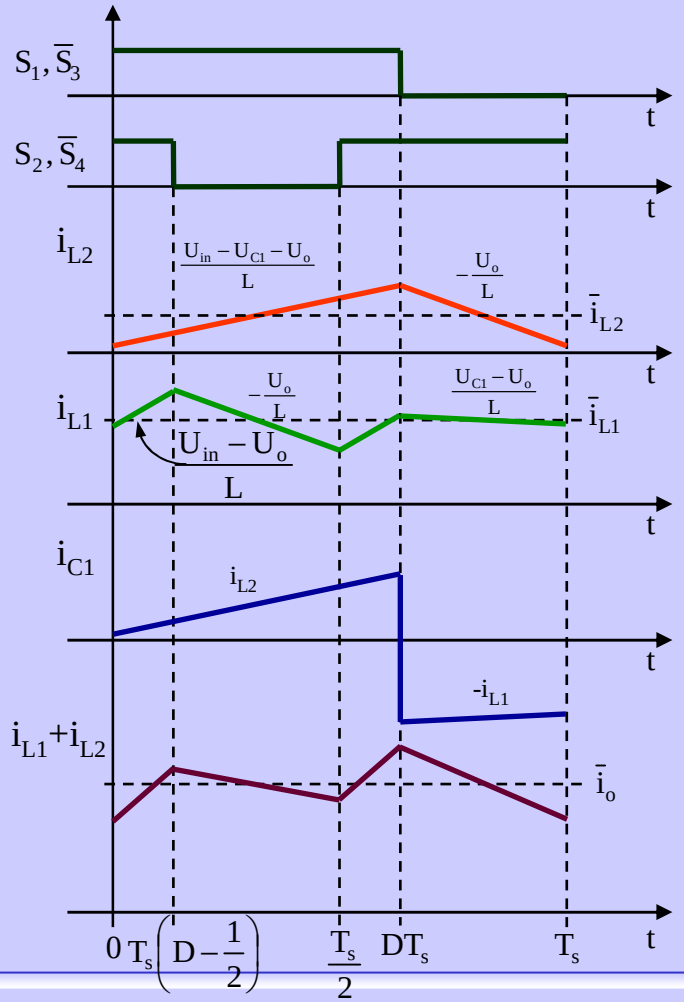


Two-Phase Interleaved Buck with Voltage Divider

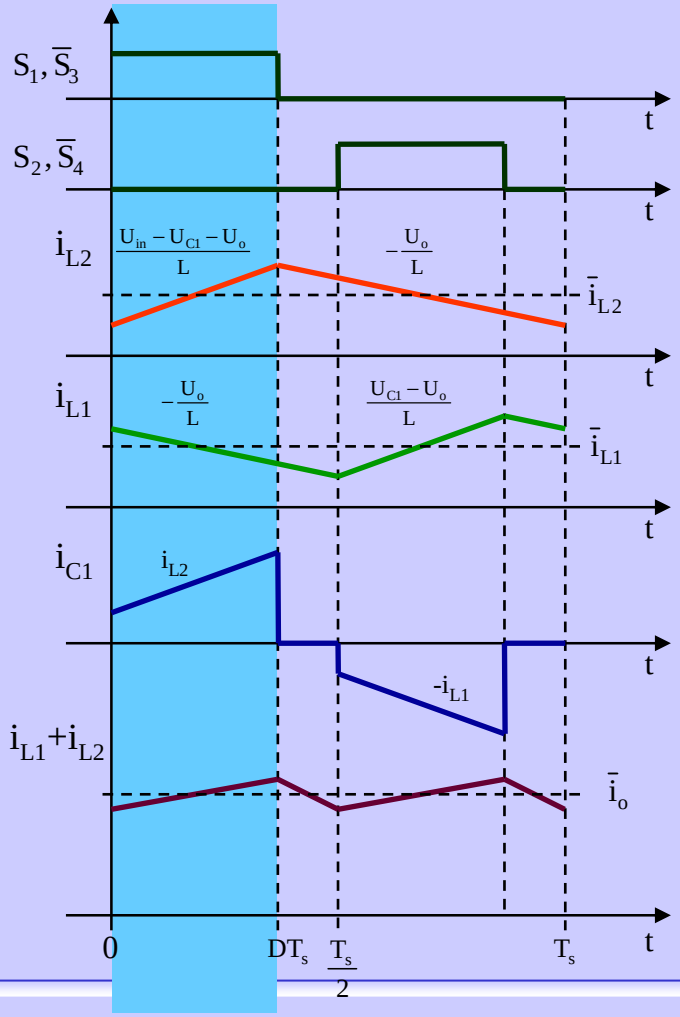
D<0.5

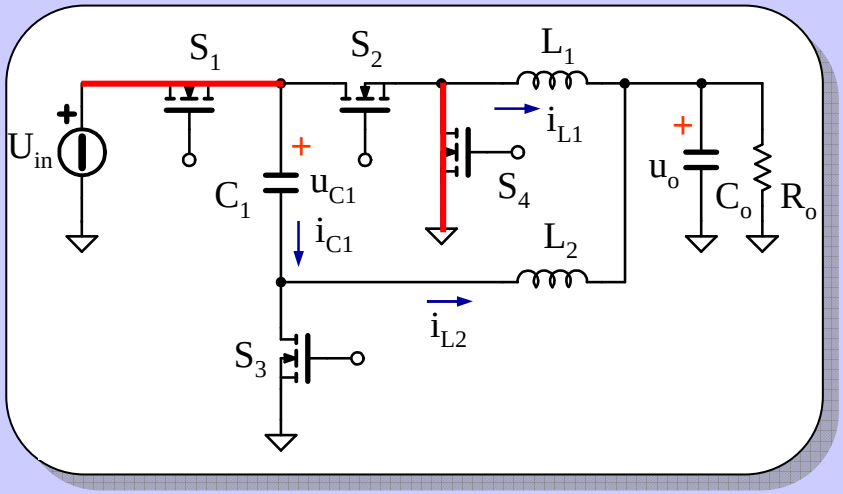


D>0.5

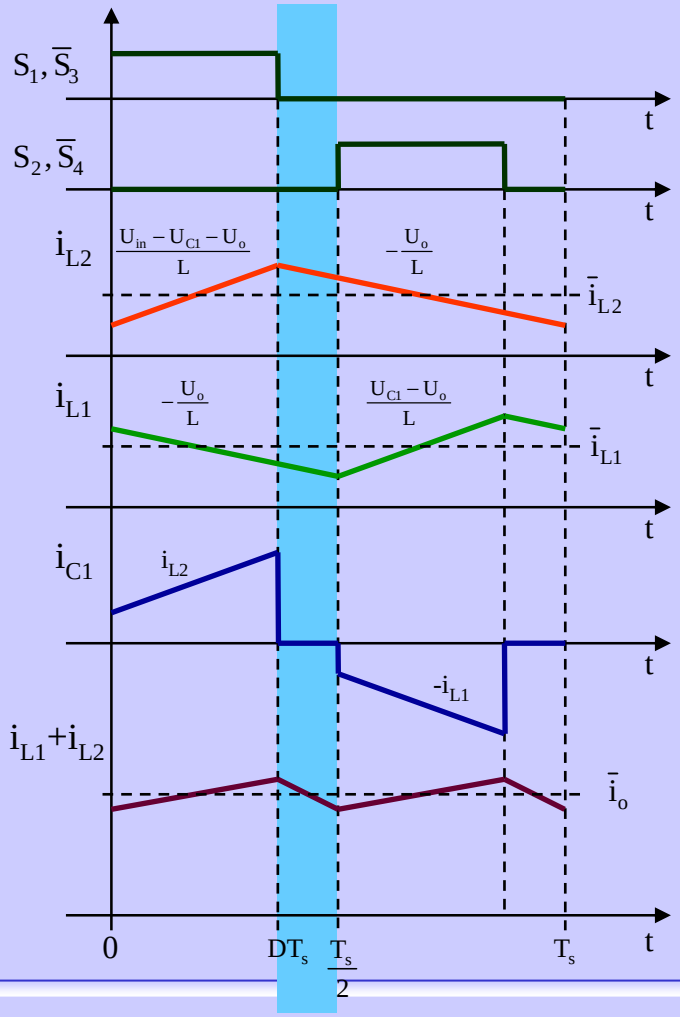


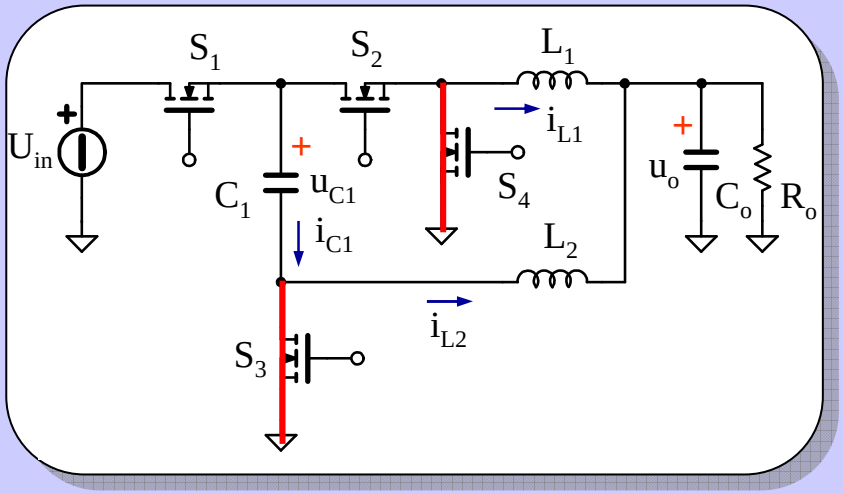
Two-Phase Interleaved Buck with Voltage Divider: D < 0.5



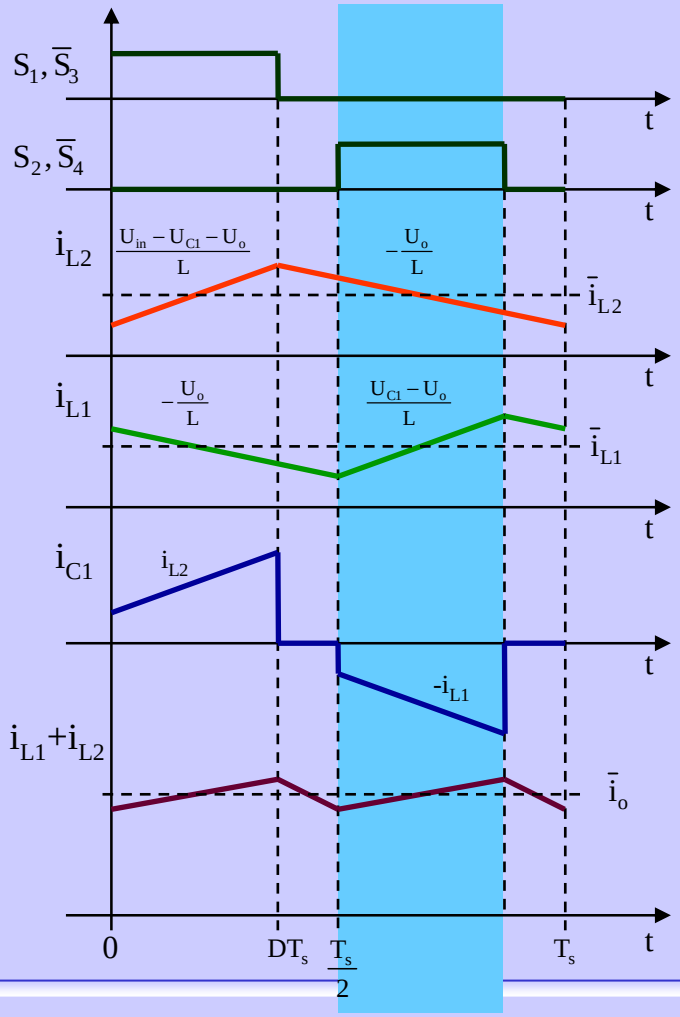


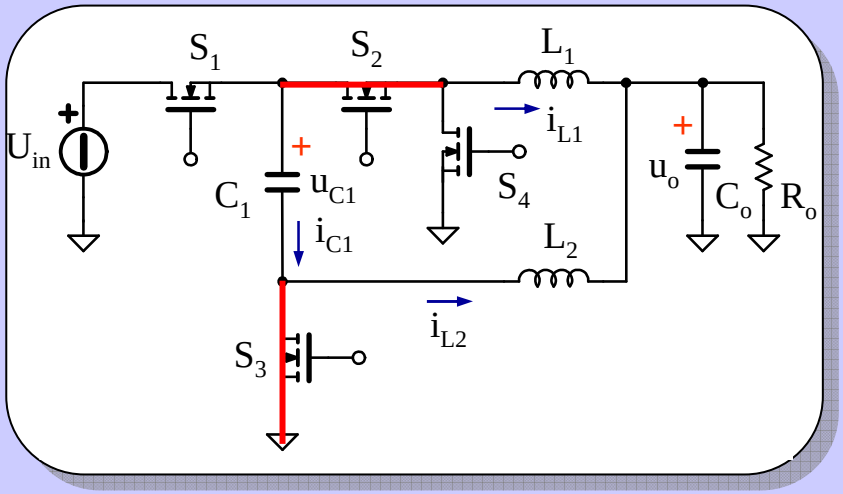
Two-Phase Interleaved Buck with Voltage Divider: D < 0.5



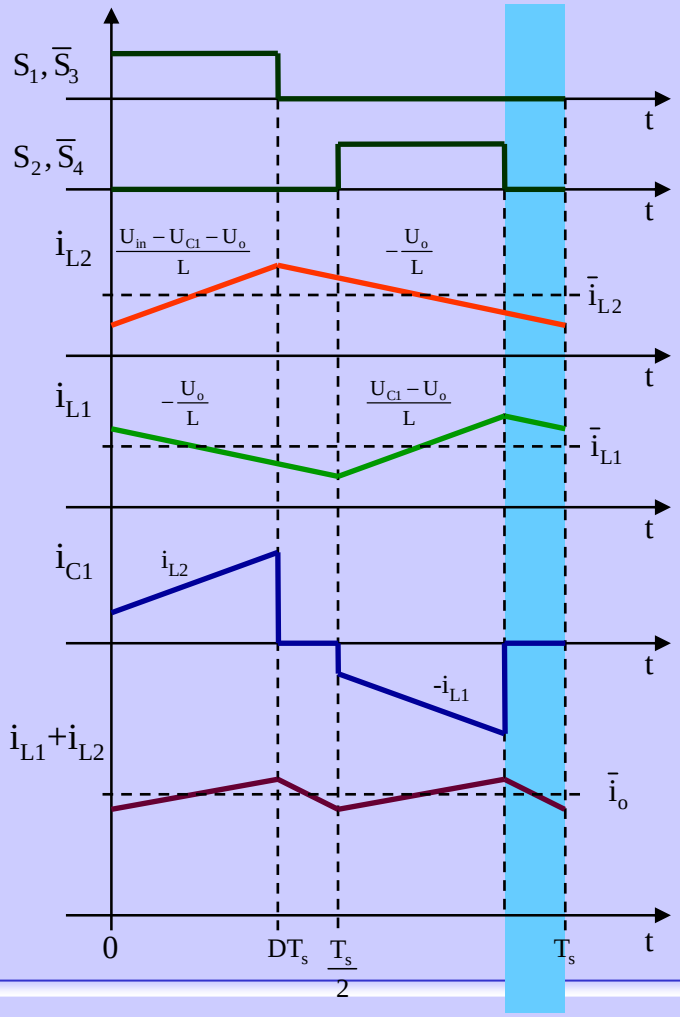


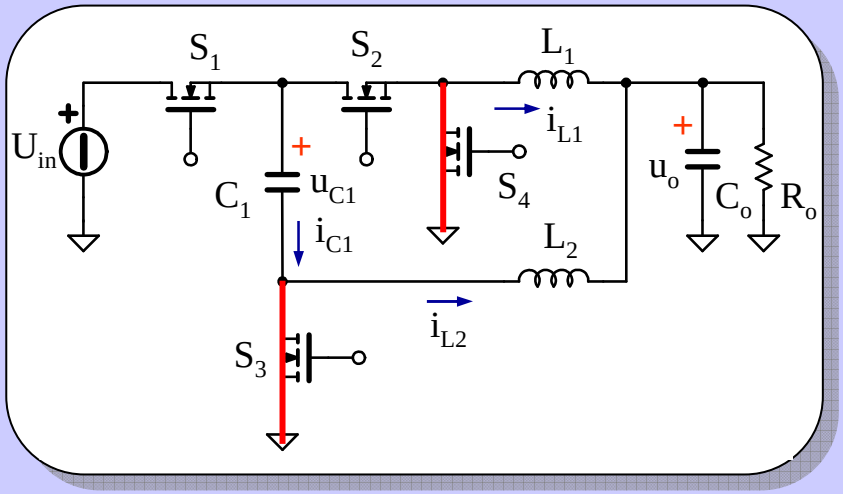
Two-Phase Interleaved Buck with Voltage Divider: D < 0.5





Two-Phase Interleaved Buck with Voltage Divider: D < 0.5





Steady-state analysis (D < 0.5)

- Inductor flux balance:

$$\overline{u}_{L1} = 0 \quad \Rightarrow \quad (U_{C1} - U_o)D - U_o(1-D) = 0 \quad \Rightarrow \quad U_{C1}D = U_o$$

$$\overline{u}_{L2} = 0 \quad \Rightarrow \quad (-U_{C1} + U_{in} - U_o)D - U_o(1-D) = 0 \quad \Rightarrow \quad (U_{in} - U_{C1})D = U_o$$

$$M = \frac{U_o}{U_{in}} = \frac{D}{2} \qquad \frac{U_{C1}}{U_{in}} = \frac{1}{2}$$

- Capacitor charge balance:

$$I_2 D - I_1 D = 0 \quad \Rightarrow \quad I_2 = I_1 \quad \Rightarrow \quad I_2 + I_1 = I_o \quad \Rightarrow \quad I_1 = I_2 = \frac{I_o}{2}$$

Two-Phase Interleaved Buck with Voltage Divider: D < 0.5

- "Natural" current sharing
- Optimal ripple cancellation for overall voltage conversion ratio equal to $\frac{1}{4}$
- Reduced switch voltage stress (one half of input voltage)

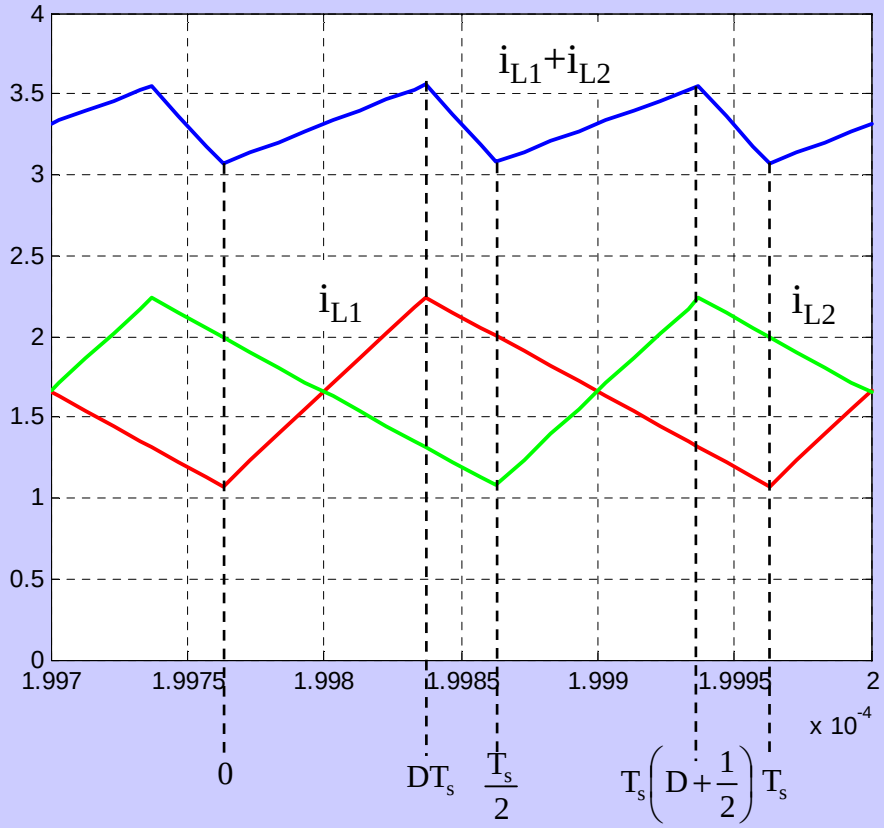
Two-Phase Interleaved Buck with Voltage Divider: D > 0.5

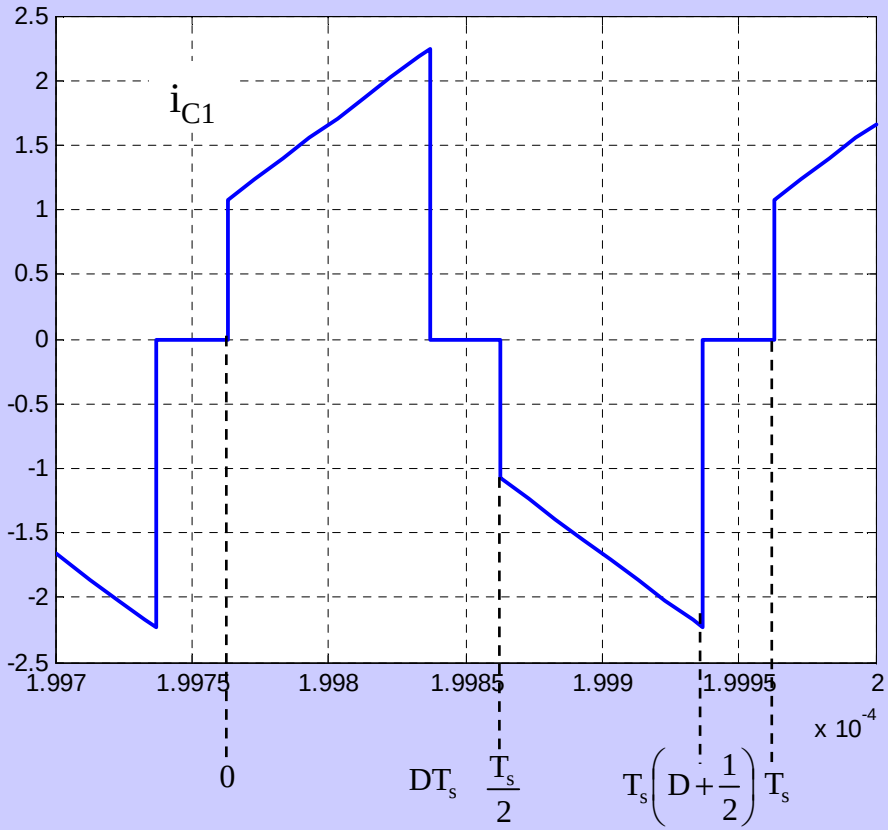
$$M = \frac{U_o}{U_g} = D^2 \qquad \frac{U_{C1}}{U_g} = 1 - D$$

- Unequal average currents in the two phases
- Increased switch voltage stress (equal to the input voltage)

Two-Phase Interleaved Buck with Voltage Divider: D < 0.5

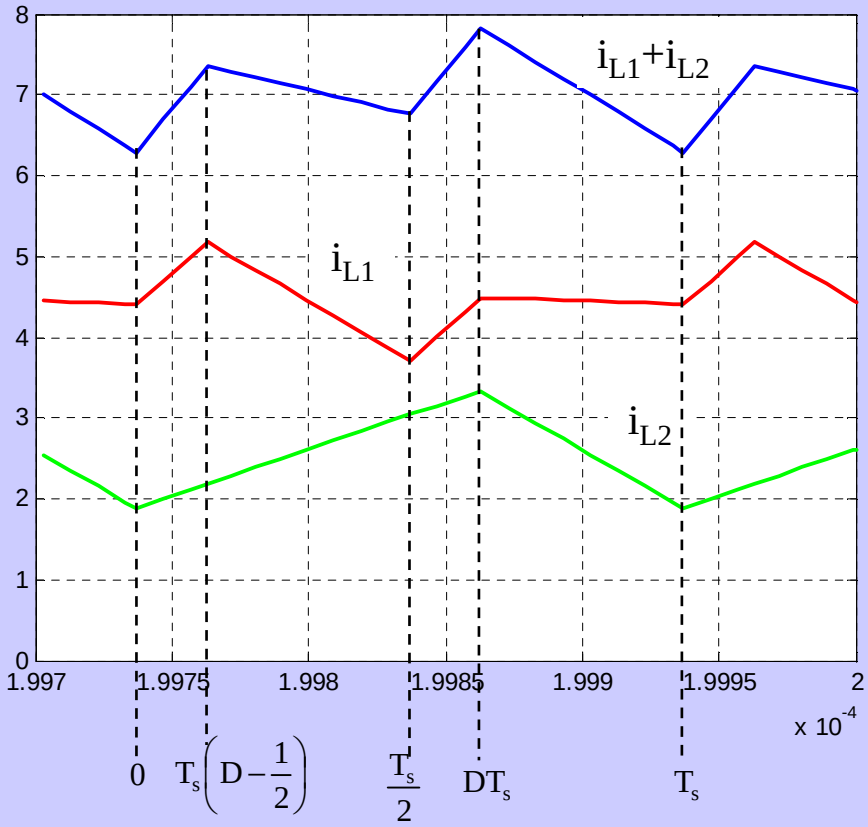
D=0.37

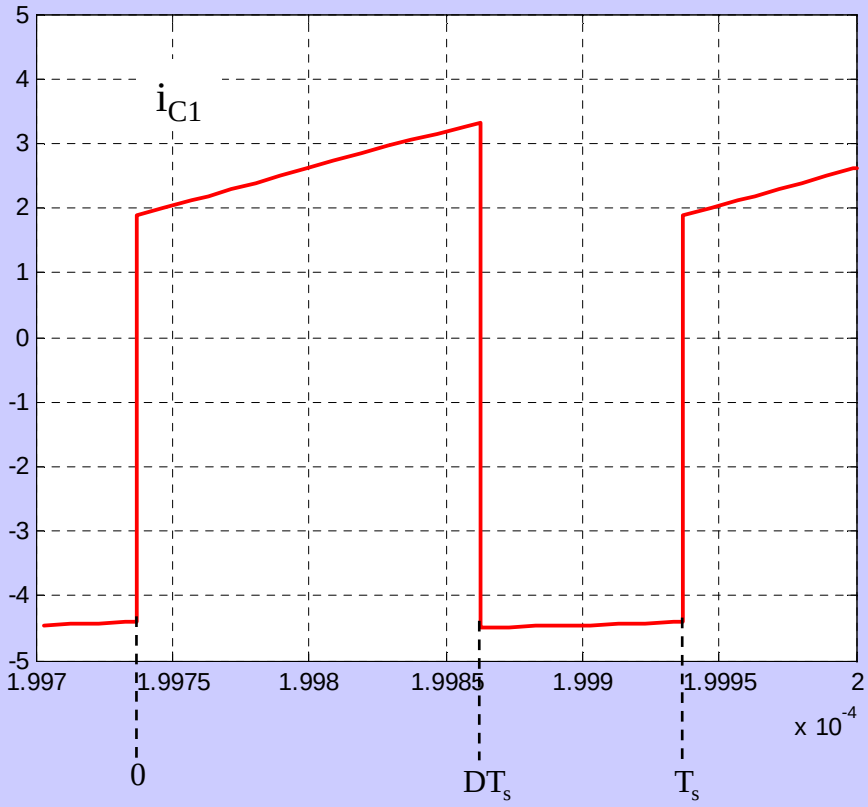




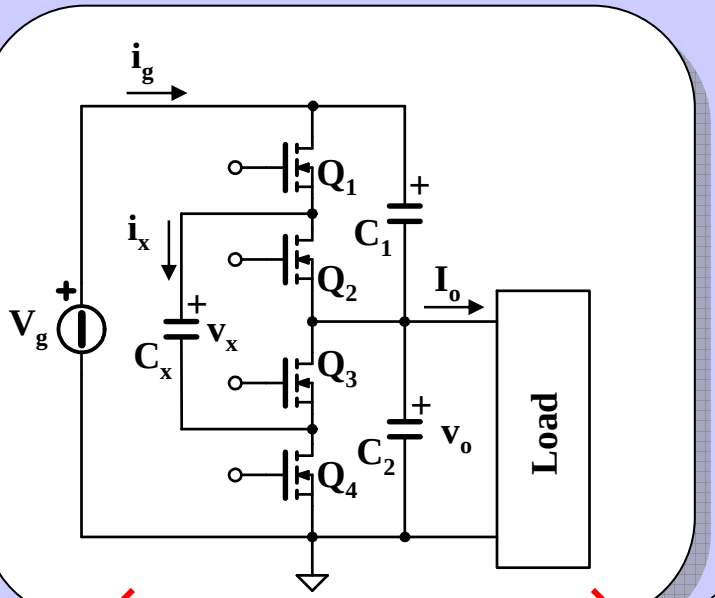
Two-Phase Interleaved Buck with Voltage Divider: D > 0.5

D=0.63

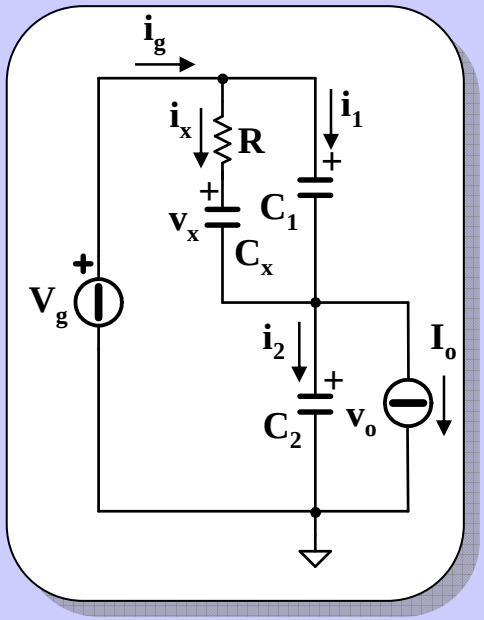




Switched-Capacitor Voltage Divider



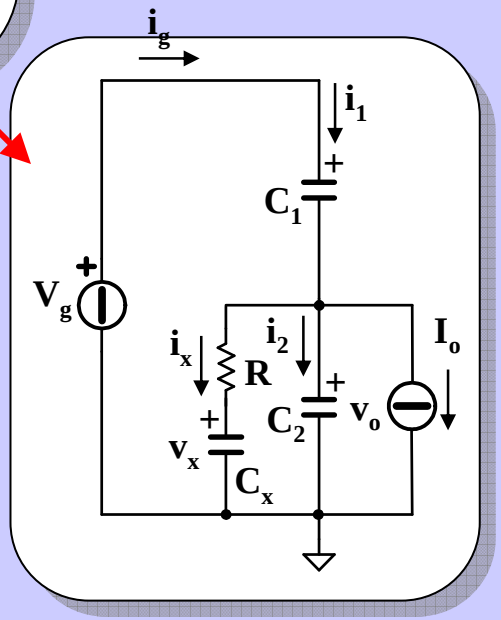
Topology corresponding to Q_1, Q_3 = "on"; Q_2, Q_4 = "off"



$R = 2R_{DSon} + R_{ESRx}$

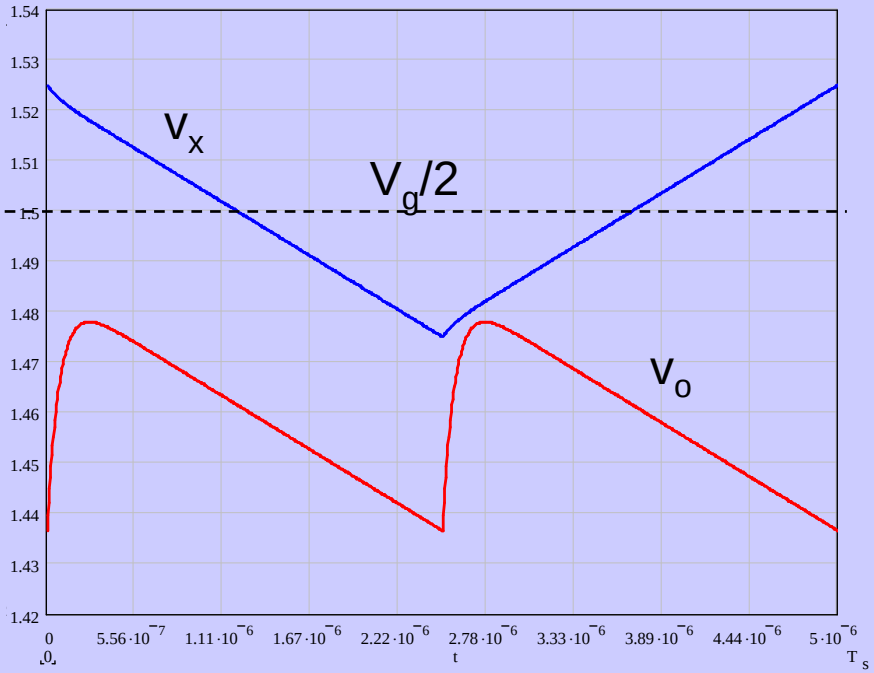
$C_1 = C_2 = C$

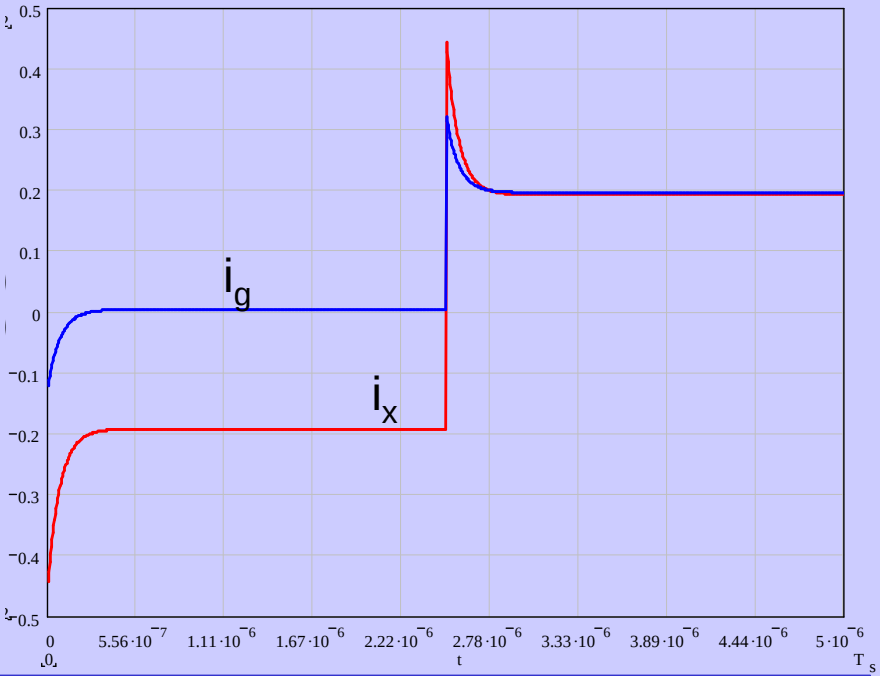
Topology corresponding to Q_2, Q_4 = "on"; Q_1, Q_3 = "off"



SCVD: Steady-State Analysis

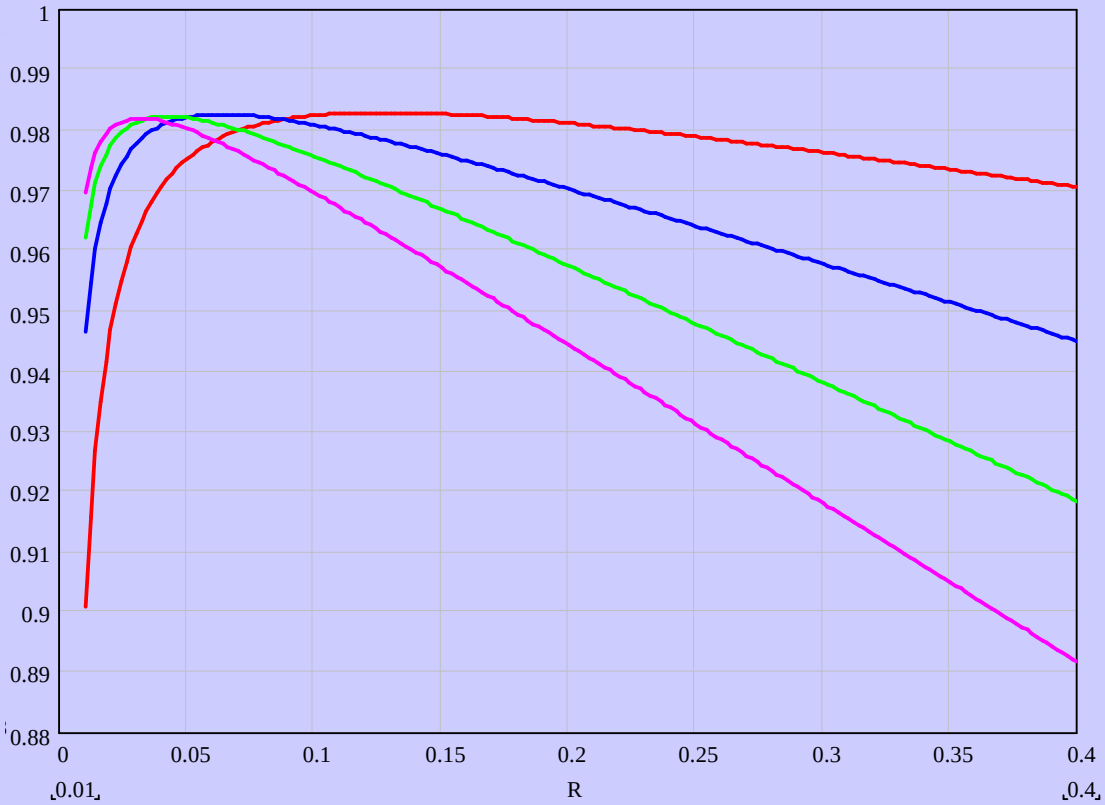
- Input voltage: $V_g = 3V$
- Output current: $I_o = 0.1A$
- Switching frequency: $f_S = 200kHz$
- MOSFET on resistance: $R_{DSon} = 100m\Omega$
- Filter capacitors: $C = 200nF$
- Charge transfer capacitor: $C_x = 10\mu F$





SCVD: Steady-State Analysis

Converter efficiency as a function of output current total parasitic resistance R = 2xR_{DSon} for four different output current values: I_o = 0.1 A (red curve); I_o = 0.2 A (blue curve); I_o = 0.3 A (green curve); I_o = 0.4 A (magenta curve) (C = 200nF, C_x = 10µF)



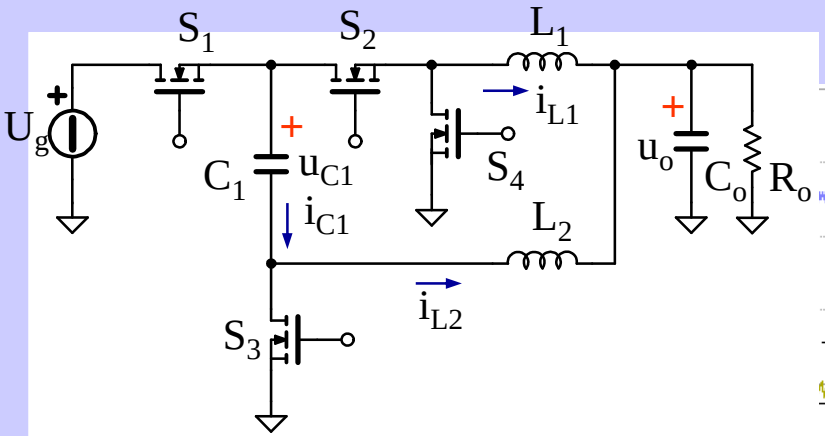
2PIB-VD: Experimental Results at f_s = 1MHz

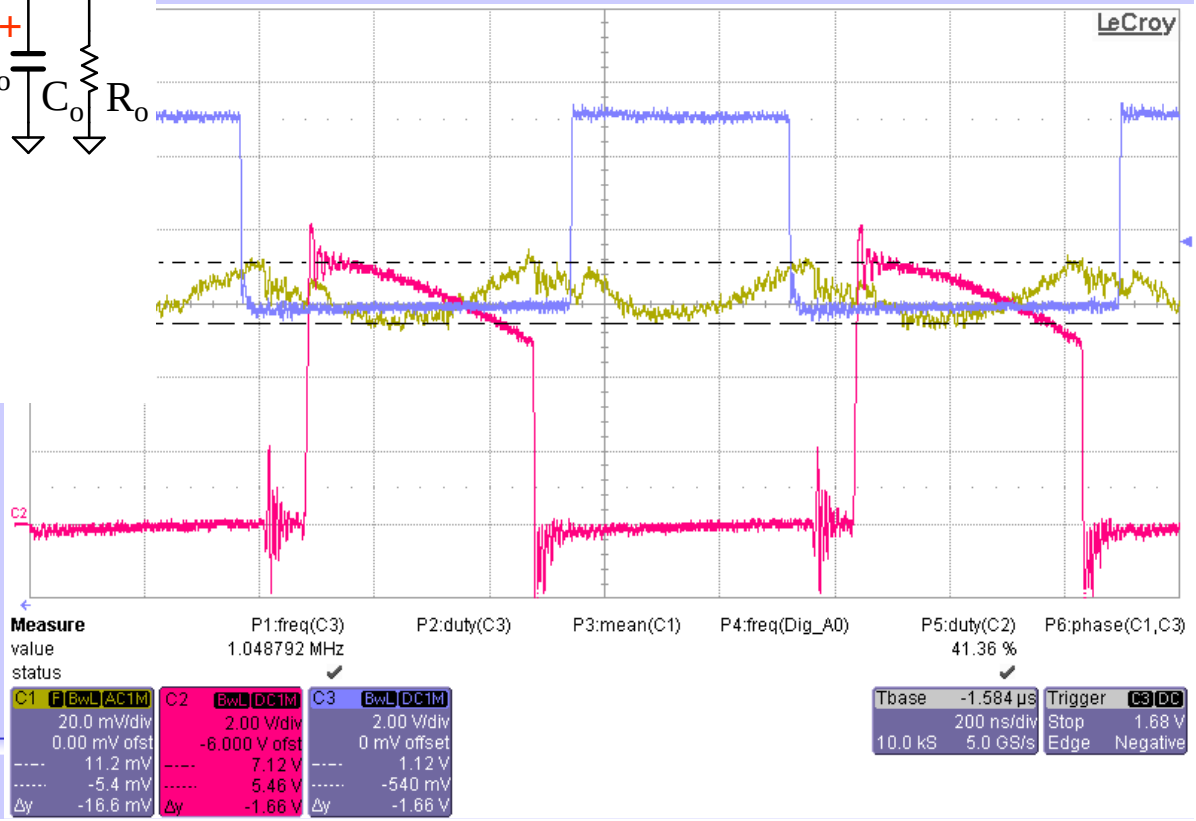
Input voltage: U_g = 12 V
Output voltage: U_o = 2.5 V
Nominal output power: P_o = 7.5W
Nominal output current: I_o = 3A

C_{in} = 100nF + 10µF	C_o = 2x47nF + 4x2.2 µF	C_1 = 2x220nF (1206)
L_1 = 353nH – 90mΩ	L_2 = 342nH – 86mΩ	$S_{1,4}$ = IRF8915

2PIB-VD: Experimental Results at f_s = 1MHz

Converter's main waveforms at nominal power: S_3 logical driving signal (Blue); output voltage ripple (yellow); S_3 Drain-to-Source voltage (red)





Single Buck Converter: Experimental Results at f_s = 1MHz

Input voltage: U_g = 12 V
Output voltage: U_o = 2.5 V
Nominal output power: P_o = 7.5W
Nominal output current: I_o = 3A

C_{in} = 100nF + 10µF	C_o = 2x47nF + 2x47µF + 2x10µF
L = 222nH – 64mΩ (12L Coilcraft)	$Q_{1,2}$ = 2xIRF8915

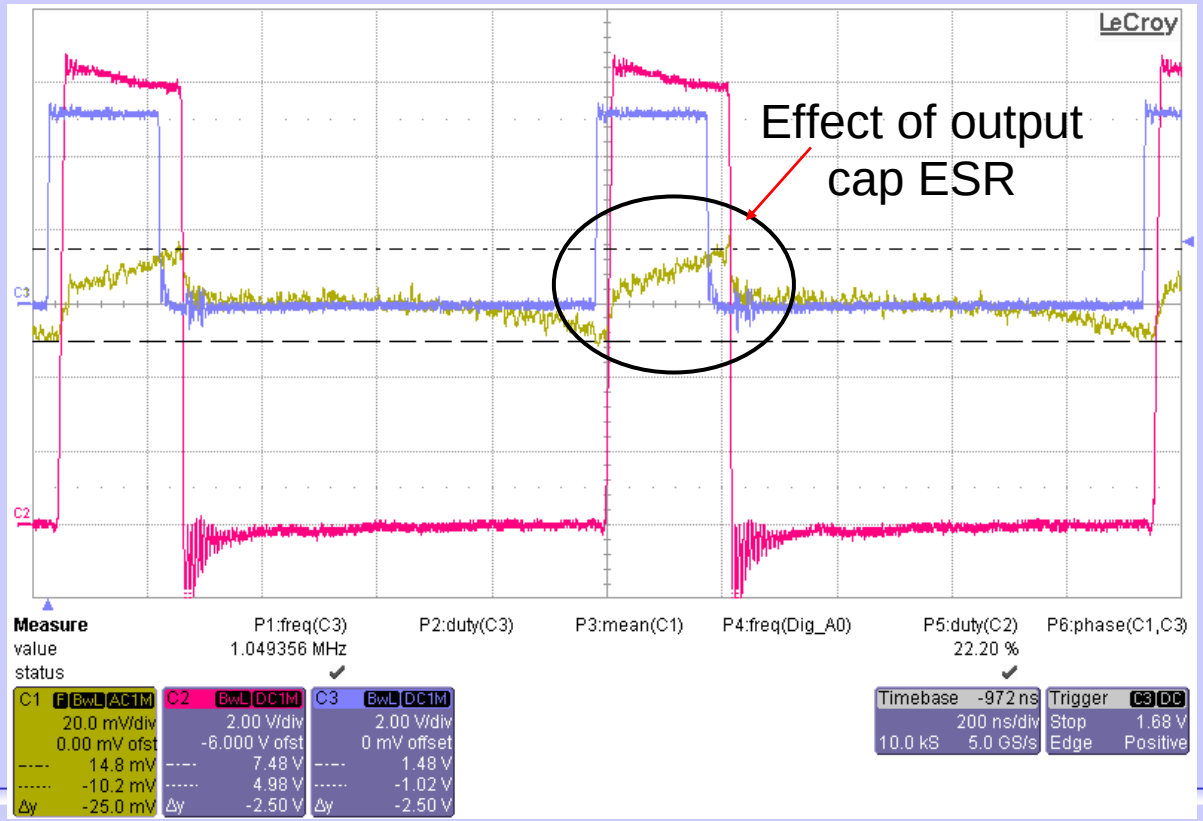
Lower Inductance value

Parallel-connected switches

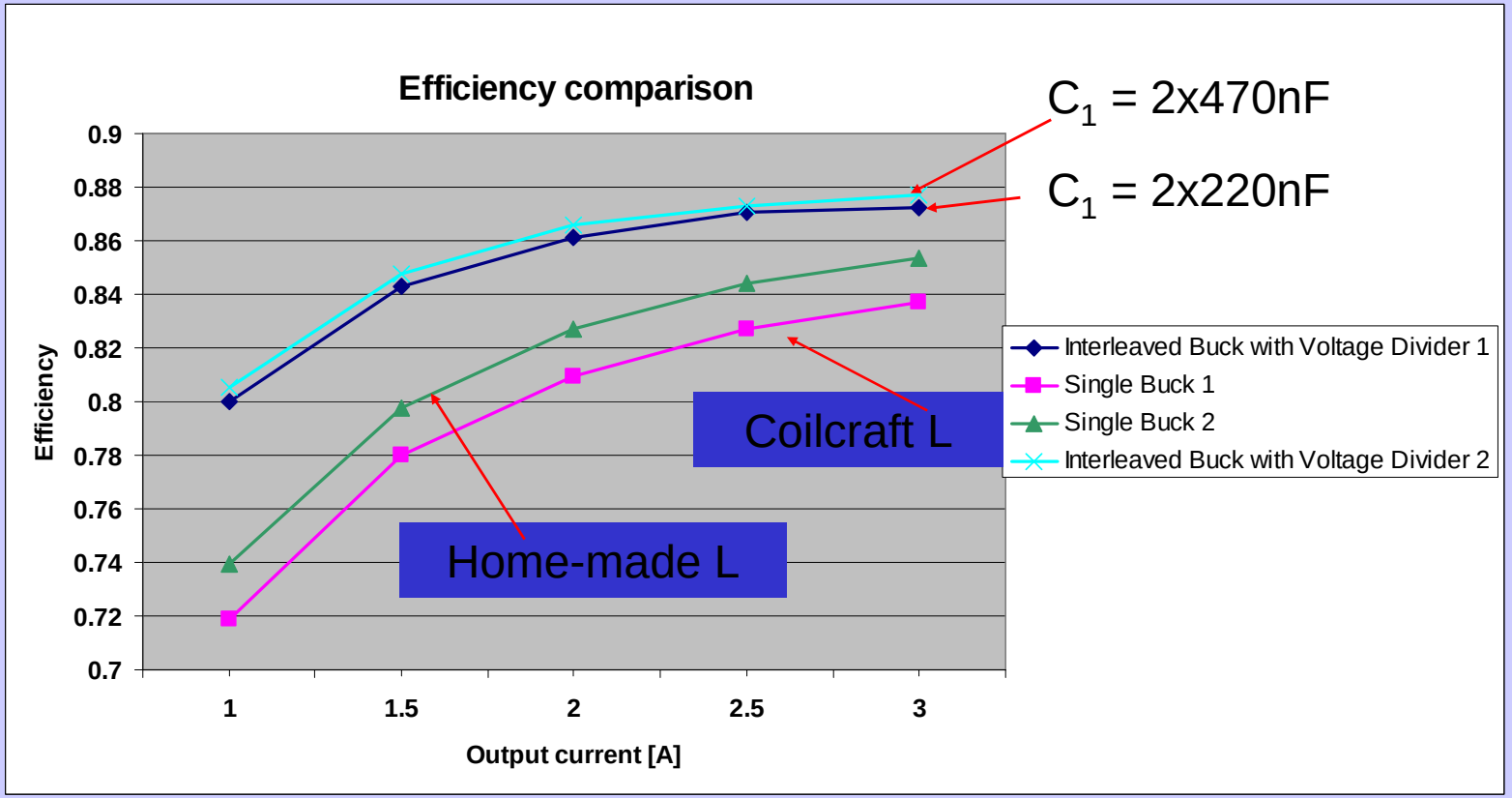
Single Buck Converter: Experimental Results at f_s = 1MHz

Quasi-square wave operation

Converter's main waveforms at nominal power: S_1 logical driving signal (Blue); output voltage ripple (yellow); S_3 Drain-to-Source voltage (red)



Efficiency Comparison at f_s = 1MHz



Home-made L: 0.84mm wire diameter (L = 220nH, 50mΩ) wound on a plastic support (ϕ = 4.38mm)

Experimental Results at f_s = 2MHz

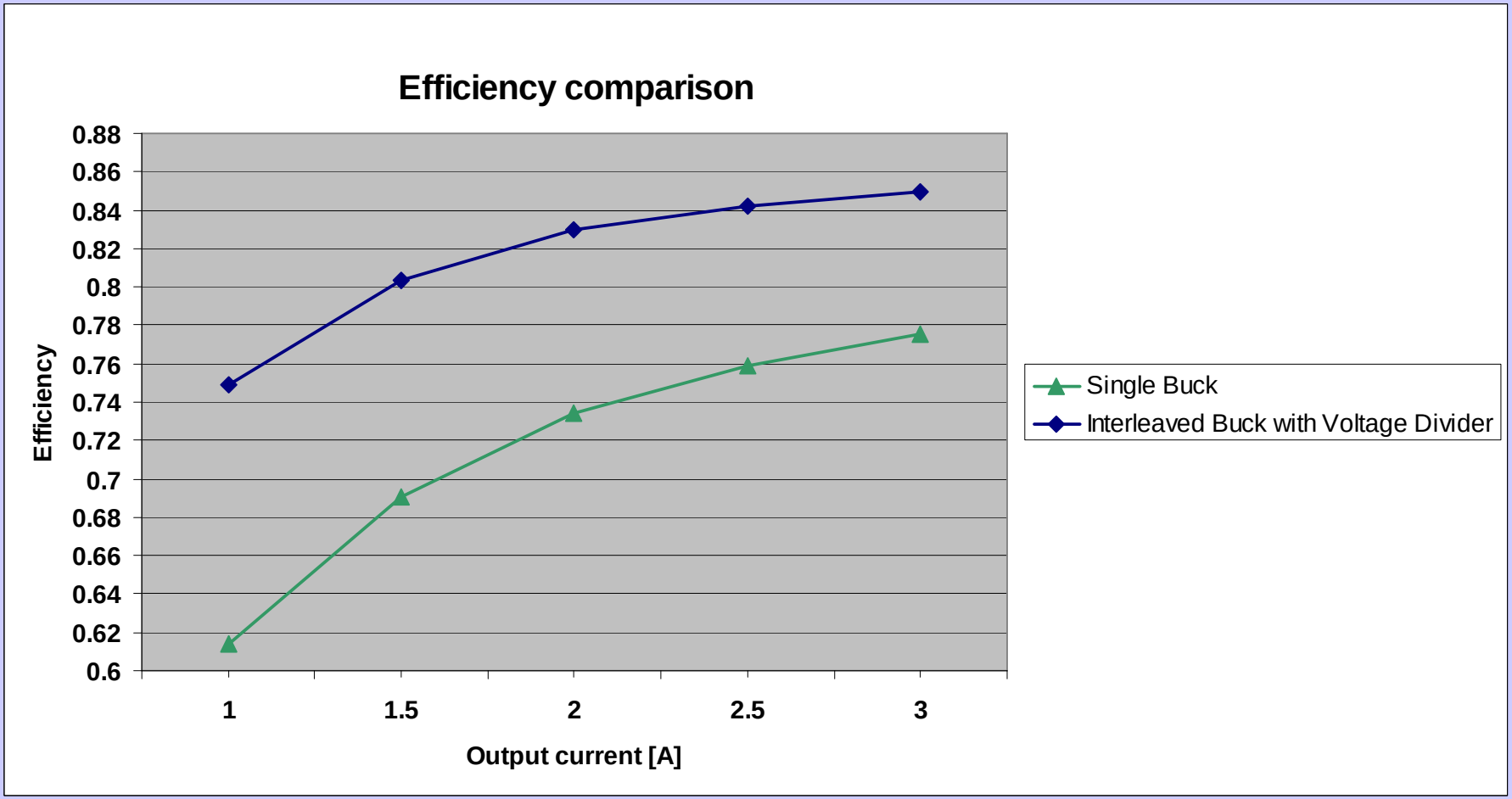
2PIB-VD

C_{in} = 100nF + 10µF	C_o = 2x47nF + 4x2.2 µF	C_1 = 2x470nF (1206)
L_1 = 161nH – 58mΩ	L_2 = 169nH – 63mΩ	$S_{1,4}$ = IRF8915

Single buck

C_{in} = 100nF + 10µF	C_o = 2x47nF + 2x47µF + 2x10µF
L = 90nH – 30mΩ	$Q_{1,2}$ = 2xIRF8915

Efficiency Comparison @ f_s = 2MHz



Conclusions

Summary

- The present power supply architecture at LHC will no longer be sustainable in the future upgrades
- Distributed power supply architectures based on DC-DC converters are proposed
- High step-down ratio topologies are the key for increasing power distribution with the same cabling
- High conversion efficiency as well as low switching noise are mandatory

Future investigations

- Radiation tolerance components and technologies must be selected
- More intensive investigations on switching noise effects must be carried out