Monolithic pixels for Innovative Silicon Trackers

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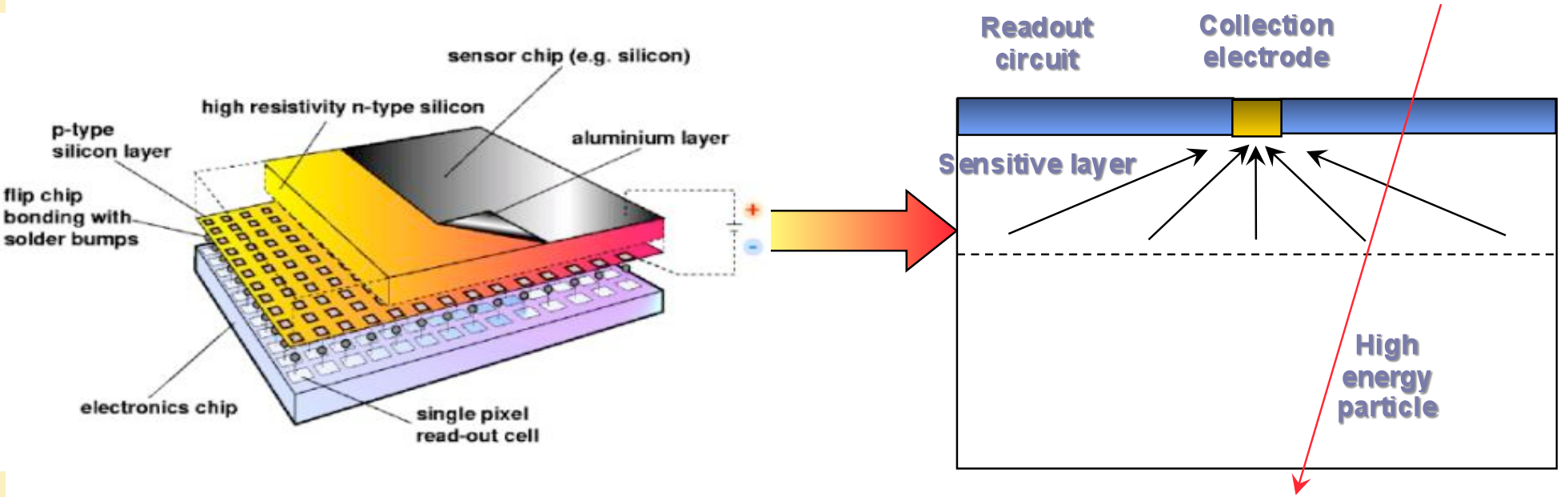
MONOLITHIC DETECTORS : definition

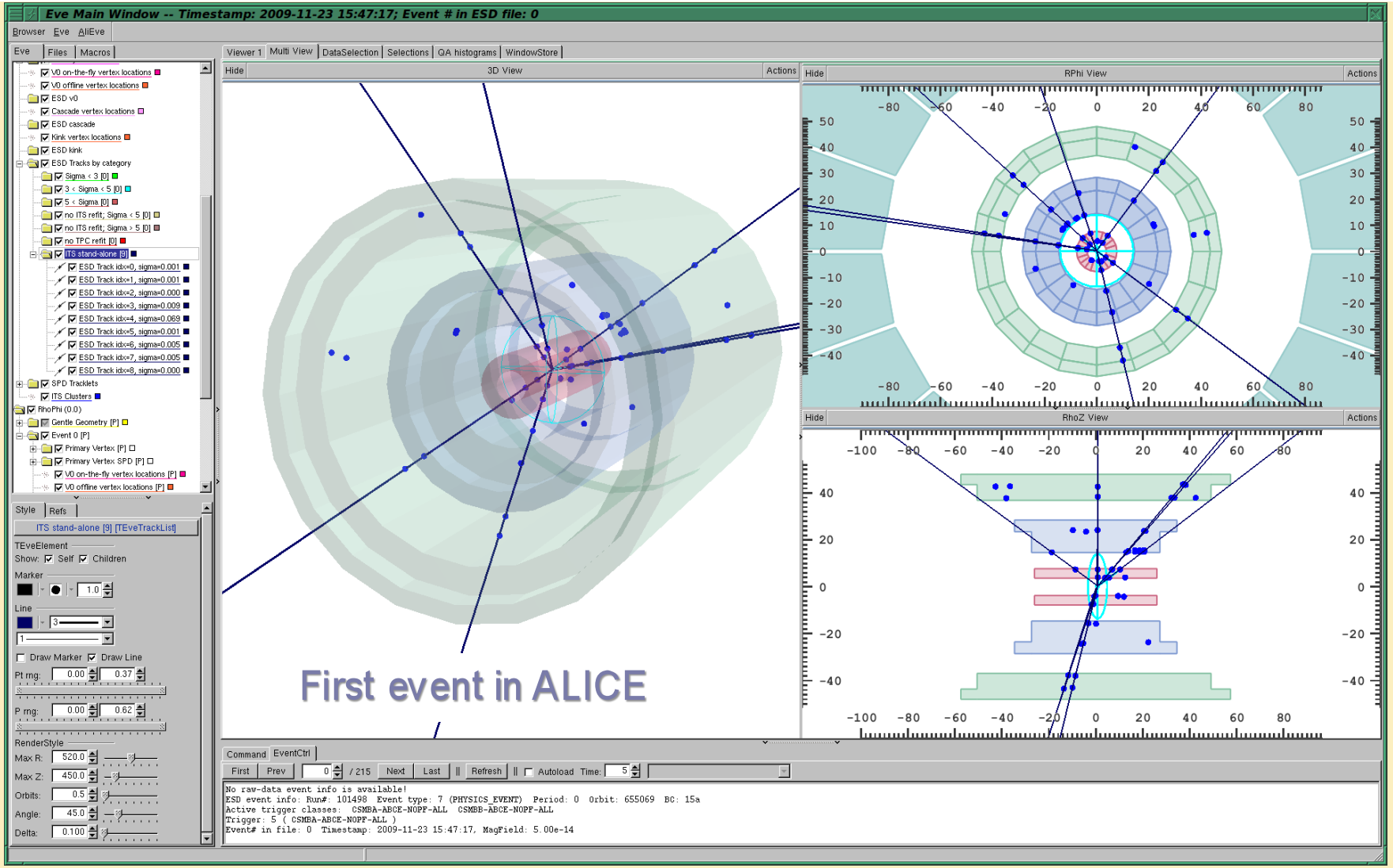


Integrate the readout circuitry – or at least the front end – together with the detector in one piece of silicon

The charge generated by ionizing particle is collected on a designated collection electrode

- Motivation :
  - Impact of power consumption on material in high energy physics experiments
  - The importance of Q/C for power consumption
- Some examples of monolithic detectors
- Device design & device simulations
- Processing
- Monolithic detectors in deep submicron CMOS : example LePIX
  - Q/C and segmentation
  - Device design
  - Some (analog front end) readout circuits
  - Status of first prototype submission & measurement setup
- Digital part of the readout and power consumption
- Radiation tolerance

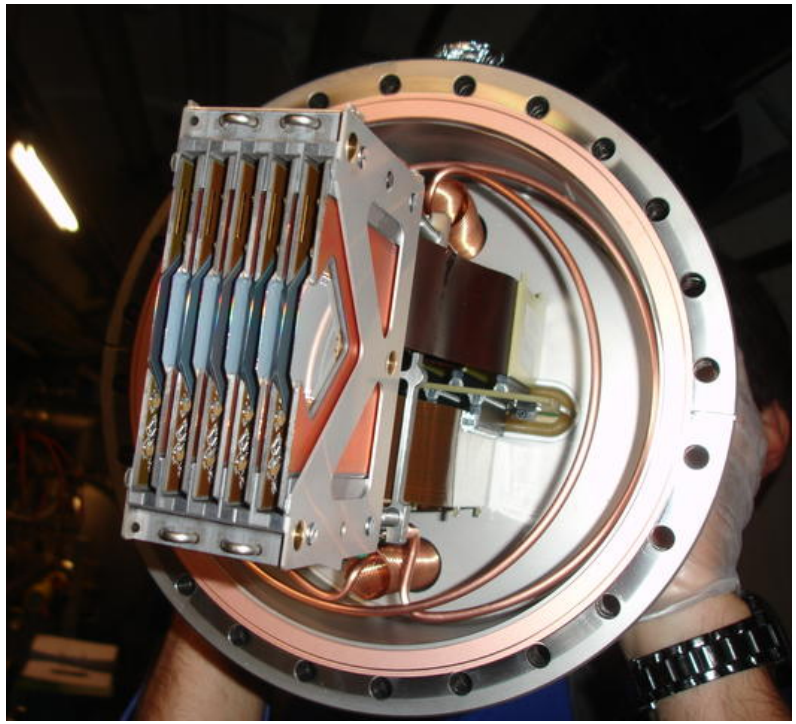
NOW THAT LHC HAS STARTED PRODUCING COLLISIONS !



THINKING ABOUT TRACKER UPGRADES…

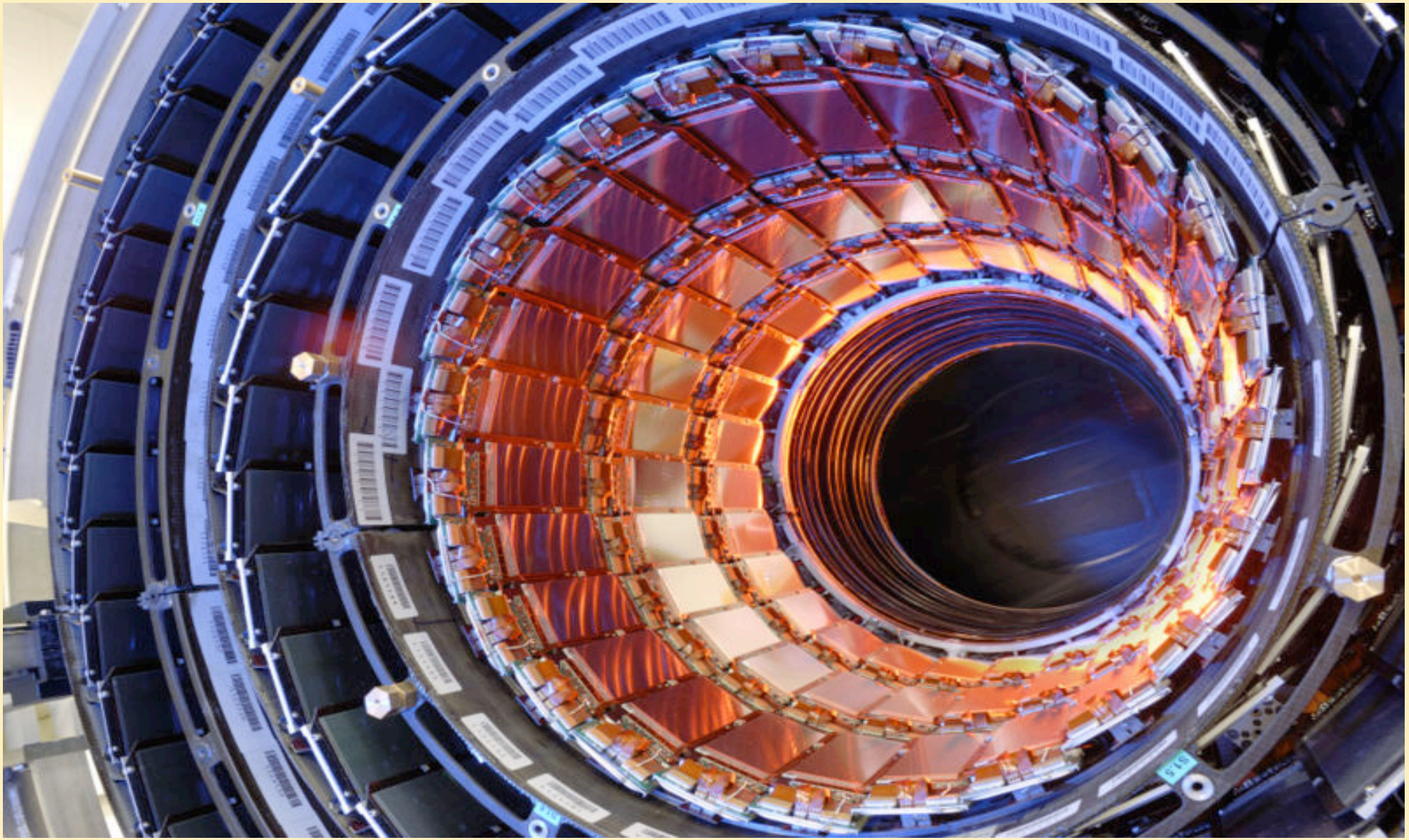
Services: cables, power supplies, cooling, etc…

- Represent a lot of work and a considerable fraction of the total budget
- Subject to severe spatial constraints, limiting for future upgrades
- Power often consumed at CMOS voltages, so kW means kA

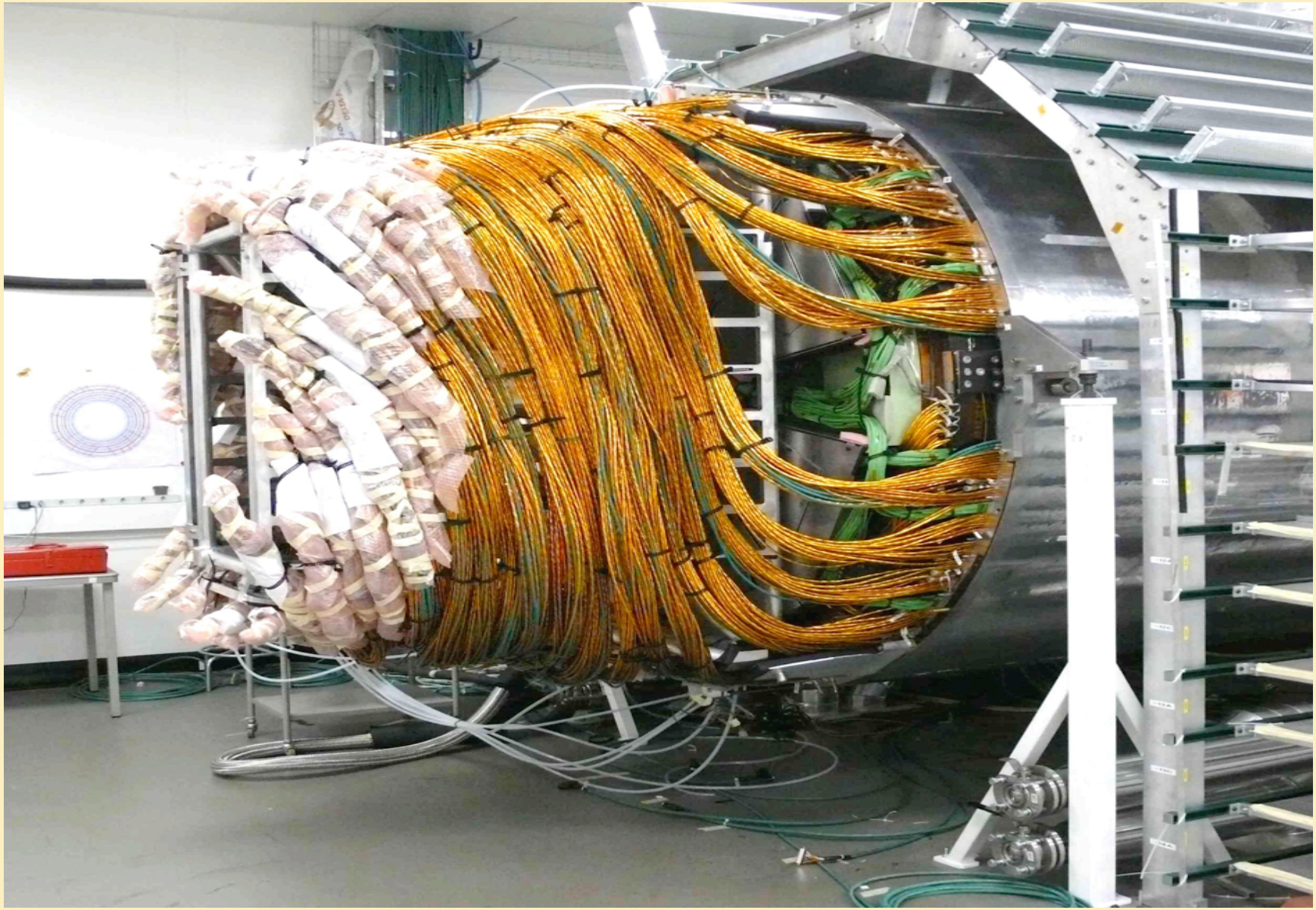


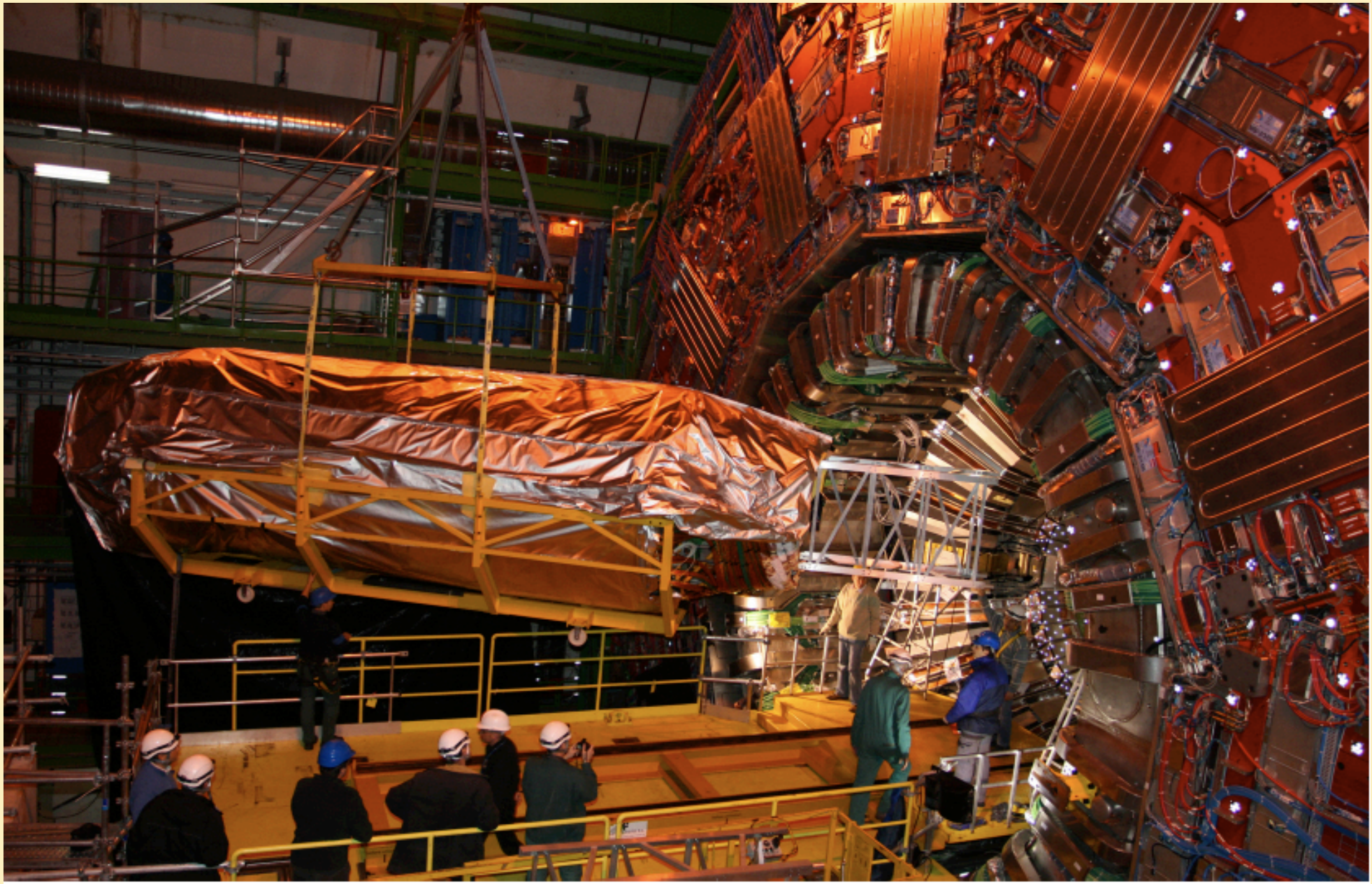
- Even if power for detector is low, voltage drop in the cables has to be minimized: example analog supply one TOTEM Roman Pot:
  - ~ 6A @ 2.5 V
  - ~100m 2x16mm^2 cable: 0.1 ohm or 0.6 V drop one way
  - 8230kg*2*100*16E-6=26kg of Copper for ~ 15 W

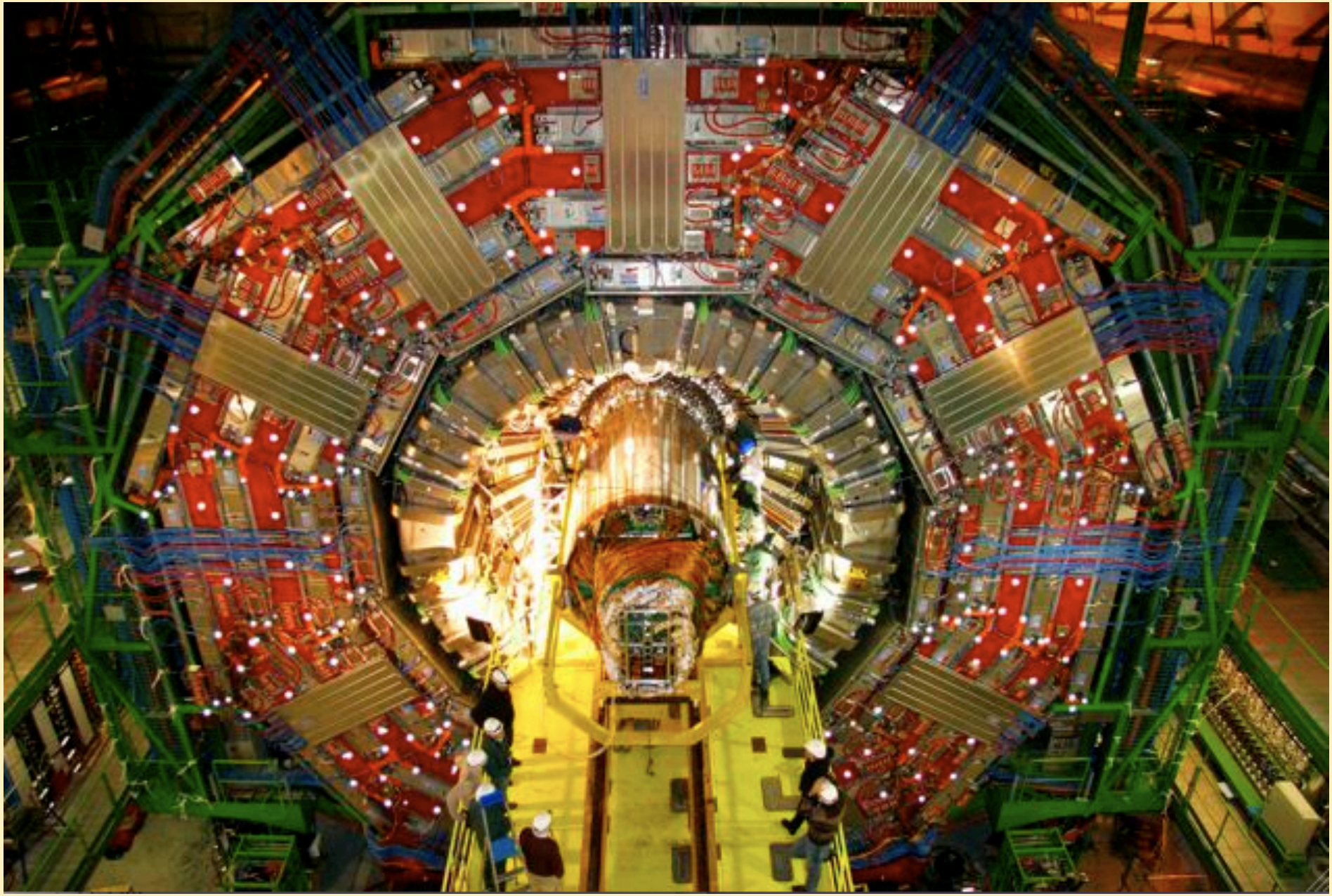
The CMS Tracker before dressing …



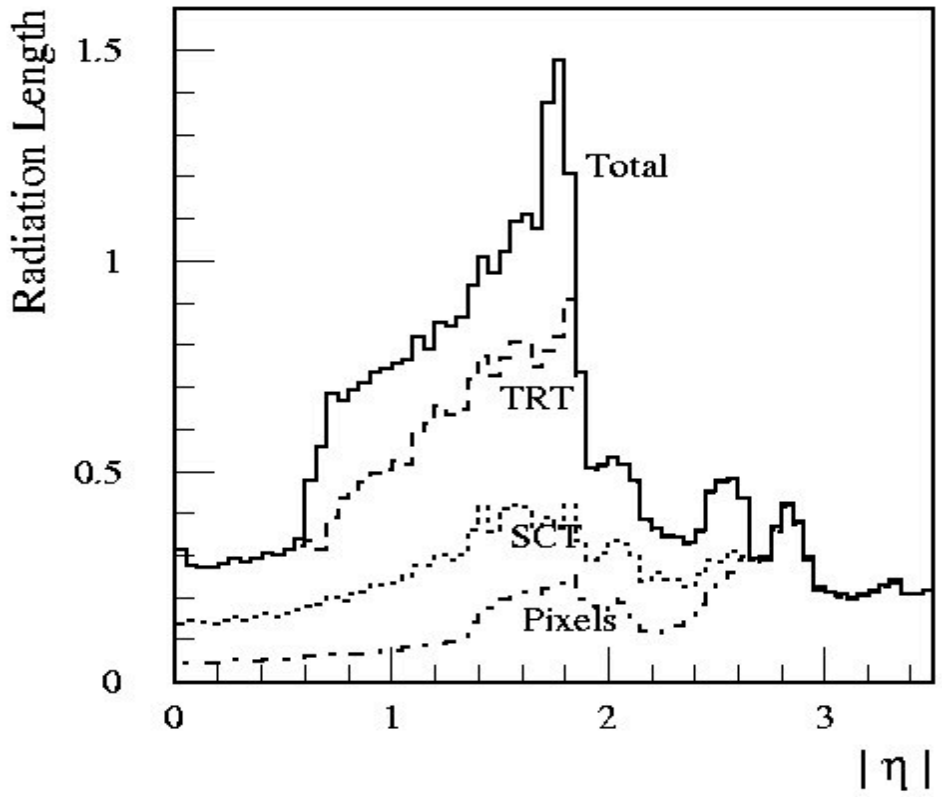
… and after



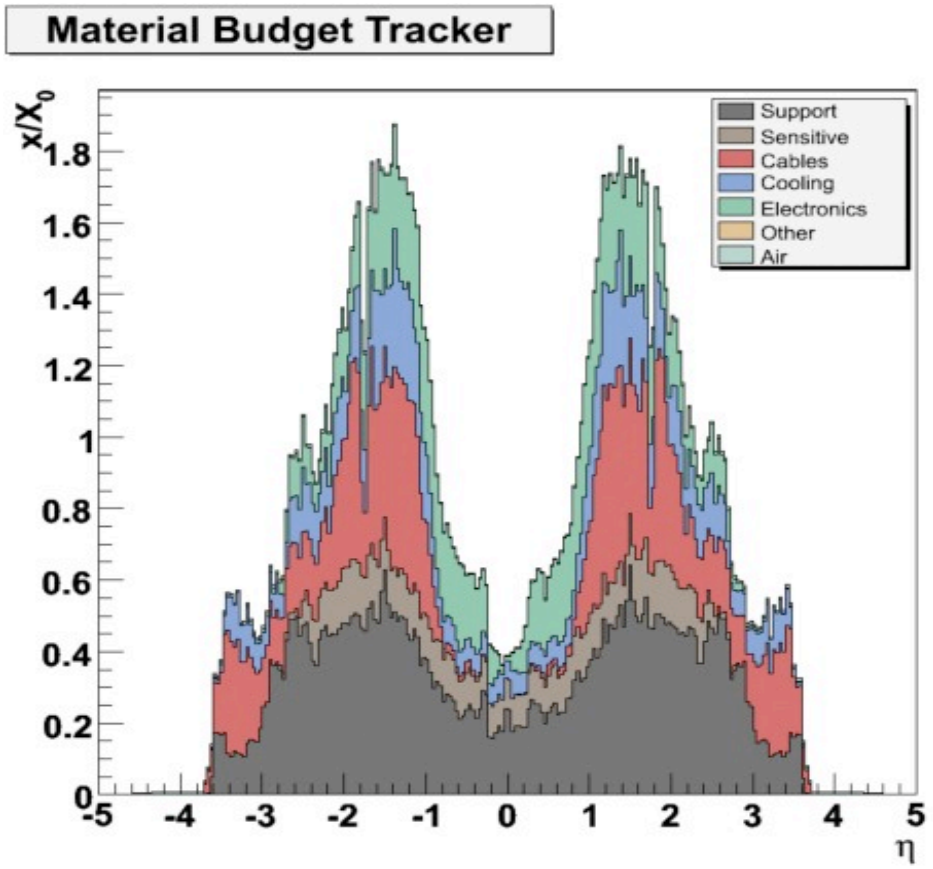




Power and material budget



Atlas tracker material budget

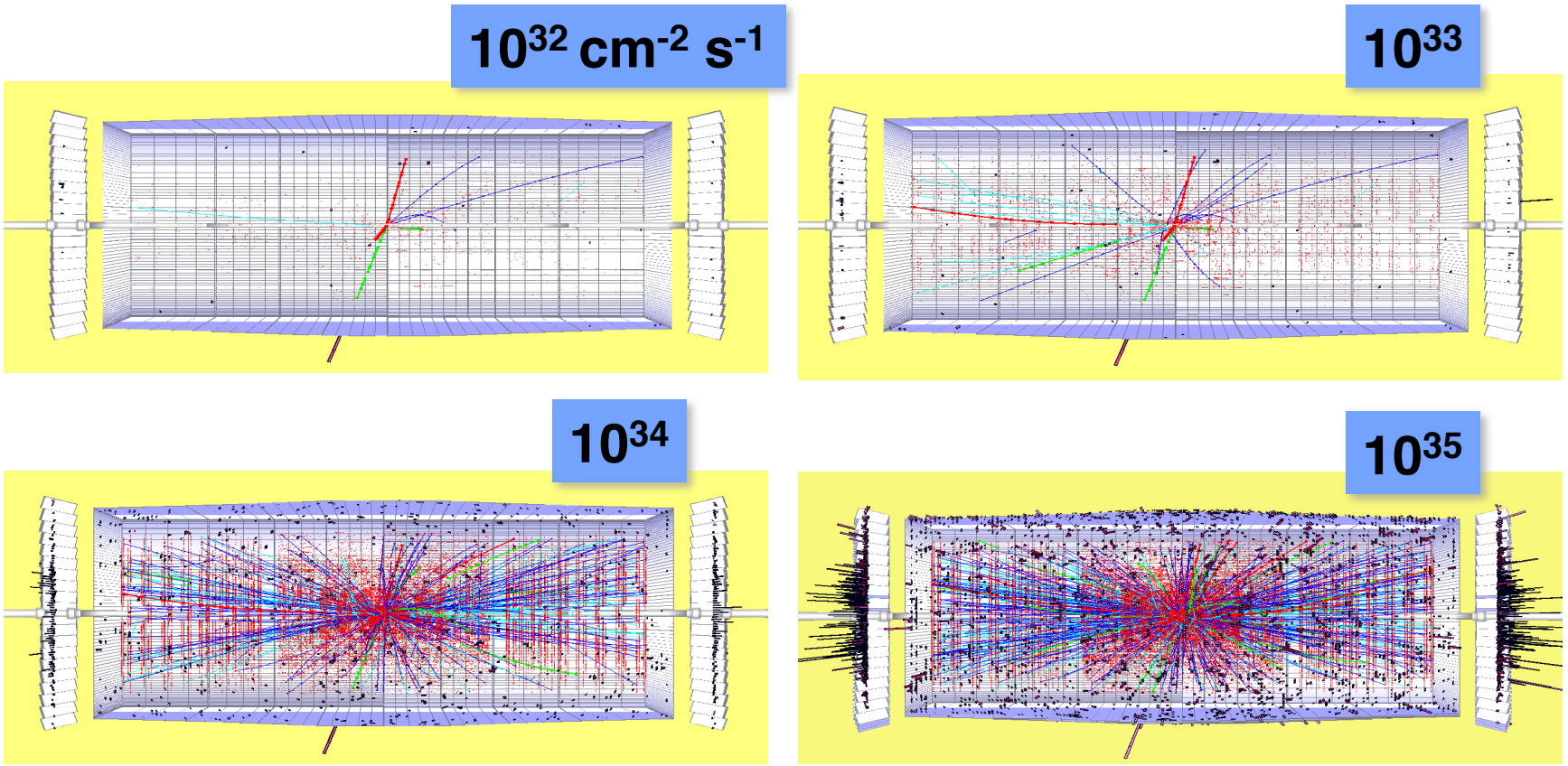


CMS tracker material budget

Power in CMS Tracker

- Total # channels: 75,500 FE chips x 128 = ~10M
- Power/FE: ~ 2.9 mW/channel
- Pwr/ch data TX: ~0.6 mW/channel
- Supply all included: 2.5 V and 1.25
  P_{tot}= ~33 kW
- PSUs on balconies
- # of service cables: 1,800
- Power in the cables: ~62 kW, as 4 Volts dropped on cables!
- Services of PSUs: + 12 kW
- Pixel total is 25 kW extra

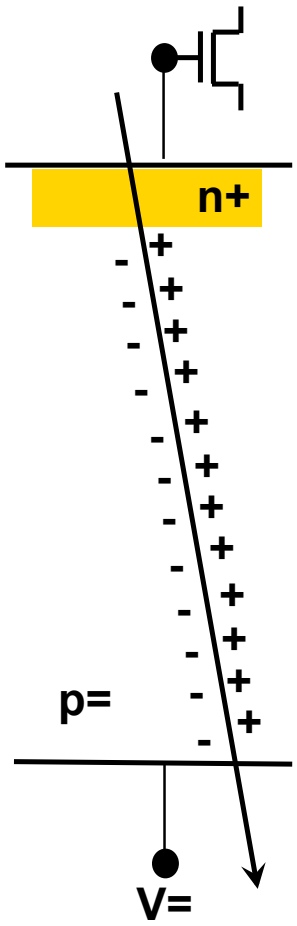
CMS from LHC to SLHC



Thinking about upgrades

- Power has severely impacted amount of material through cables (feeding current in and out) and cooling.
- Different approaches possible to reduce material:
  - Reduce severely power per channel -> monolithic detector, topic for today
  - Reduce material per detector layer -> monolithic detector, topic for today
  - Use part of mechanical structure to bring in power
  - Special powering schemes : DC-DC converter, serial powering
- Physicists are discussing:
  - 10x in luminosity (so 10 times more collisions)
  - triggering from the tracker (fast information to select useful data) using coincidences between layers
- So more functionality without power increase…

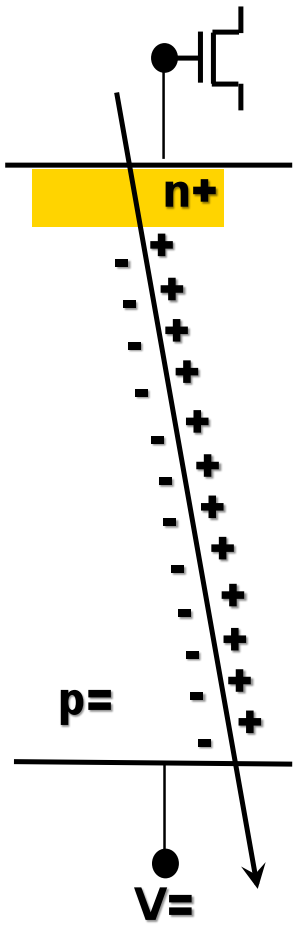
SIGNAL FORMATION



- Minimum Ionizing Particle (MIP) creates ~80 e/h pairs per micron of silicon traversed
- In a detector (for instance PIN diode):
  - bias applied to separate positive and negative charge
  - collect charge onto collection electrode
- Charge read out from collection electrode by circuit
- Signal charge ~ collection depth
- Voltage developed on collection electrode ~ 1/C
- In current generation typical detector thickness 300 microns for a charge of about 24 000 electrons (4 fC)

$$\text{Signal-to-Noise} \sim \frac{Q}{C} \sim \frac{\text{Charge collection depth}}{\text{Collection electrode capacitance}}$$

MOTIVATION FOR MONOLITHIC DETECTORS



- Detector-readout connection automatically realized
- Cost
  - one chip instead of two or readout immediately included
  - some monolithic detectors offer lower cost per unit area than traditional high resistivity silicon detectors alone
- Less material
- Low capacitance of the collection electrode allows very favorable power – signal-to-noise ratios

$$\text{Signal-to-Noise} \sim \frac{Q}{C} \sim \frac{\text{Charge collection depth}}{\text{Collection electrode capacitance}}$$

- Motivation :
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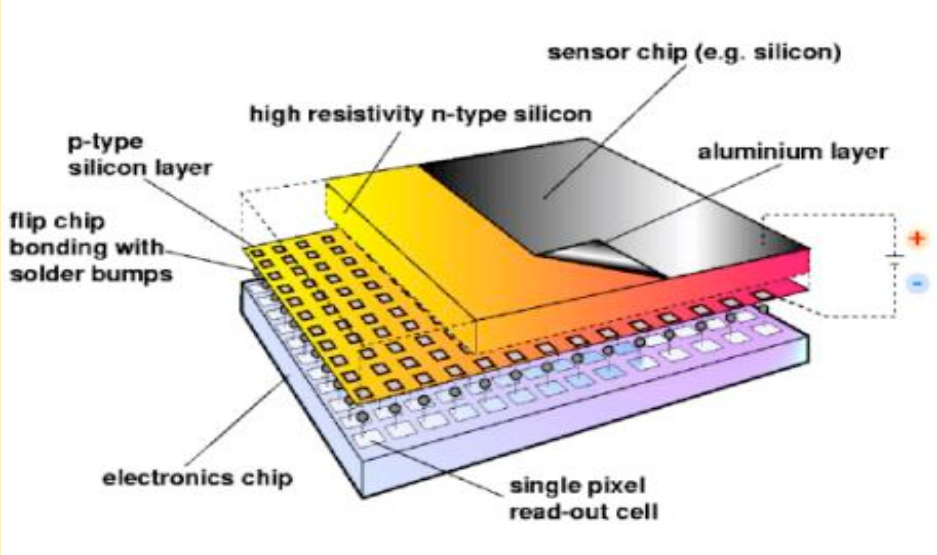
SOME HIGH RESOLUTION HYBRID TRACKING DETECTORS

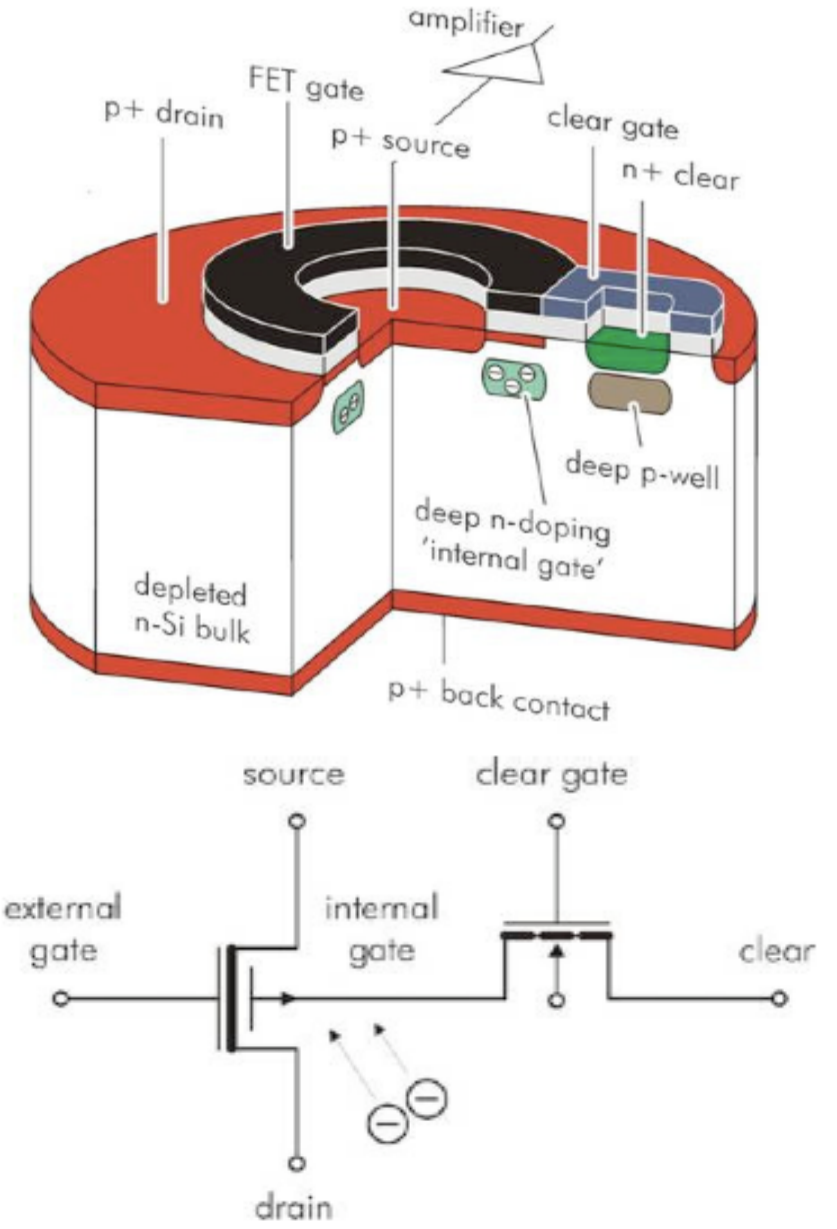


Hybrid pixels

- Detectors and electronics fabricated on different substrates.
- Charge collection by drift, good radiation hardness.
- Pixel size 50 x 50...400 microns
- Complex front-end electronics high readout speed.
- Typical power density : 250 mW/cm^2

Silicon strips

- Detector and front end electronics on different substrates.
- Suitable for covering large areas at low particle densities
- Power density 20 mW/cm^2

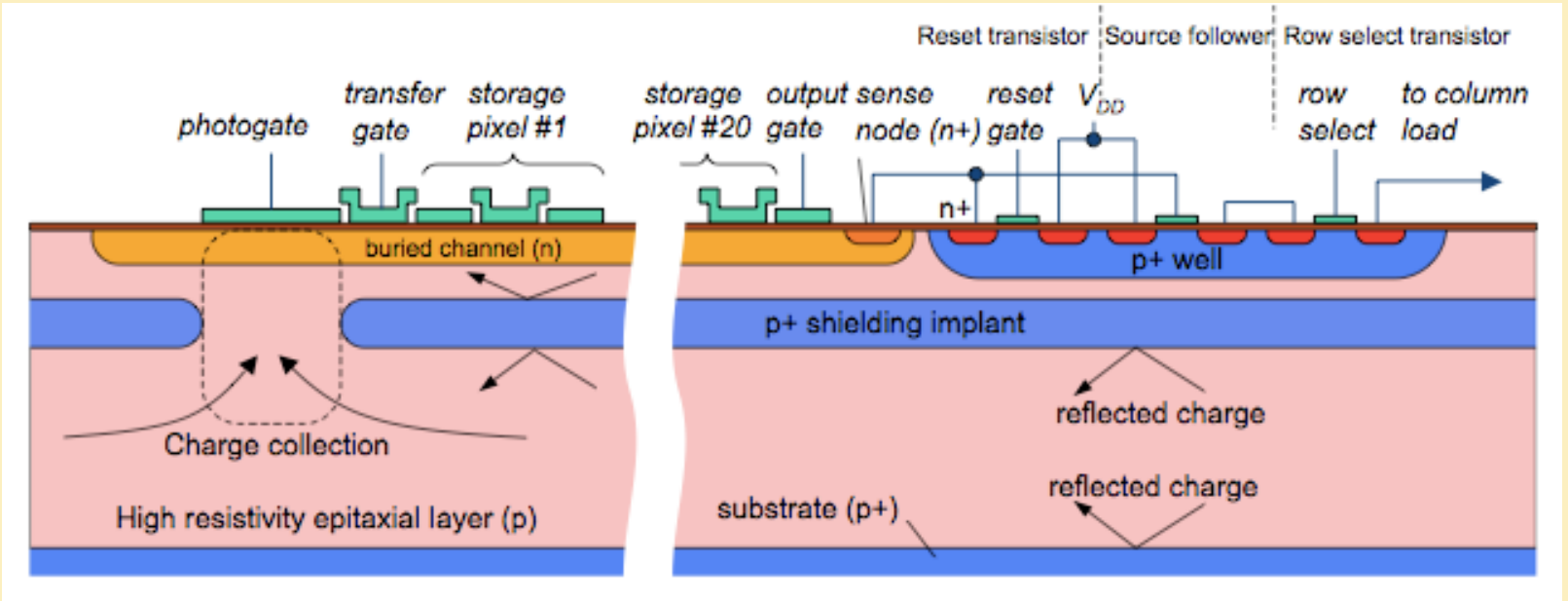


DEPFET (MPI MUNICH)

Principle of operation:

- An annular PFET is created on top of a fully depleted substrate (back side junction).
- A potential well is created under the gate area collecting the charge generated in the substrate.
- The potential of this potential well changes with collected charge and modulates the source-drain current of the DEPFET
- Charge collection continues even if DEPFET is switched off.
- Clear gate allows reset of the potential well.
- The readout can occur via the source (voltage out), or via the drain (current out)
- Very small collection electrode capacitance, allows high S/N operation.
- Need steering and rest of readout off chip or on another chip.

CHARGE COUPLED DEVICES (CCD)

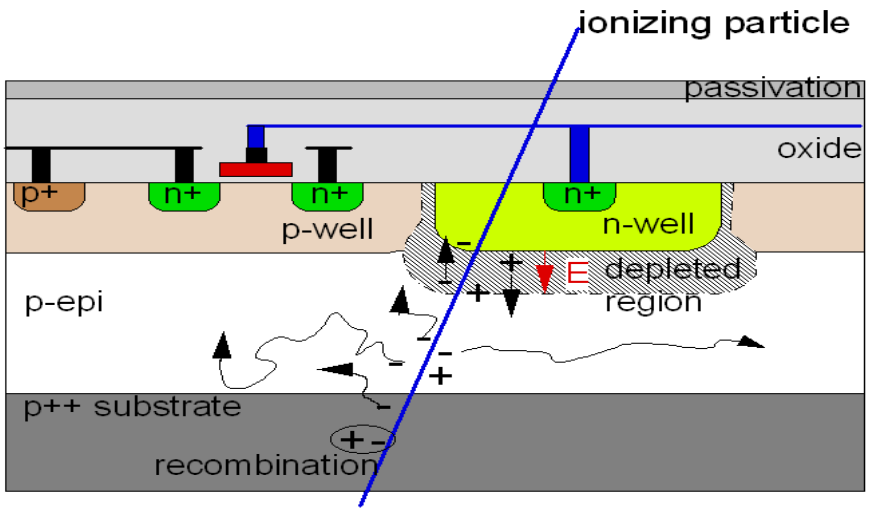


Principle of operation:

- Signal charge is collected in potential well under a gate and then transferred from one location to the next => serial readout needing very large drive currents (20nF at 50MHz = Amps !)
- To increase speed ColumnParallelCCD (CPCCD) Readout per column in parallel
- Interesting development (figure above LCFI collaboration): In Situ Storage Sensor:

principle is to store hits and read out during quiet periods, need special technology (combination of CCD and CMOS)

Monolithic Active Pixel Sensors (MAPS)



- Commercial CMOS technologies
- Very few transistors per cell
- Pixel size : 20 x 20 micron or lower
- Charge collection by diffusion, more sensitive to bulk damage (see next slides)
- Serial readout, slower readout
- Time tagging can be envisaged but then would like fast signal collection, and requires extra power

Example: three transistor cell

Monolithic Active Pixel Sensors (MAPS) Radiation tolerance

- **Ionising radiation tolerance (chips irradiated with 10 keV X-Rays) :**
  - ✳ **Pixels modified against hole accumulations (thick oxide) and leakage current increase (guard ring)**
  - ✳ **MIMOSA-15 tested with $\sim$ 5 GeV e^- at DESY after 10 kGy exposure : Preliminary results**
    - T = - 20°C, $t_{r.o.} \sim 180\ \mu s$
    - $t_{r.o.} << 1$ms crucial at T_{room}

Integ. Dose	Noise	S/N (MPV)	Detection Efficiency
0	9.0 $\pm$ 1.1	27.8 $\pm$ 0.5	100 %
1 MRad	10.7 $\pm$ 0.9	19.5 $\pm$ 0.2	99.96 $\pm$ 0.04 %

- **Non-ionising radiation tolerance (chips irradiated with O(1 MeV) neutrons):**
  - ✳ **MIMOSA-15 (20 μm pitch) tested on DESY e^- beams : Preliminary results**

- T=-20°C, $t_{r.o.} \sim 700\mu s$
  - 5.8·10^{12} n_{eq}/cm^2 values with standard & soft cuts

Fluence (10^{12} n_{eq}/cm^2)	0	0.47	2.1	5.8 (5/2)	5.8 (4/2)
S/N (MPV)	27.8 $\pm$ 0.5	21.8 $\pm$ 0.5	14.7 $\pm$ 0.3	8.7 $\pm$ 2.	7.5 $\pm$ 2.
Det. Efficiency (%)	100.	99.9 $\pm$ 0.1	99.3 $\pm$ 0.2	77. $\pm$ 2	84. $\pm$ 2.

  - ✳ **MIMOSA-18 (10 μm pitch) tested at CERN-SPS (120 GeV π^- beam) : Preliminary results**
    - T = - 20°C, $t_{r.o.} \sim 3$ ms
    - parasitic 1–2 kGy γ gas $\Rightarrow$ N ↗

Fluence (n_{eq}/cm^2)	0	6·10^{12}	1·10^{13}
Q_{clust} (e^-)	1026	680	560
S/N (MPV)	28.5 $\pm$ 0.2	20.4 $\pm$ 0.2	14.7 $\pm$ 0.2
Det. Efficiency (%)	99.93 $\pm$ 0.03	99.85 $\pm$ 0.05	99.5 $\pm$ 0.1

- **Conclusion :**
  - ✳ observed ionising radiation tolerance: O(10 kGy)
  - ✳ observed non-ionising rad. tol.: $>$ 1·10^{13} n_{eq}/cm^2 (10μm pitch) & 2·10^{12} n_{eq}/cm^2 (20μm pitch)

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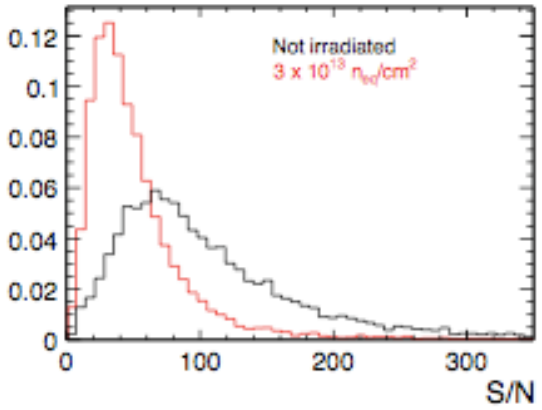
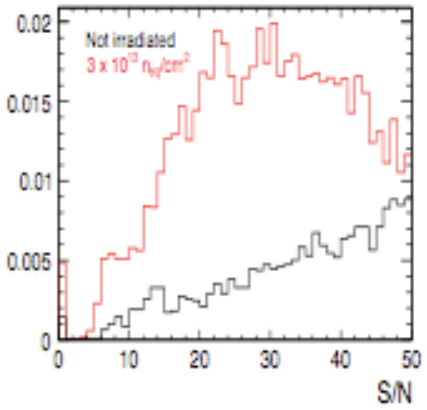
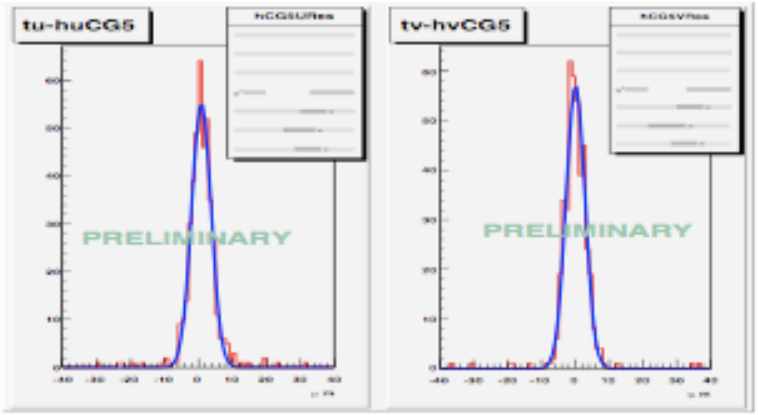
MAPS: Radiation tolerance: the benefit of collection by drift

- **Advantages of depleted epitaxial layer:**
  - ⁂ *faster charge collection (< 10 ns) ⇛ faster frame read-out frequency possible*
  - ⁂ *shorter minority charge carrier path length ⇛ improved tolerance to non-ionising radiation*
- **Exploration of 0.6 μm techno:** ~ 15 μm thick epitaxy ; $V_{dd} \leq 5$ V ; $\rho \sim O(10^3)\Omega \cdot cm$
  - ⁂ MIMOSA-25: fabricated in 2008 & tested at CERN-SPS before/after O(1 MeV) neutron irradiation







- **Effect of $3 \cdot 10^{13} n_{eq}/cm^2$ at room temperature:** ($\sigma_{sp} \sim 2.5 \pm 0.2\ \mu m$)
  - ⁂ SNR(MPV): ~ 60 ↘ ~ 30 ▷ ϵ_{det}: 99.9...% ↘ 99.5% at T_{room} with 20μm pitch & 80μs r.o. time
  - ⇛ thin depleted epitaxy approach validated for $\gtrsim 10^{14} n_{eq}/cm^2$ ▷ 0.35 μm version available soon

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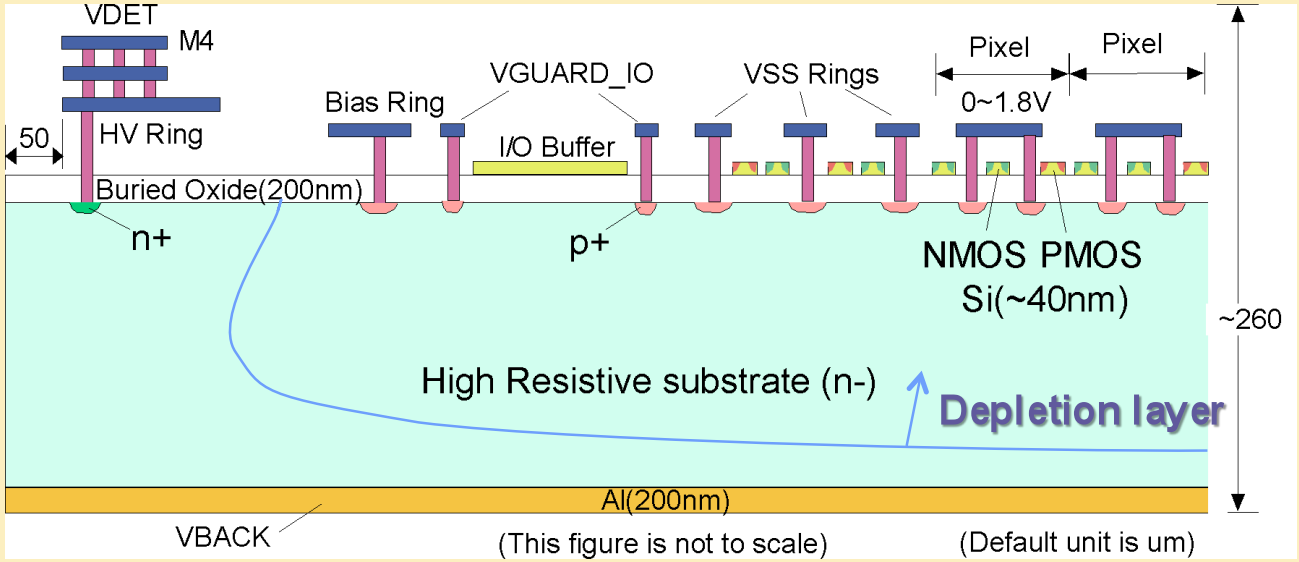
Silicon-On-Insulator (SOI)



- Buried oxide separates detector silicon from readout silicon
- Example: OKI Fully depleted 0.2μm CMOS on , ~18 Ω-cm, p-type, ~40 nm, 700 Ω-cm (n-type) detector material
- Quite some experience developed
- Working on issues: back gating effect at detector reverse bias, radiation tolerance difficult due to charge accumulation in the buried oxide

R. Ichimiya (KEK) SOI Pixel collaboration http://rd.kek.jp/project/soi/

EXAMPLES OF « TRADITIONAL » MONOLITHIC DETECTORS

- Non-standard processing on very high resistivity substrate -> volume production is main challenge
  - CCD on high resistivity substrate
  - DEPFET
  - Stanford-Hawaii
  - …

Or

- Implementation in more or less standard commercial process
  - MAPS
  - CCD with epi or on more standard substrate
  - MAPS and CCD based on serial readout
  - Silicon-on-Insulator (SOI) promising but radiation tolerance difficult

3D or vertically integrated detectors

The Italian VIPIX project (Vertically Integrated PIXels)

- **8 labs participating in this program supported by INFN** (Italian Institute for Nuclear Physics):

  Bologna, Pisa, Perugia, Pavia-Bergamo, Roma3, Milano, Trento, Trieste

- **Vertically integrated pixel detectors** have the potential to satisfy the needs of the next generation of high energy physics experiments (main interest of VIPIX groups: Super B-Factory):

  • **small pitch pixels** capable of handling high data rates.

  • **complex functionalities at the pixel level** (low-noise amplification, zero suppression, time stamping...)

- The Tezzaron/GlobalFoundries technology appears to be very interesting for the fabrication of three-dimensional microelectronic circuits:

  • monolithic active pixel sensors

  • mixed-signal integrated circuits for the readout of high-resistivity fully-depleted silicon pixel sensors.

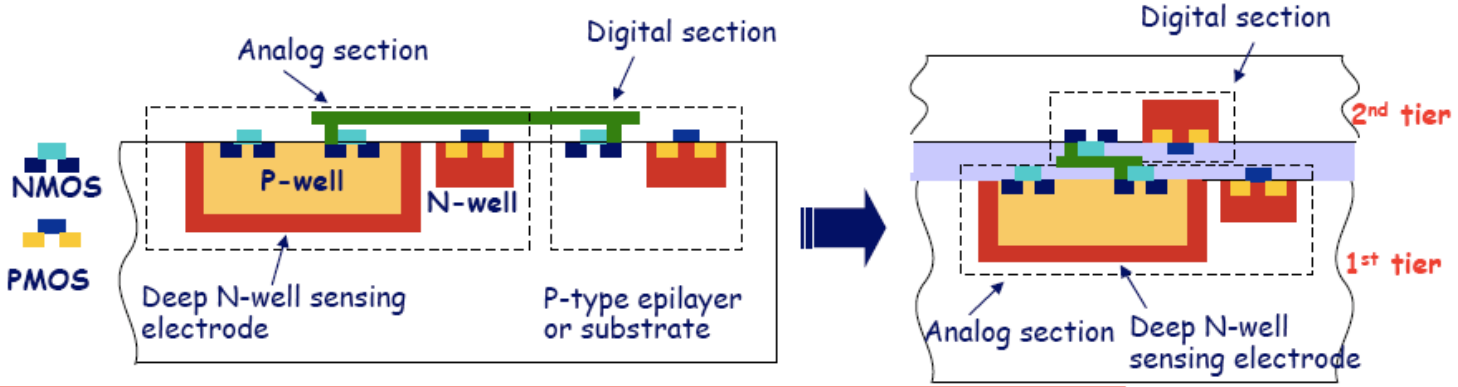
V. Re 2

3D or vertically integrated detectors

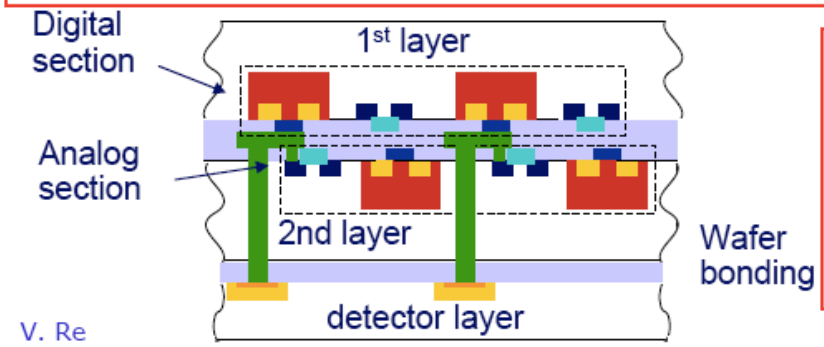
VIPIX concepts for 2-tier devices in the Tezzaron/GlobalFoundries process

3D MAPS

Convert 2D MAPS device to a full CMOS 3D design, with digital readout separated from the sensor and the analog front-end



3D mixed-signal readout integrated circuits



Interconnection between a 3D CMOS readout electronics chip and a fully-depleted high resistivity sensor, possibly with a low-mass, low-pitch technology

V. Re

3

CMOS on lightly doped substrates ?

- Several applications now demand more lightly doped substrates for reasons of isolation of blocks in the same substrate, reduction of losses for RF… This has lead to some experience and availability of advanced CMOS on higher resistivities.
- We have received feedback from foundry that advanced CMOS can be implemented on resistivities > 100 Ωcm needed to obtain several tens of microns depletion at 100 V

Can we exploit the features of very deep submicron CMOS processes to combine most of the advantages of the previous technologies ?

- Good radiation hardness (charge collection by drift).
- Take advantage of small feature size in advanced CMOS processes
- Low power consumption: target 20 mW/cm^2 in continuous operation.
- Monolithic integration.
- Use of CMOS technologies with high production rate (20 m^2 per day…) and cost per unit area less than traditional detectors
- Significant advantages beyond 130 nm (low K dielectrics in the metal stack)
- Several approaches are in principle possible. As an example in the following the currently ongoing development of LePix will be described.
- First have a more general look at some issues.

DESIGN ASPECTS and ISSUES

- Device
  - One needs to design a device structure (a diode for instance) to collect generated charge onto a designated collection electrode without losing it in some other part of the readout circuit. Collection can be by drift (electric field) or diffusion
  - Need to guarantee uniform response across the sensitive area
  - Would like to minimize collection electrode capacitance
  - Need to avoid electric breakdown
- Process
  - Standard or not ?
- Readout circuitry
  - Would like to minimize power 20mW/cm^2 or less

- Motivation :
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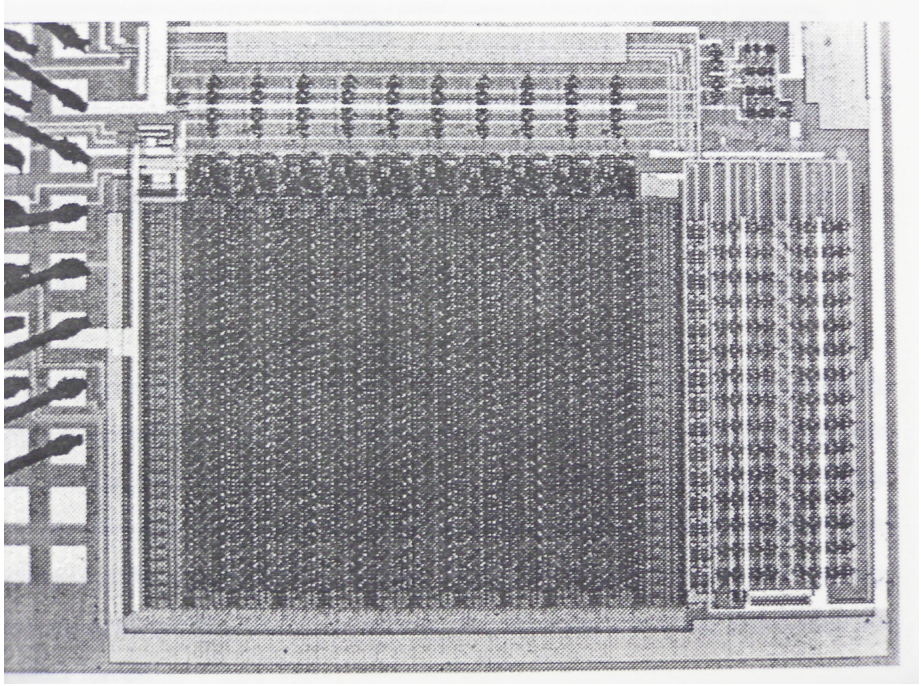
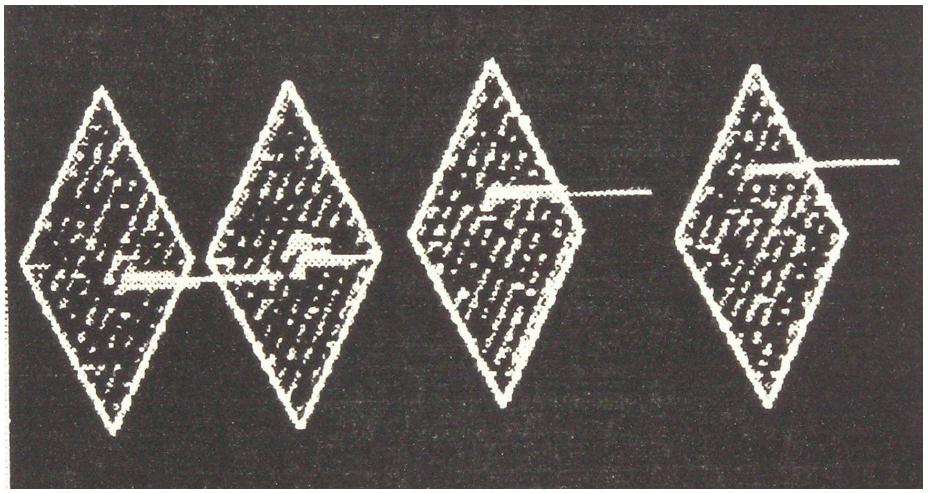
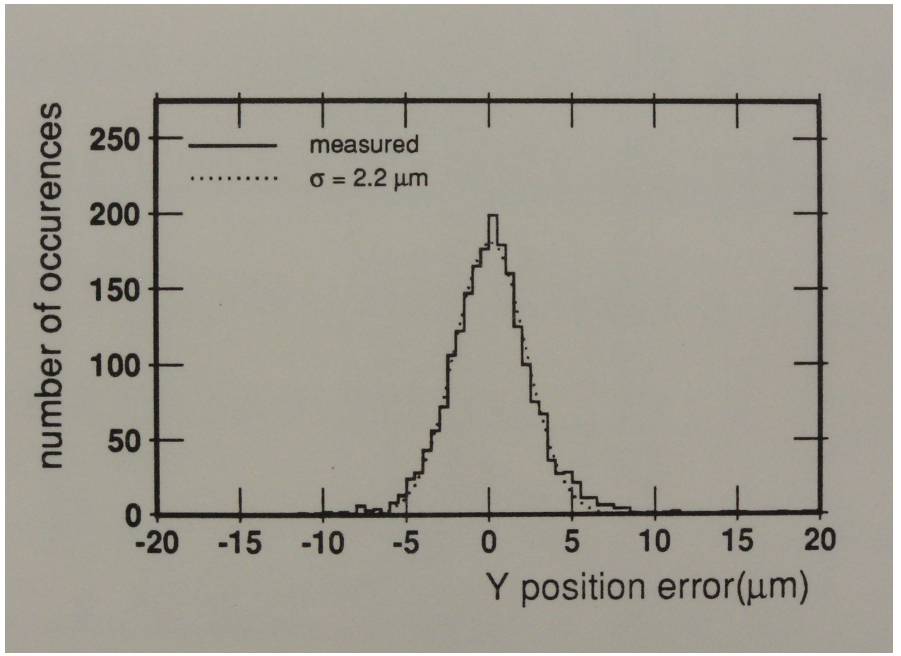
DEVICE DESIGN : A CASE STUDY







C. Kenney, S. Parker (U of Hawaii)

W. Snoeys, J. Plummer et al (Stanford U)

1992

Collection by drift in depletion region

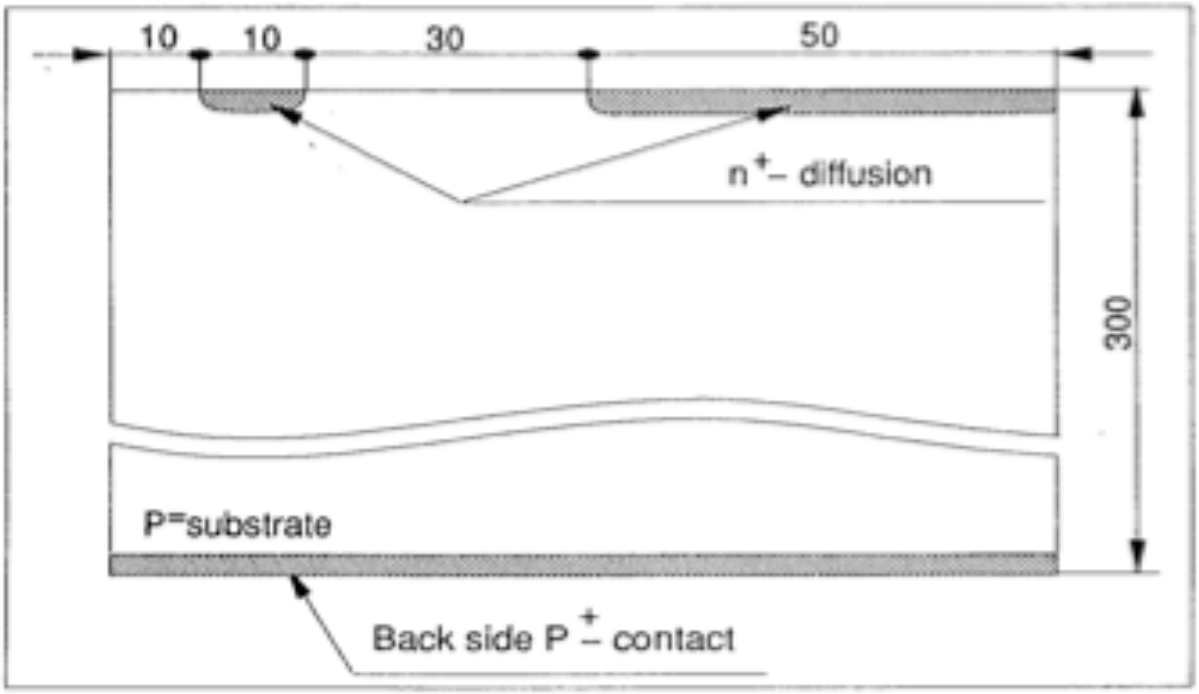
N=1E12cm^{-3} Ccoll=26fF

DEVICE DESIGN

- Case study based on collection by drift in a depleted region
- Use device simulation extensively to understand device behavior, operating margins etc…
- We will see a number of issues: undepletion, punchthrough, etc…

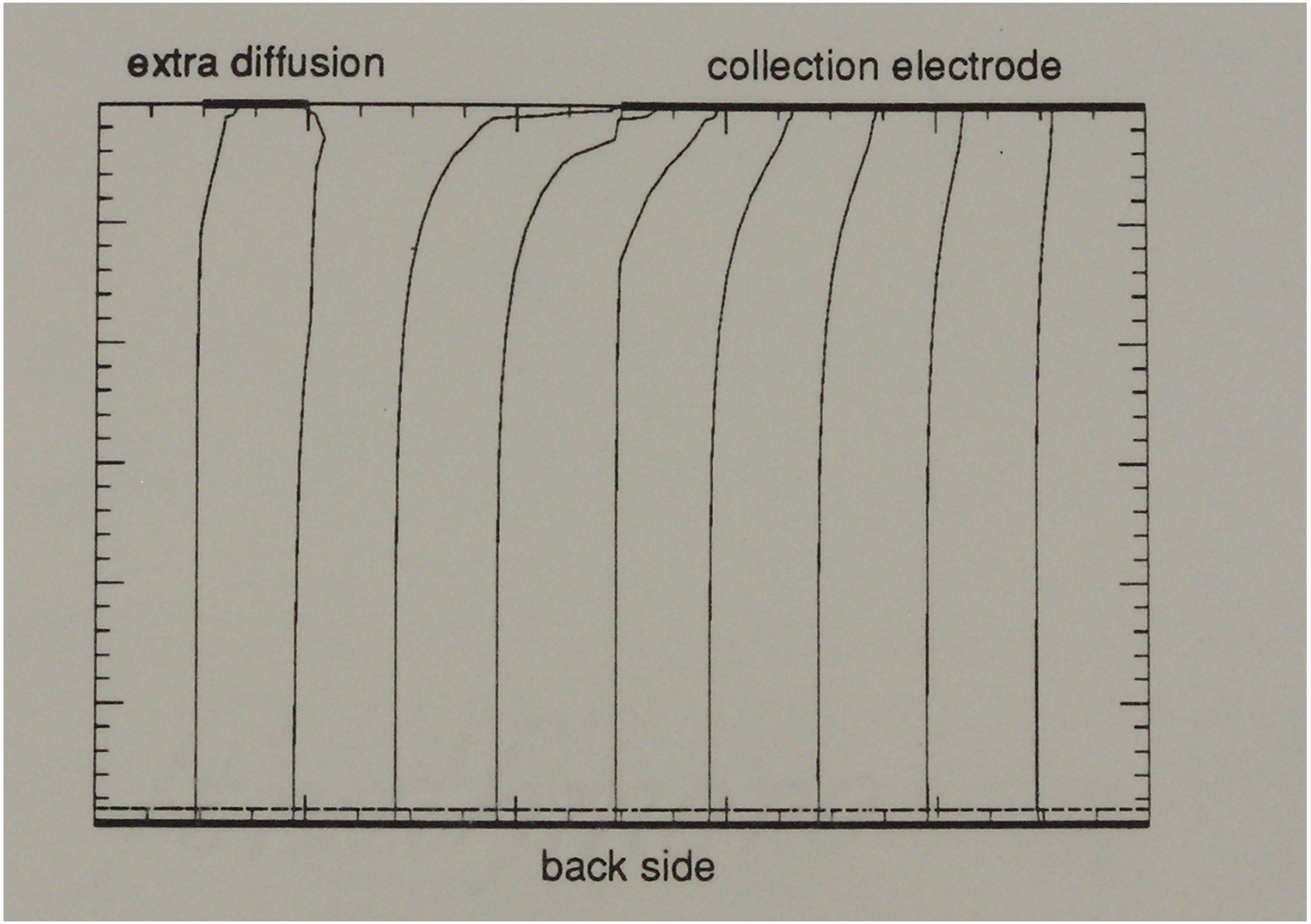
CHARGE COLLECTION ONTO A DESIGNATED COLLECTION ELECTRODE

Extra N+ diffusion N+ Collection electrode



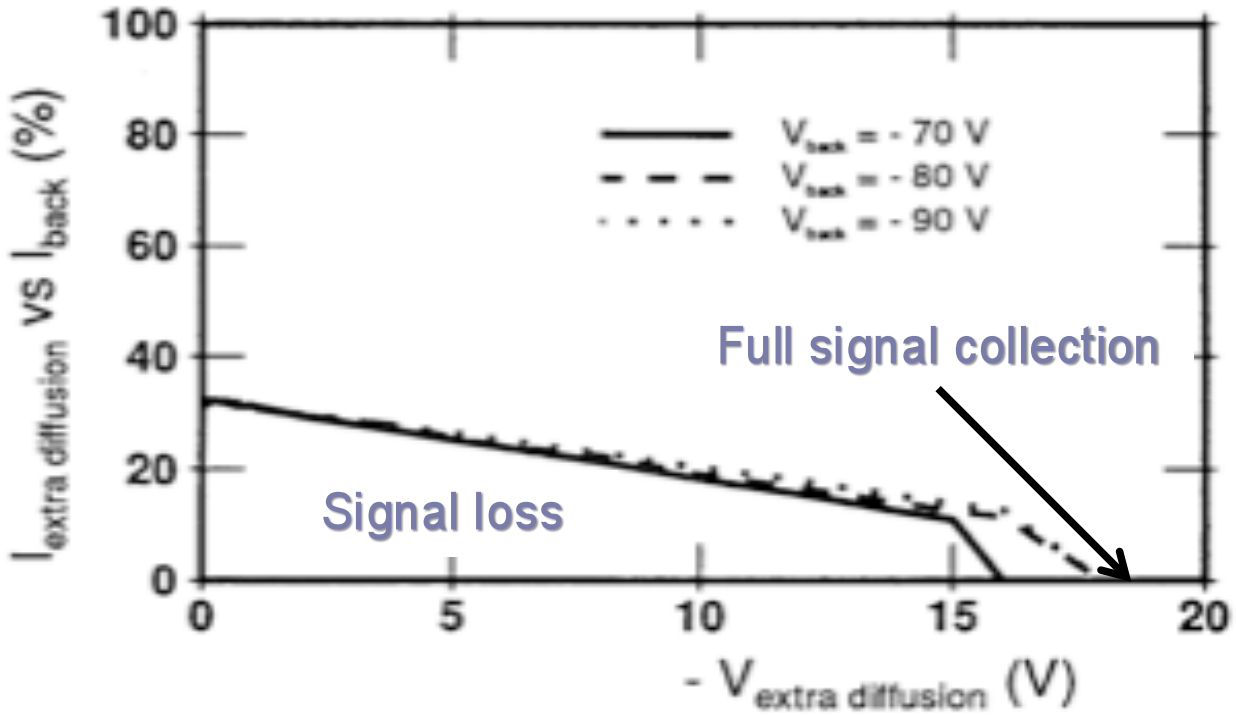
CHARGE COLLECTION ONTO A DESIGNATED COLLECTION ELECTRODE

Extra diffusion collects charge from significant fraction of the area !!



Collection electrode at gnd, Vextra diffusion = -5 V, Vback= -80V

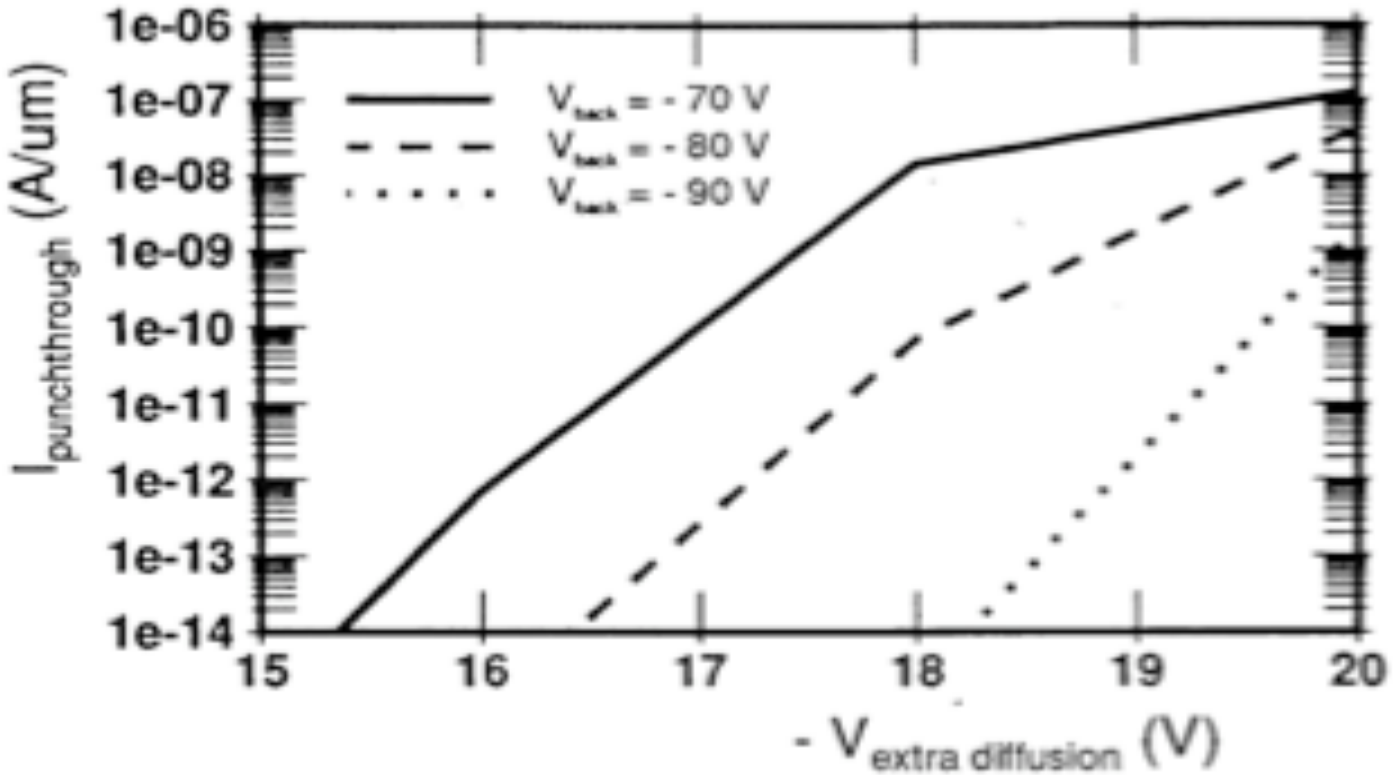
CHARGE COLLECTION ONTO A DESIGNATED COLLECTION ELECTRODE



Large voltage on extra diffusion is required to avoid signal loss !

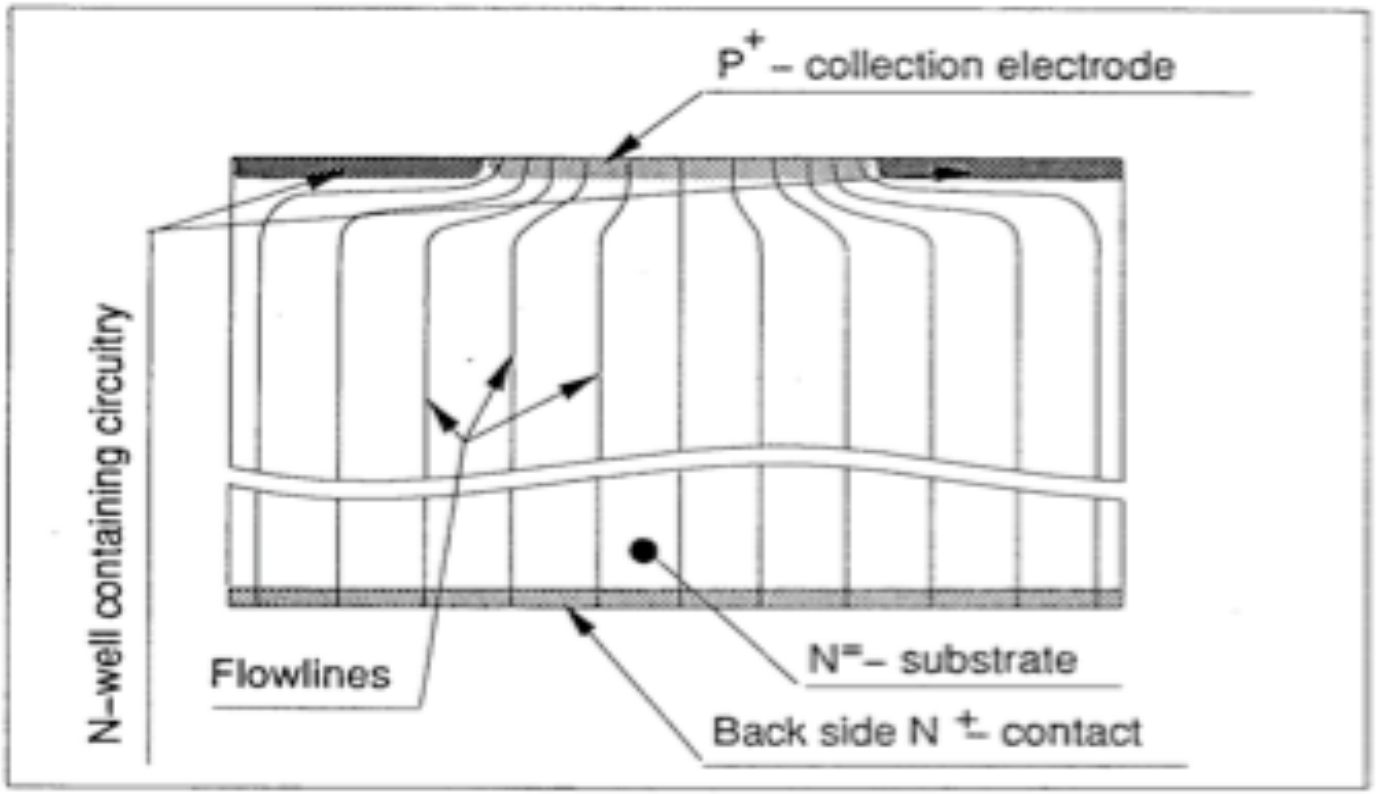
=> Placing readout circuit directly in the substrate and connecting to the collection electrode is difficult

CHARGE COLLECTION ONTO A DESIGNATED COLLECTION ELECTRODE



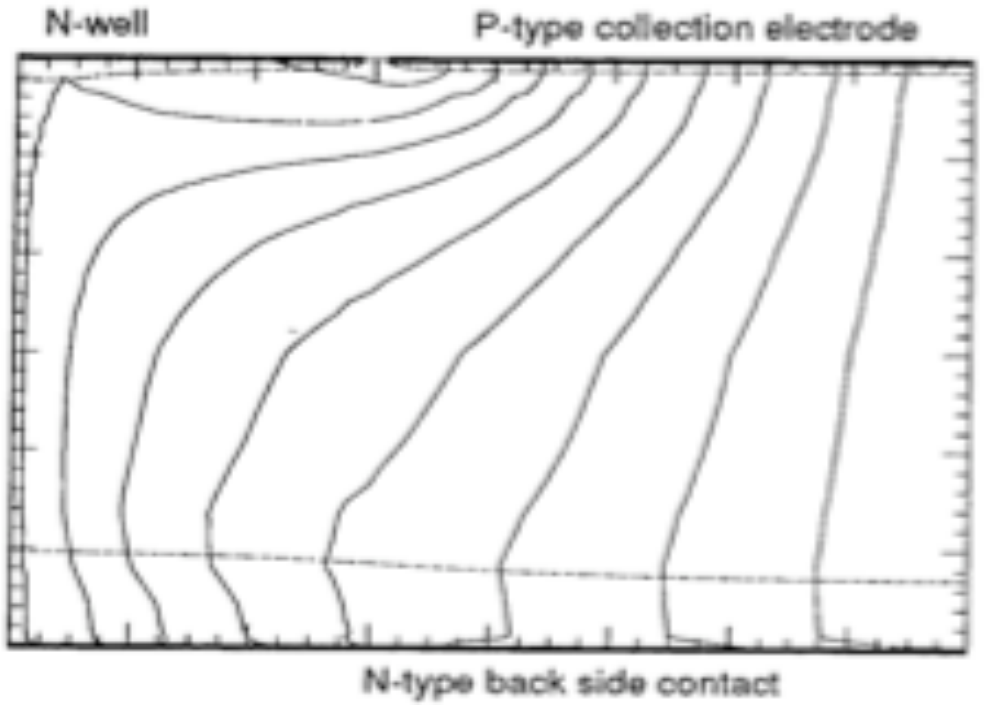
Once charge loss solved
punchthrough between collection electrode and extra diffusion sets in…

USE OF A WELL FOR THE READOUT CIRCUITRY



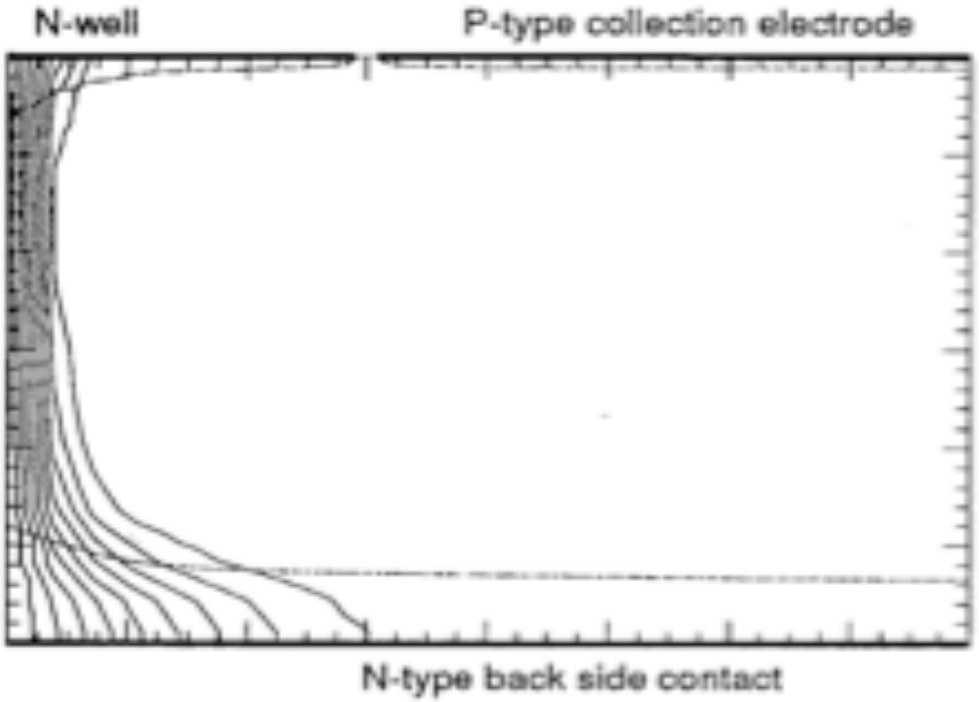
Proposed by S. Parker to shield circuit from detector part by putting it in a well

USE OF A WELL FOR THE READOUT CIRCUITRY



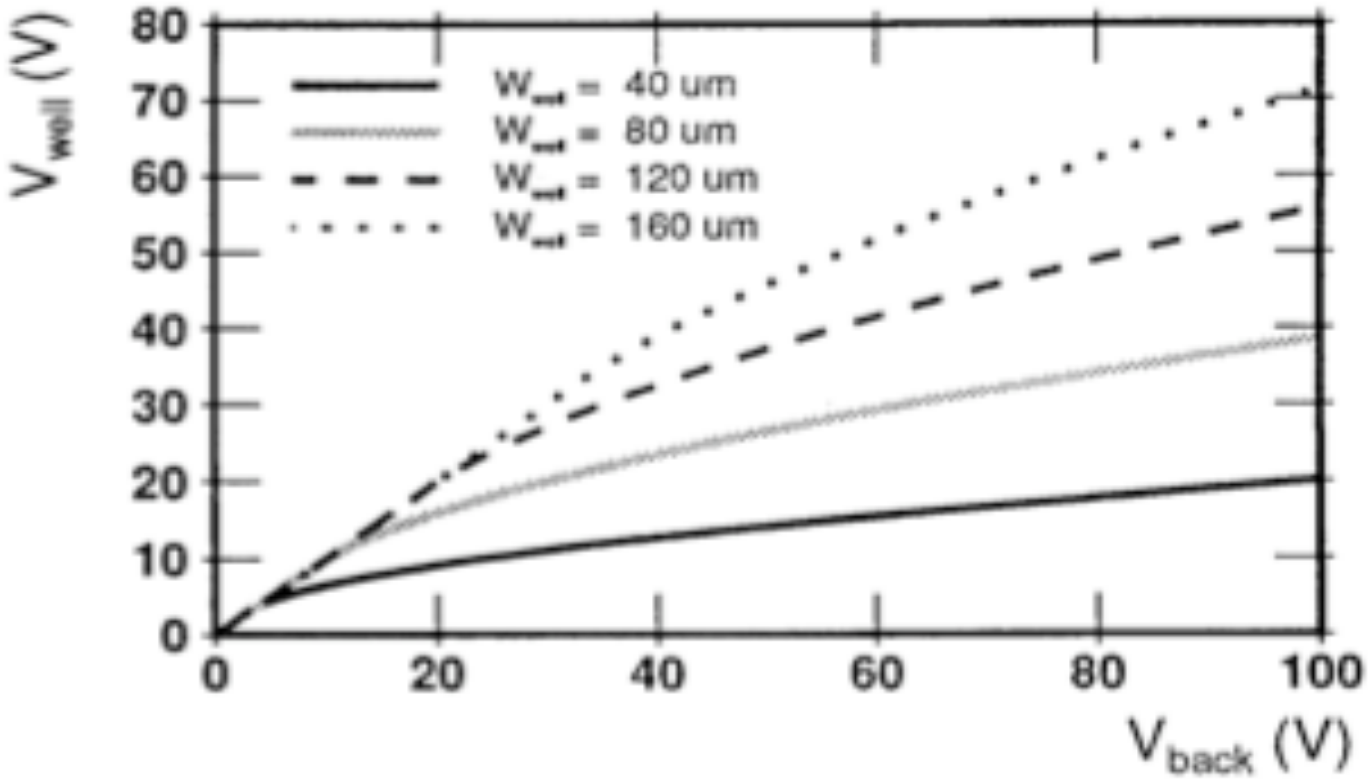
Minimum well bias needed to avoid undepletion and large current between Nwell and back side contact.
Simulation above is a few V above the limit.
Charge is collected on the collection electrode.

USE OF A WELL FOR THE READOUT CIRCUITRY



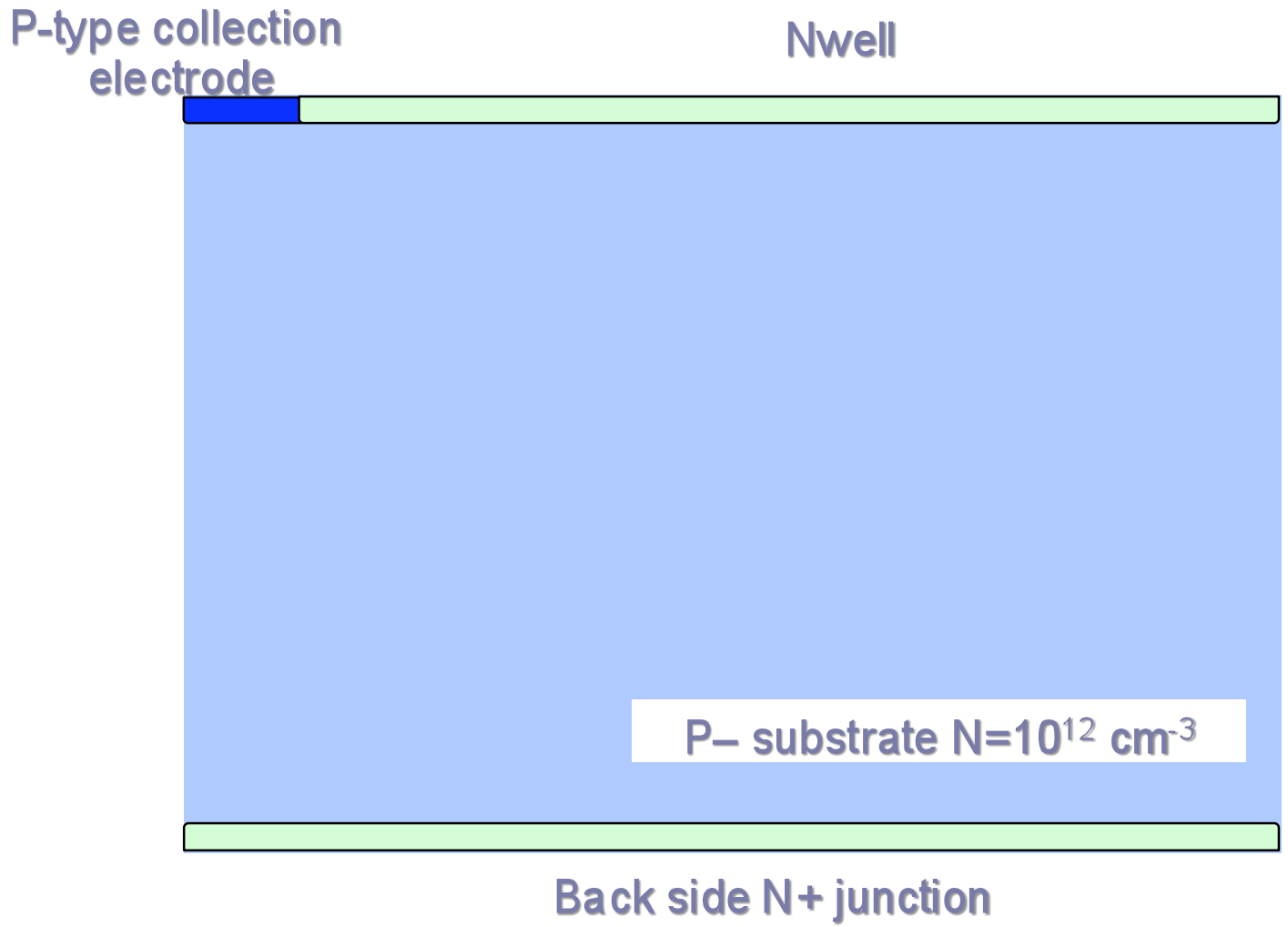
Minimum well bias needed to avoid undepletion and large current between Nwell and back side contact.
Simulation above is just below (a few V) below the limit.

USE OF A WELL FOR THE READOUT CIRCUITRY

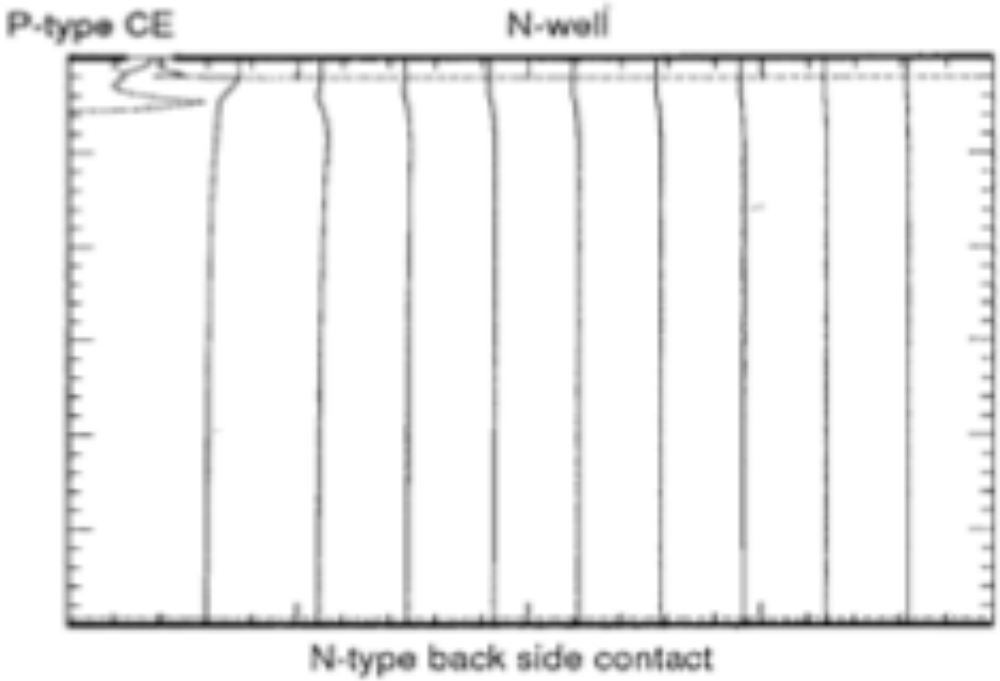


Minimum well bias for a collection electrode of 200 microns wide and various well sizes
Still a large voltage difference between well and collection electrode and also a very large collection electrode size !!

OTHER IDEA: USE OF A WELL WITH BACK SIDE JUNCTION

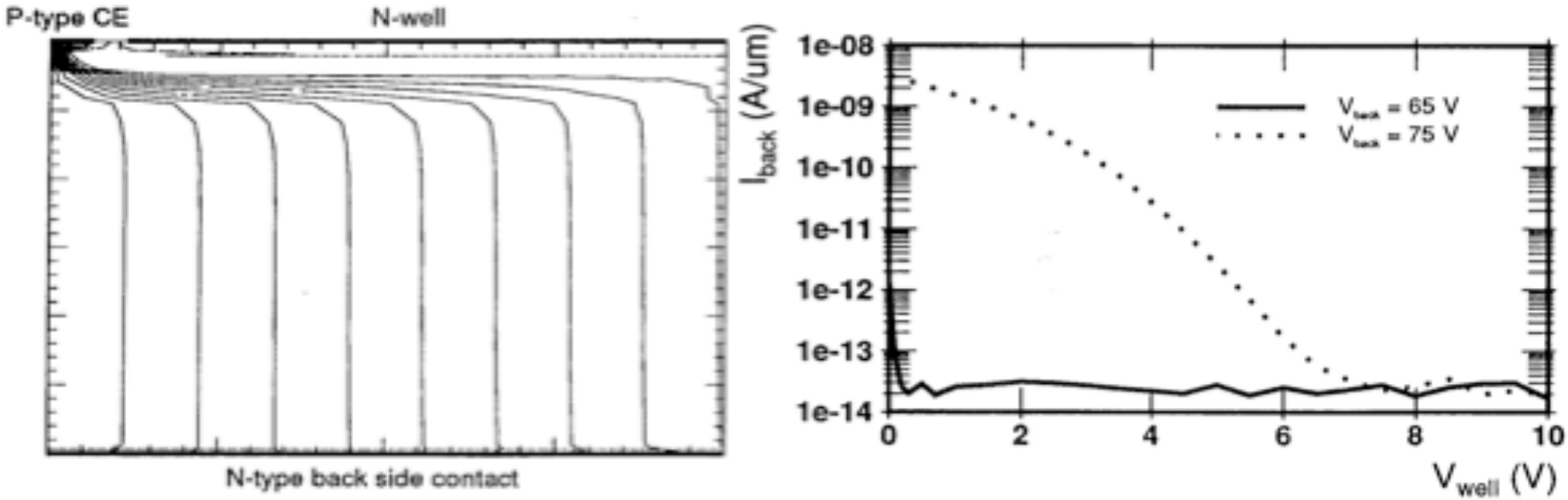


USE OF A WELL WITH BACK SIDE JUNCTION



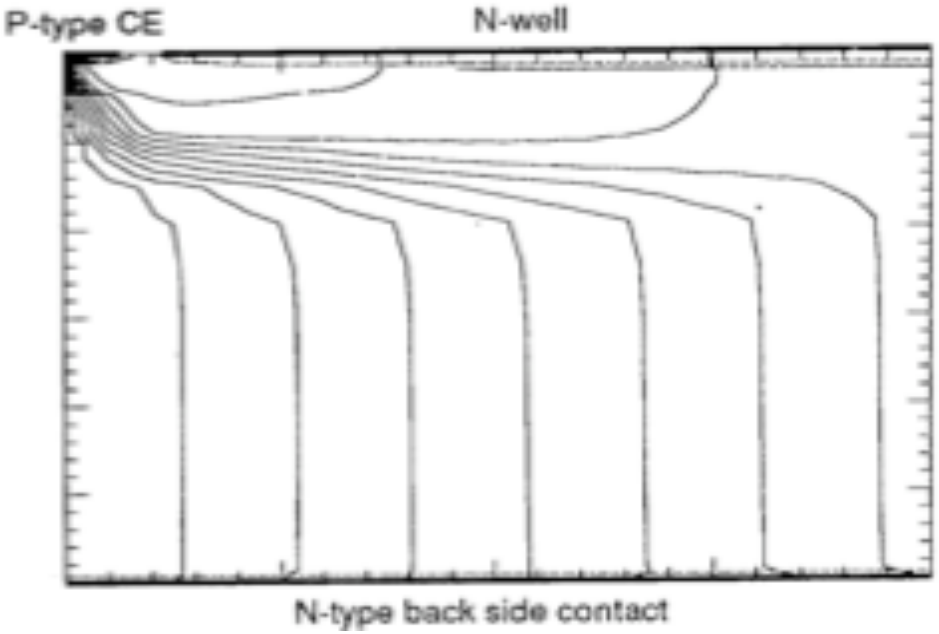
P-type collection electrode covers 1/10 of the width.
Full depletion required (otherwise short between collection electrodes)
At zero well bias and full depletion punchthrough between Nwell and N-diffusion on the back

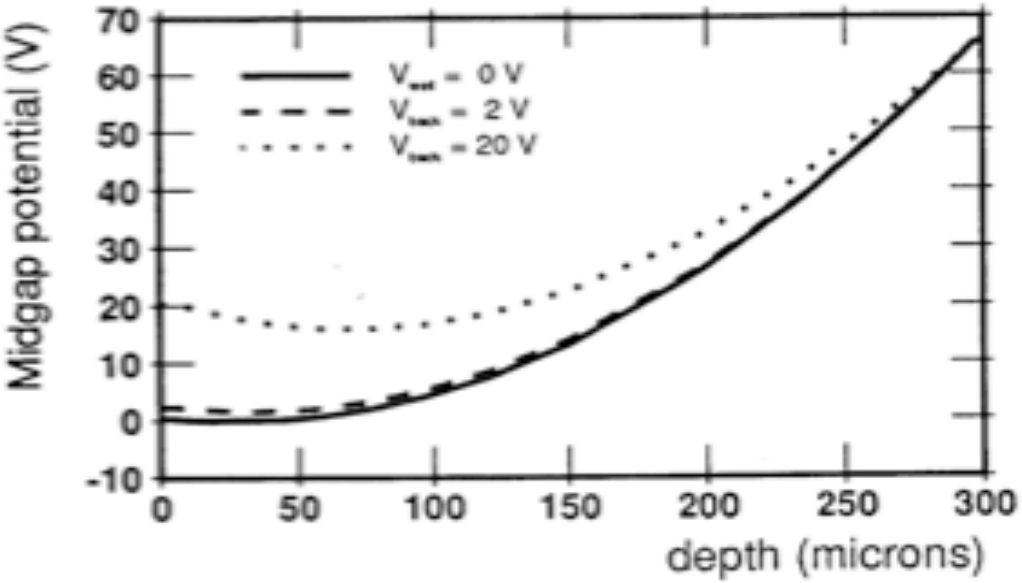
USE OF A WELL WITH BACK SIDE JUNCTION



A few V on the well (with 65 V on the back) diverts all flow lines to the collection electrode because a potential barrier is formed underneath the well The back side to Nwell current drops by orders of magnitude as the punchthrough is eliminated.

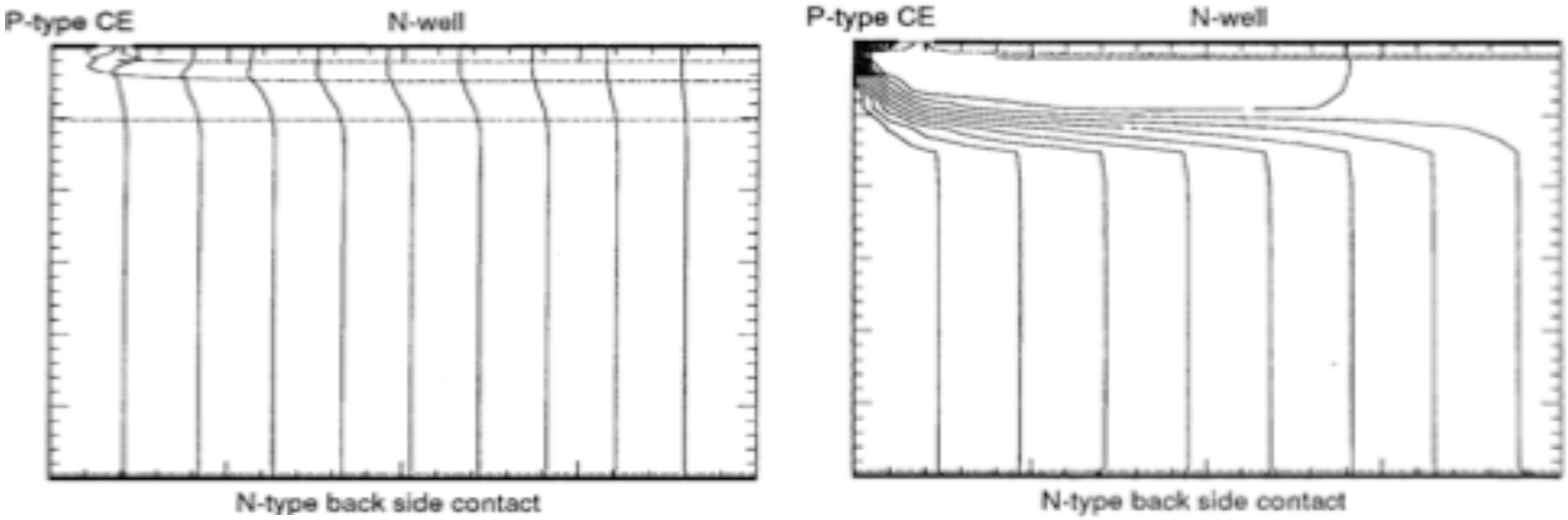
USE OF A WELL WITH BACK SIDE JUNCTION





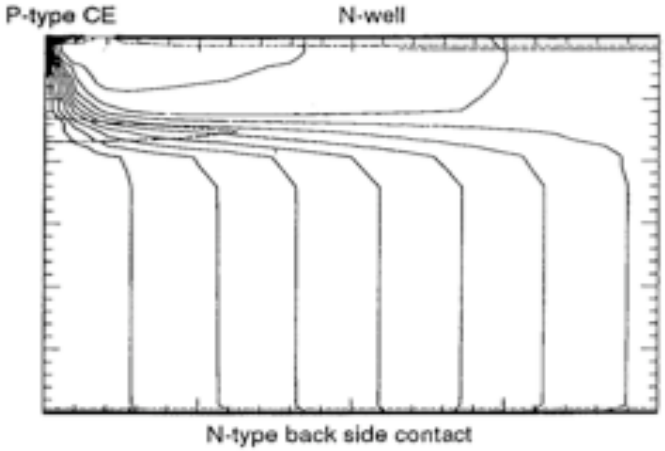
Increasing the well bias increases the potential barrier and moves the potential valley deeper into the substrate

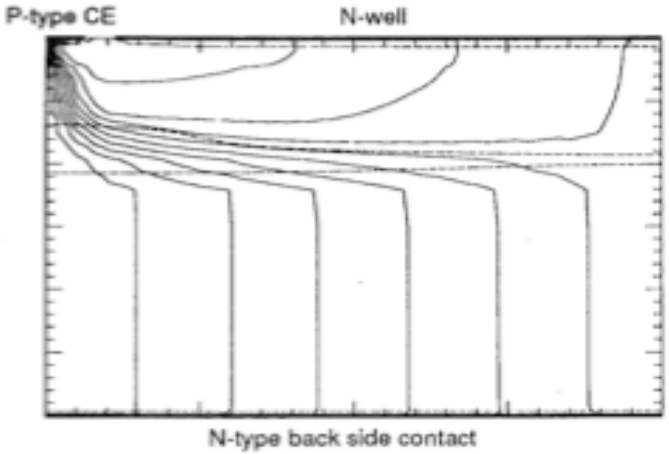
USE OF A WELL WITH BACK SIDE JUNCTION



At lower biases not fully depleted (left). Need a few V (4V) for full depletion (right)

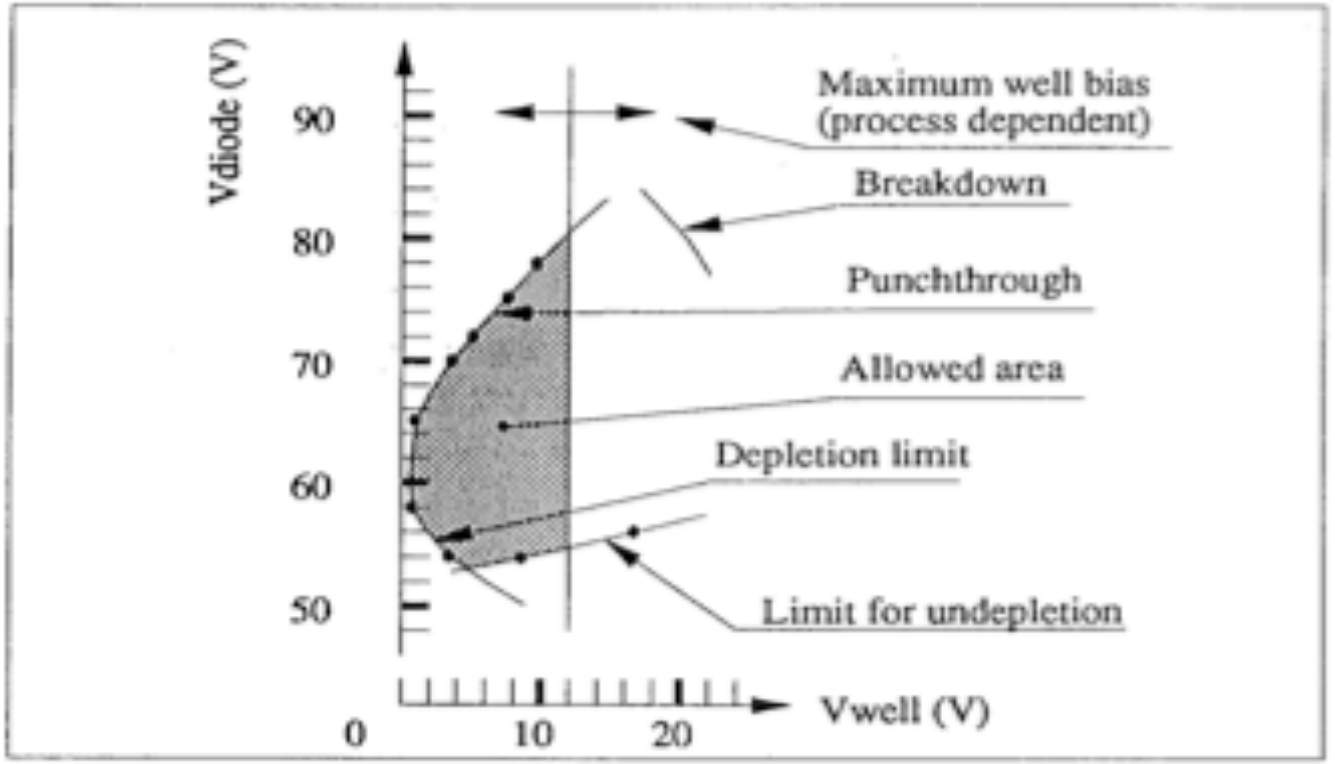
USE OF A WELL WITH BACK SIDE JUNCTION





At high well biases (20 V left) undepletion occurs progressing over the full width when increasing the bias further (30 V right).

USE OF A WELL WITH BACK SIDE JUNCTION

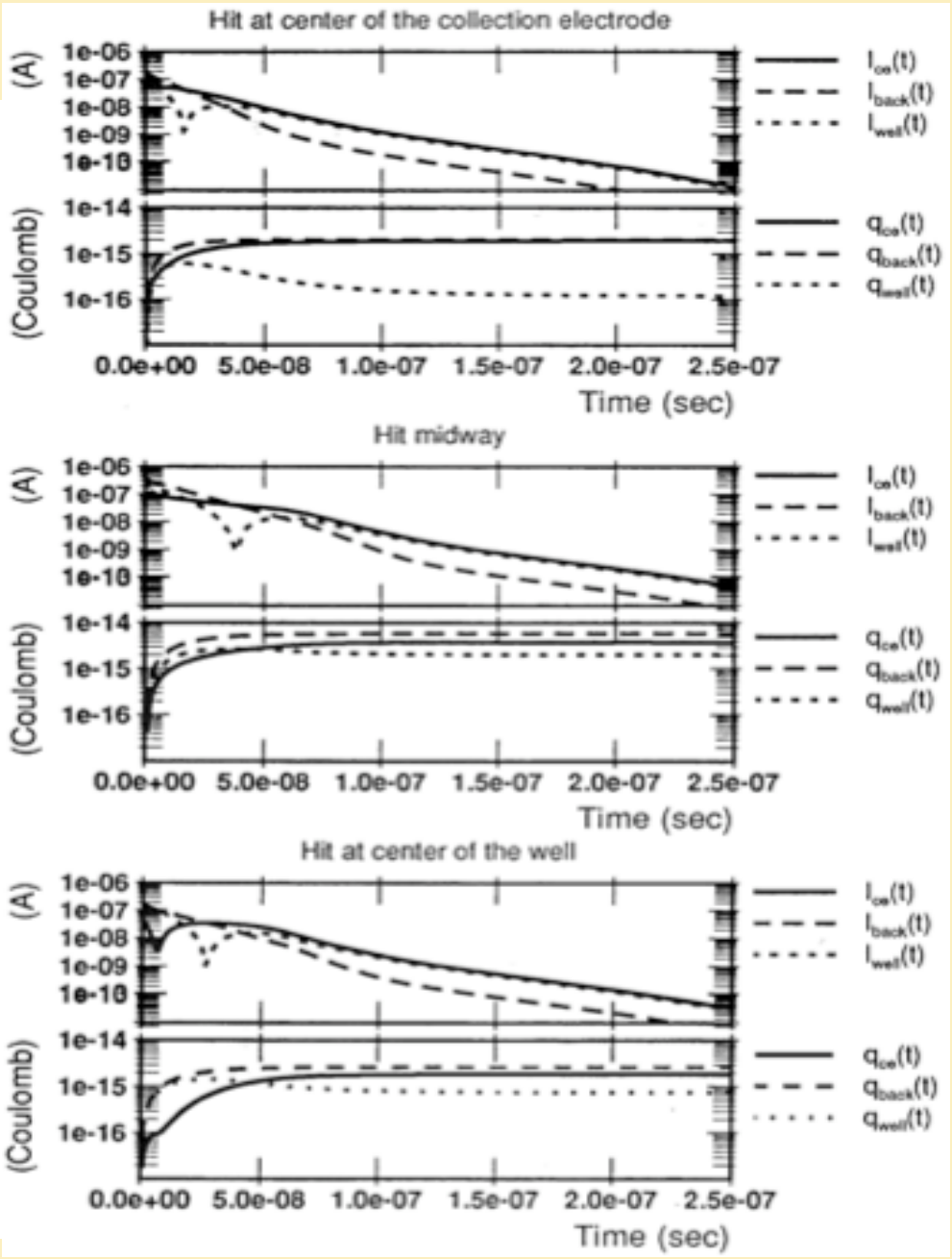


Operational limits

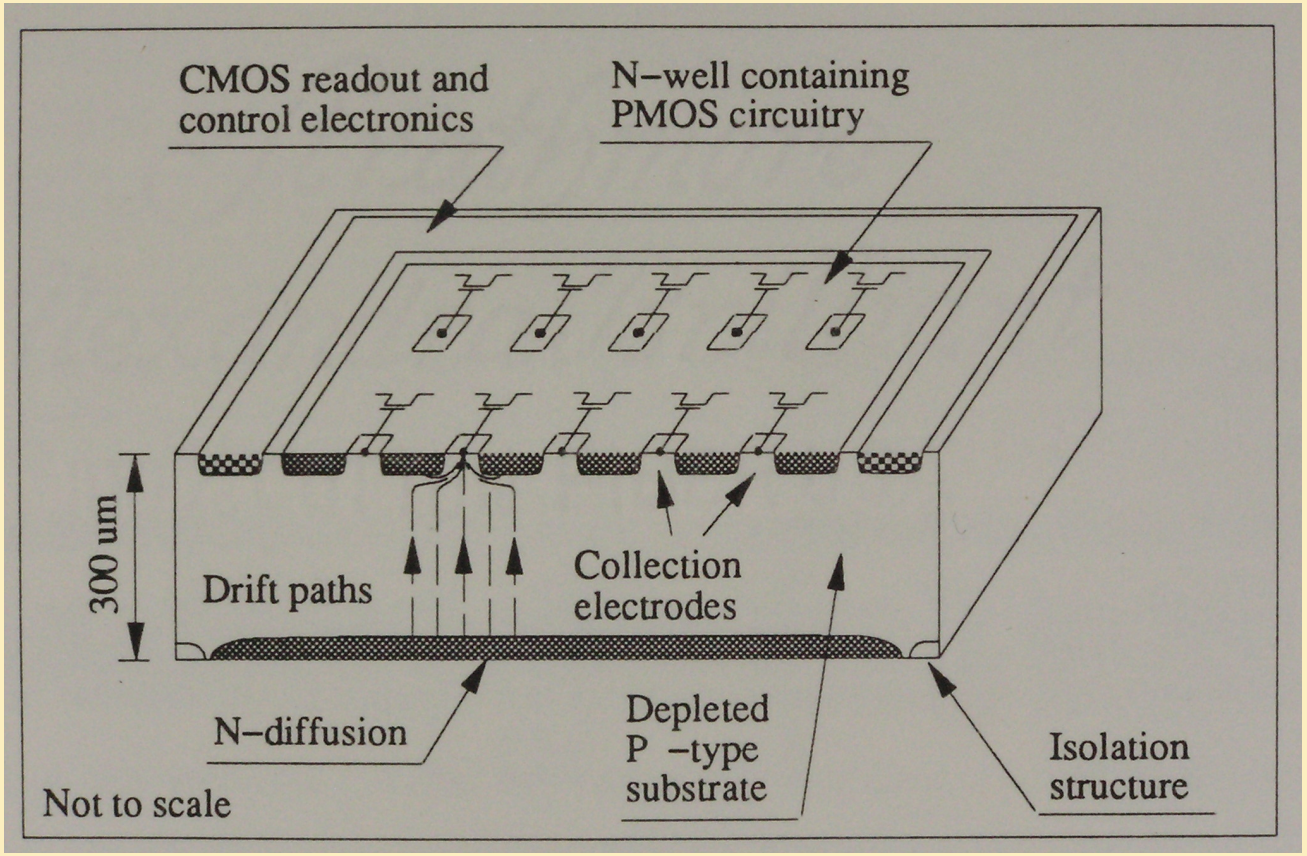
SIGNAL FORMATION

Simulation for different locations of incidence of an ionizing particle

Main issue = speed of signal collection very different depending on the location of incidence of the particle



FINAL DEVICE

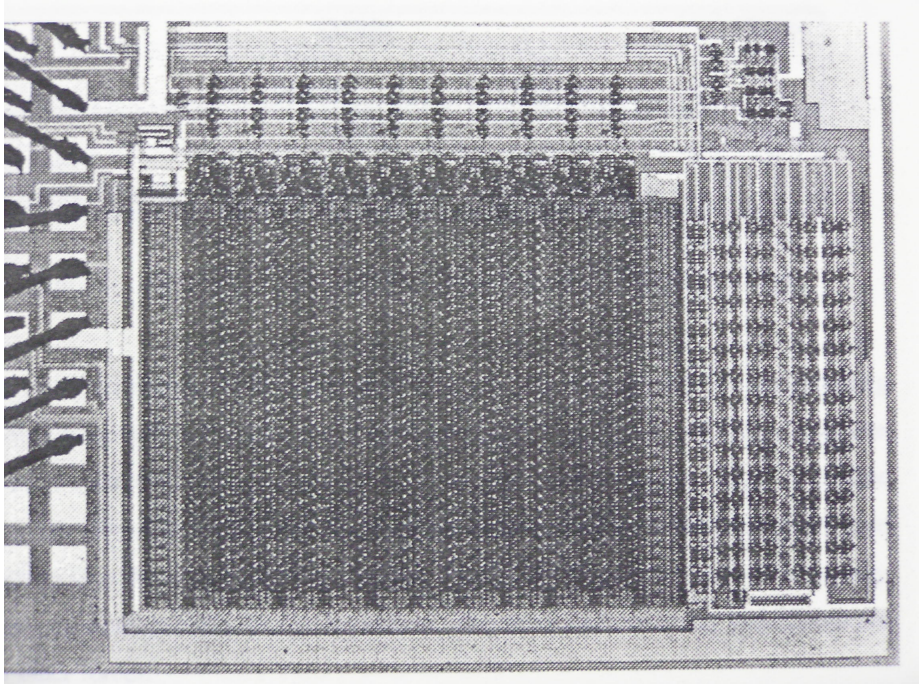


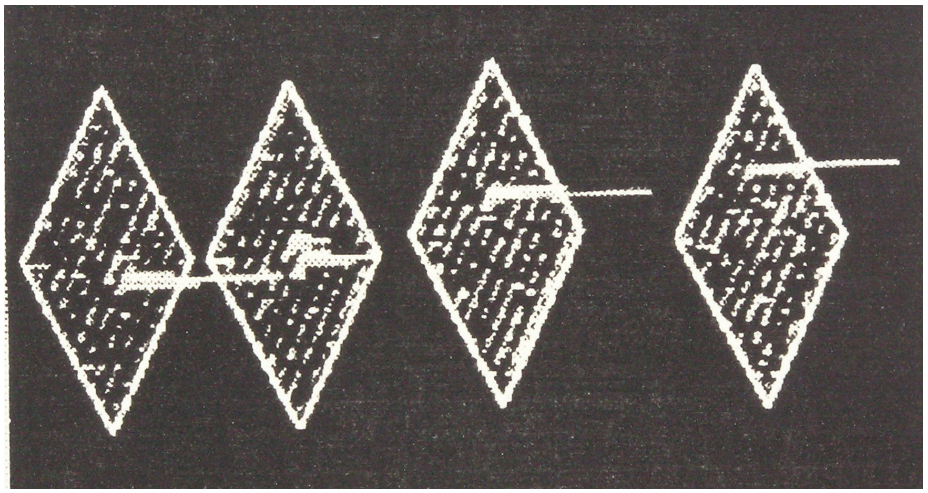
Works well (cfr position resolution)

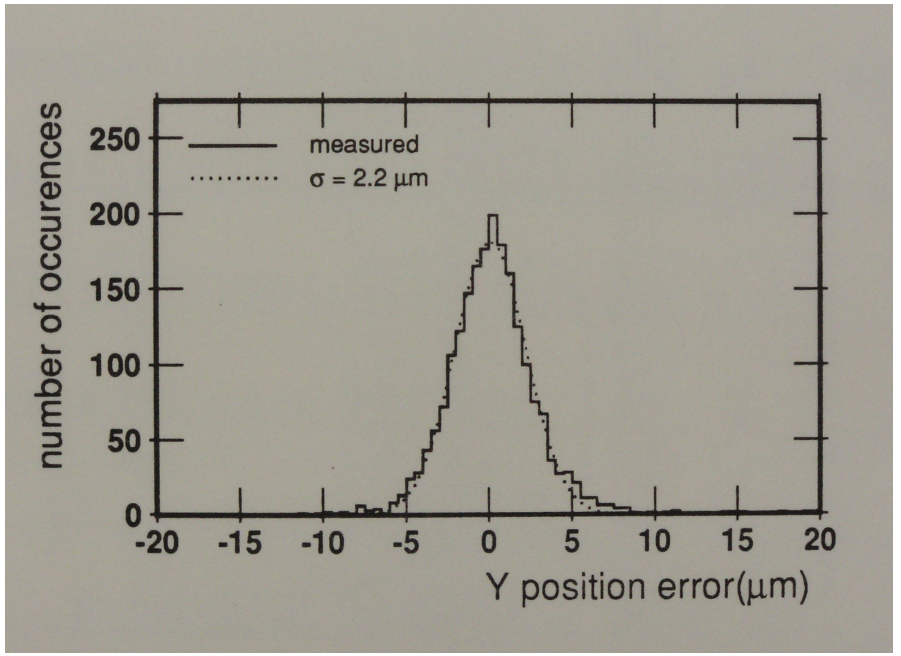
but… non-standard processing, both sides, junction isolation on the back …

Importance of device simulations, can reveal many issues

DEVICE DESIGN : A CASE STUDY







C. Kenney, S. Parker (U of Hawaii)

W. Snoeys, J. Plummer et al (Stanford U)

1992

Collection by drift in depletion region

N=1E12cm^{-3} Ccoll=26fF

PROCESSING just a few remarks

- CMOS standard processing quite advanced now on 200 or 300 mm diameter wafers

Processing very high resistivity silicon has some particularities:

- High resistivity (detector grade) not easily found at larger diameter
- Float-zone silicon contains much less impurities/defects than Czochralski. These defects pin down dislocations, rendering the material more robust. Float-zone material is MUCH MORE FRAGILE
- Several process steps can introduce impurities which increase detector leakage
  - Can work at higher leakage current (might soon be dominated by radiation induced leakage)
  - Can try to make certain steps cleaner
  - Can use gettering techniques, which during processing render defects more mobile and provide traps for these where they are no longer harmful.

- Motivation :
  - Impact of power consumption on material in high energy physics experiments
  - The importance of Q/C for power consumption
- Some examples of monolithic detectors
- Device design & device simulations
- Processing
- Monolithic detectors in deep submicron CMOS : example LePIX
  - Q/C and segmentation
  - Device design
  - Some (analog front end) readout circuits
  - Status of first prototype submission & measurement setup
- Digital part of the readout and power consumption
- Radiation tolerance

CMOS on lightly doped substrates ?

- Several applications now demand more lightly doped substrates for reasons of isolation of blocks in the same substrate, reduction of losses for RF… This has lead to some experience and availability of advanced CMOS on higher resistivities.
- We have received feedback from foundry that advanced CMOS can be implemented on resistivities > 100 Ωcm needed to obtain several tens of microns depletion at 100 V

LePIX: monolithic detectors in advanced CMOS

K. KLOUKINAS, M. CASELLE, W. SNOEYS, A. MARCHIORO, W. BIALAS, C.MANSUY, Y. PALENZUELA

CERN CH-1211, Geneva 23, Switzerland

A. RIVETTI, V. MANZARI, D. BISELLO, A. POTENZA, N. DEMARIA, M. COSTA, P. GIUBILATO

I.N.F.N.

A. DOROKHOV, C. HU, C. COLLEDANI, M. WINTER

IPHC Strasbourg

P. CHALMET, H. MUGNIER, J. ROUSSET

MIND-MicroTechnologies-Bât. Archamps

M. BATTAGLIA

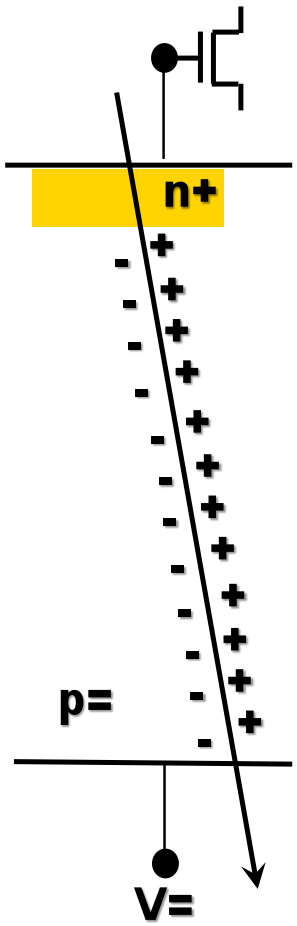
UC Santa Cruz

J. SPALEK

Kosice

✓ Within INFN project funded by the R&D scientific committee (Torino, Bari, Padova…)
✓ C4i-MIND is financed by the Dept. de la Haute Savoie.
✓ CERN, IPHC, INFN and Imperial participate in the prototype production cost

Analog power



- 10 mW/cm^2 = 1 microW/(100x100 micron)
- Example: Basic element of 100x100 micron with 1 μA of current (so we split elements to optimize power to signal/noise ratio) – We are now also looking at 50x50, maybe regrouped
- Strategy: moderately small pixel to exploit capacitance reduction through segmentation
- Take transistor noise at 40 MHz BW

$$Veq \approx 0.16mV$$

$$\frac{S}{N} = 25 \Rightarrow \frac{Q}{C} = 4mV \quad \boxed{= \frac{4\,fC}{1\,pF}} \quad \boxed{= \frac{0.4\,fC}{0.1\,pF}} \quad \boxed{= \frac{0.04\,fC}{10\,fF}}$$

Collection depth 300 μm 30 μm 3 μm

Could fit both monolithic and non-monolithic approach !

Analog power : low C is the key

Thermal noise $\sim \frac{1}{\sqrt{gm}} \sim \frac{1}{I^m}$ where $m < 1/2$

Signal-to-Noise $\sim \frac{Q \times I^m}{C}$

Weak dependence of the noise on current !

For constant signal to noise

Current I per channel : $I^{-m} \sim \frac{Q}{C}$ or $I \sim (C/Q)^{2\ldots4}$

Weak … Strong inversion

Segmentation

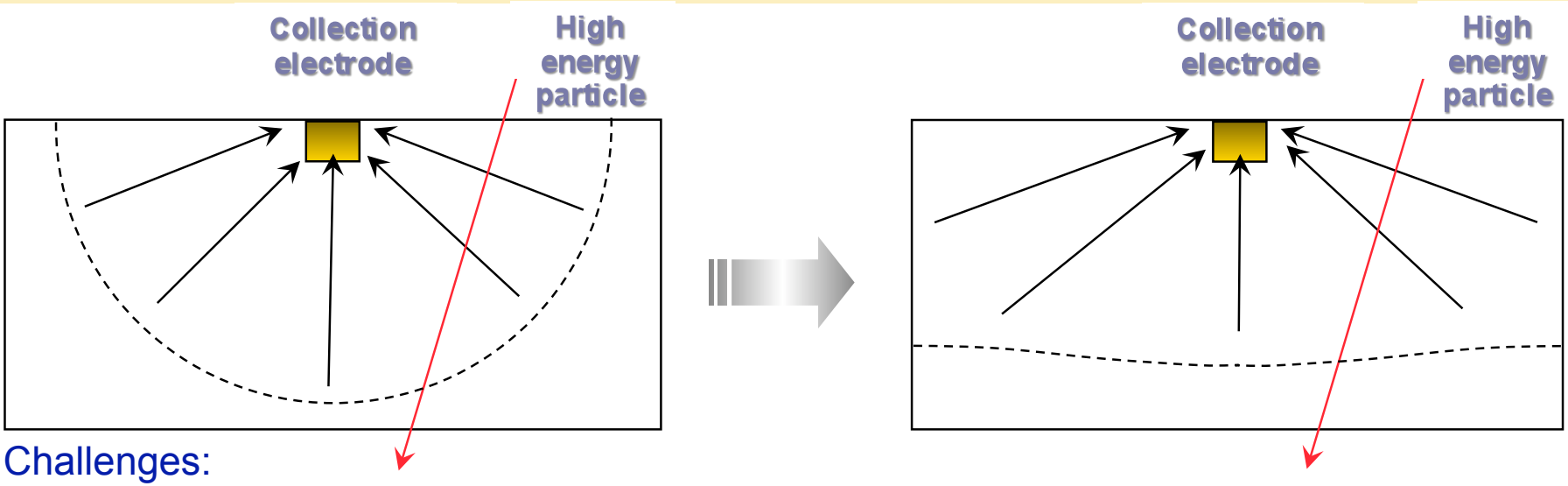
Number of elements N, C~1/N: Total analog Power $\sim N(C/Q)^{2\ldots4} \sim (1/N)^{1\ldots3}$

Higher segmentation is (very) good

Decreased depletion layer thickness -> need to segment in proportion

Xd ÷ 2 -> C ÷ 2

Device design: uniform depletion layer for a small collection electrode

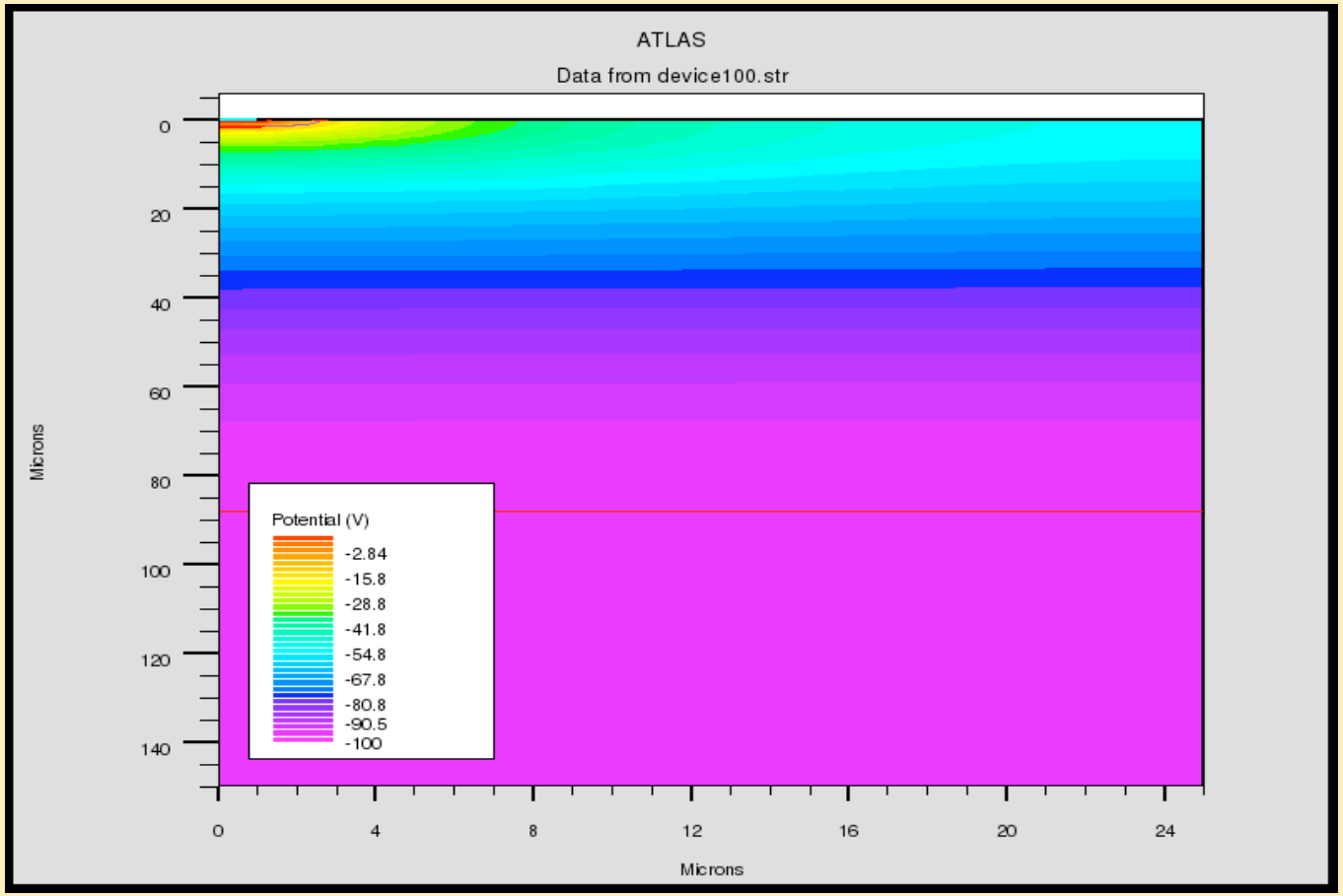


- Challenges:
- Obtaining a uniform depletion layer for uniform response
- Optimal geometry and segmentation of the read-out electrode **(PUSH FOR MINIMUM C)**
- Effective charge resetting scheme: needs to be robust over a large range of leakage currents
- Pattern density rules in very deep submicron technologies are very restrictive.
- Insulation of the low-voltage transistors from the high voltage substrate.

Sensor needs to be designed in close contact with the foundry!

Collection by drift will limit charge sharing and reduce cluster size

Device design: uniform depletion layer even with small collection electrode



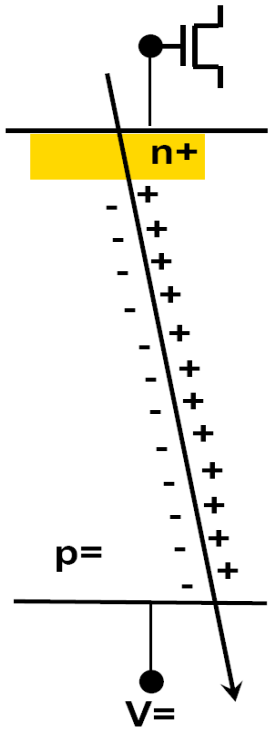
✓Pixel pitch used in this 2D simulation was 50 μm.

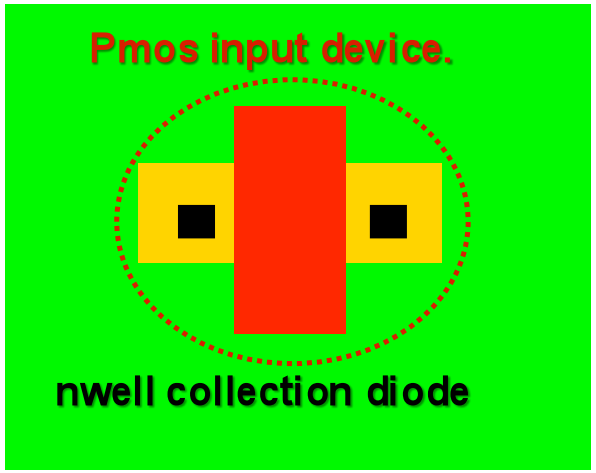
✓With the highest resistivity substrate available 80 μm depletion with 100 V

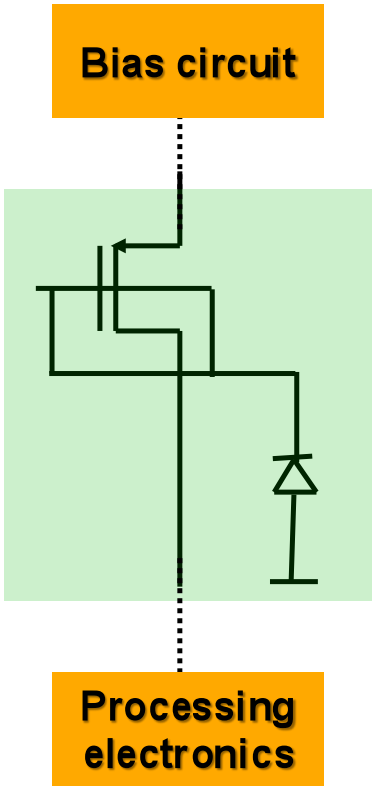
Small collection electrode

- Most of the collection electrode capacitance to ground (or at least not to the neighboring pixel)
- No issue with pixel-to-pixel capacitive cross-talk
- We could consider open loop amplifier (like MAPS), but need time tagging at the 25ns level
- Distributing the clock to every pixel will cost significant much power 10fF*10000 elements in one square cm at 40MHz 1V swing = 4mW per square cm already
- Therefore try to use analog power to send signal to the periphery

Approach



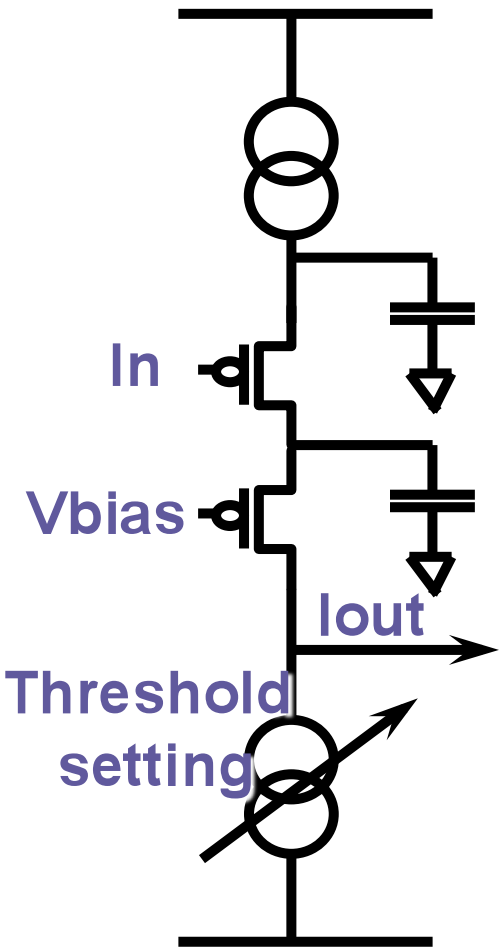




- Charge to voltage conversion on the sensor capacitance
- For 30 μm depletion and 10fF capacitance: 38 mV for 1 mip.

- ✓ Only one PMOS transistor in the pixel (or maybe very few…)
- ✓ Each pixel is permanently connected to its front-end electronics located at the border of the matrix.
- ✓ Each pixel has one or two dedicated lines: need of ultra fine pitch lithography => 90 nm CMOS.

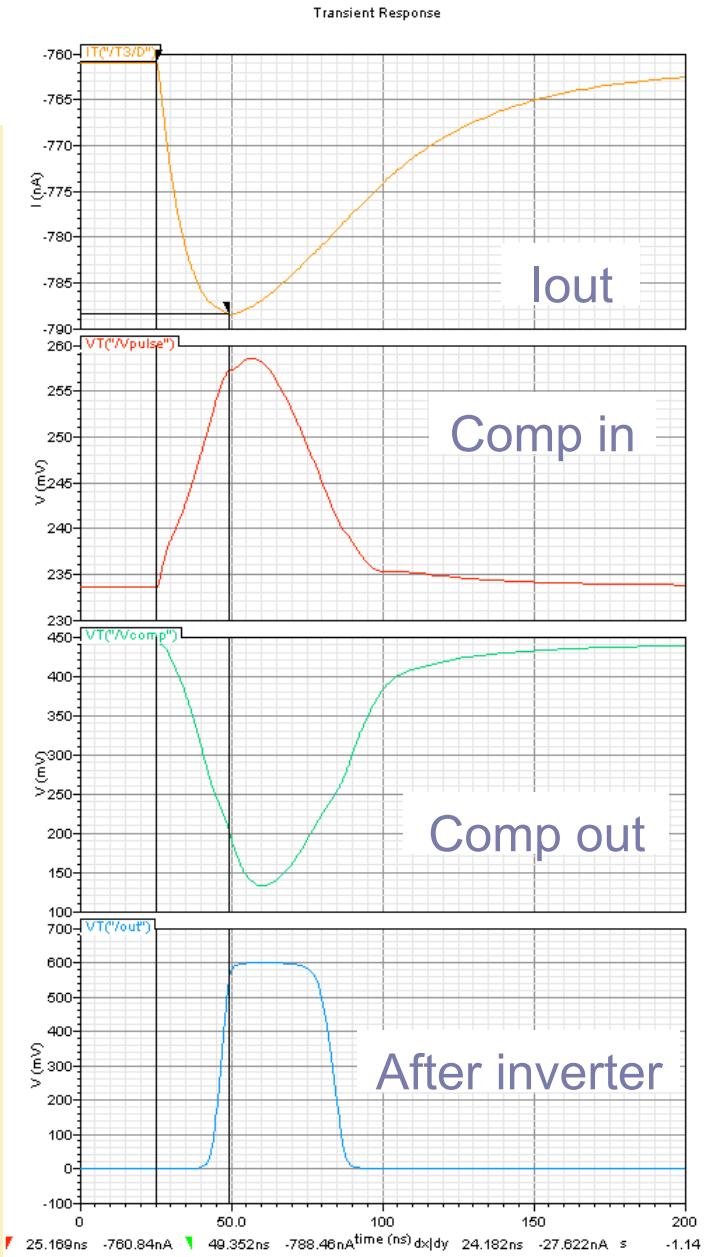
Front end for monolithic in 90nm



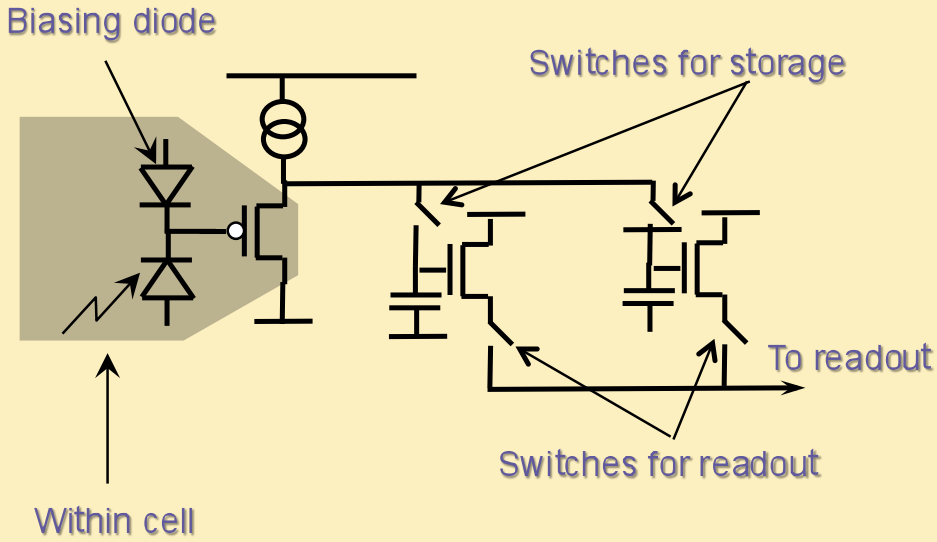
Simulations started:

~ 900 nA for integrated amplifier – shaper with comparator

Note: compared to current pixel detectors important savings in power, but less S/N (maybe some of this can be recovered, depends on Q/C finally achieved)



First readout scheme for testing (matrix 1 and 2)



① Can store analog value twice using external pulses, eg once after reset (bias diode can be replaced by reset transistor) and once a bit later. The difference between the two values is a measure of the signal collected in that time interval.

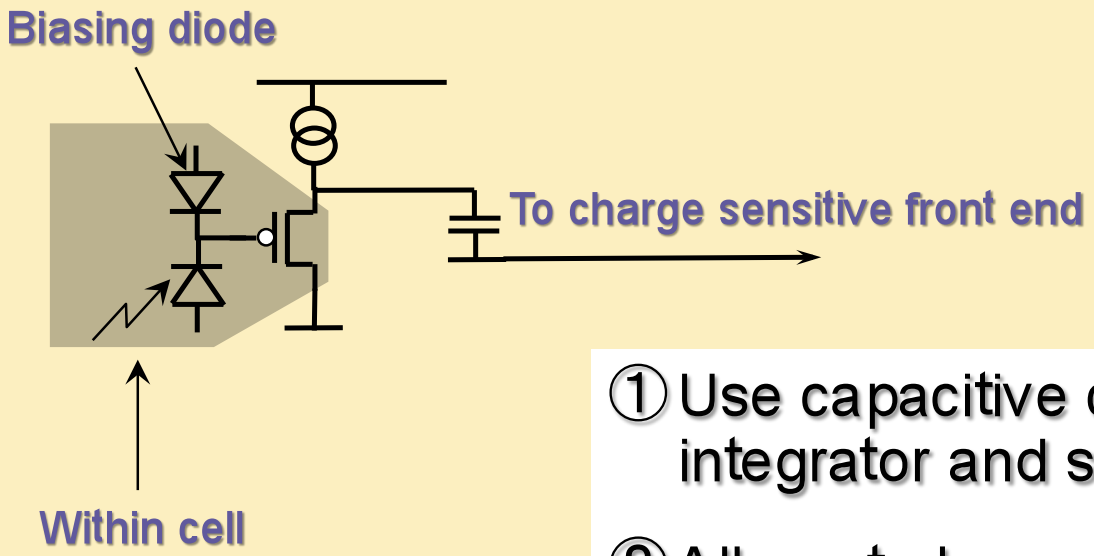
② This storing is done for all elements in the matrix in parallel.

③ Afterwards both values for all pixels are readout sequentially.

④ This mechanism allows to externally control the sensitive period independently of the readout.

⑤ **Readout a la 'MAPS' with storage to avoid loss of signal during readout**

Second readout scheme for testing (matrix 3 and 4)



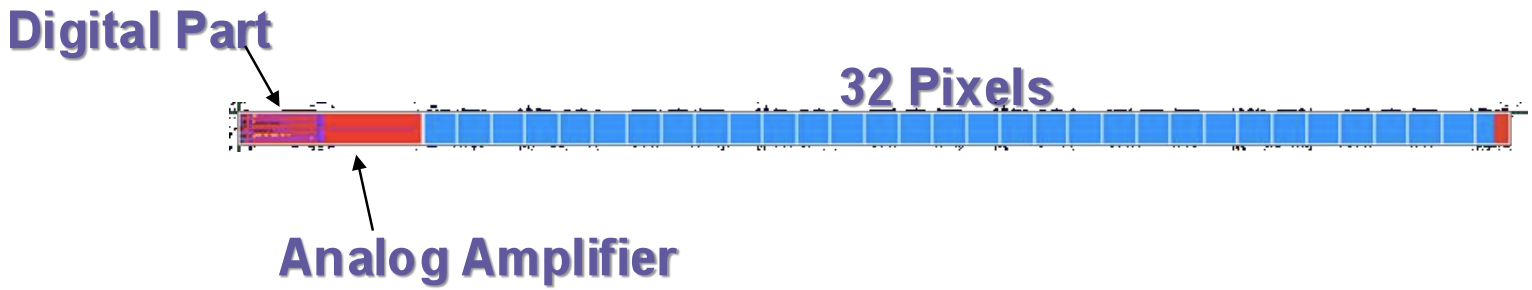
① Use capacitive coupling into a classical integrator and shaper

② Allows to be sensitive to sudden signals only.

③ Is relatively insensitive to leakage

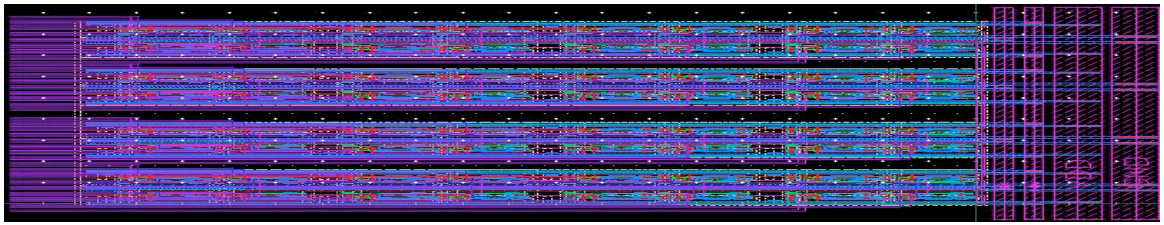
④ In final front end we also plan to filter, but more work is needed there

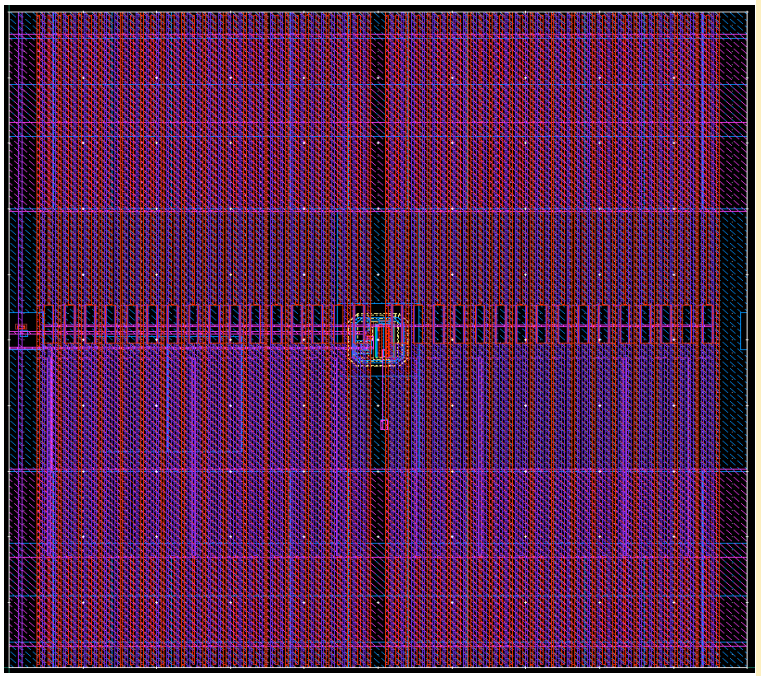
Matrix of 32x32 pixels – Pixel 50x50µm²



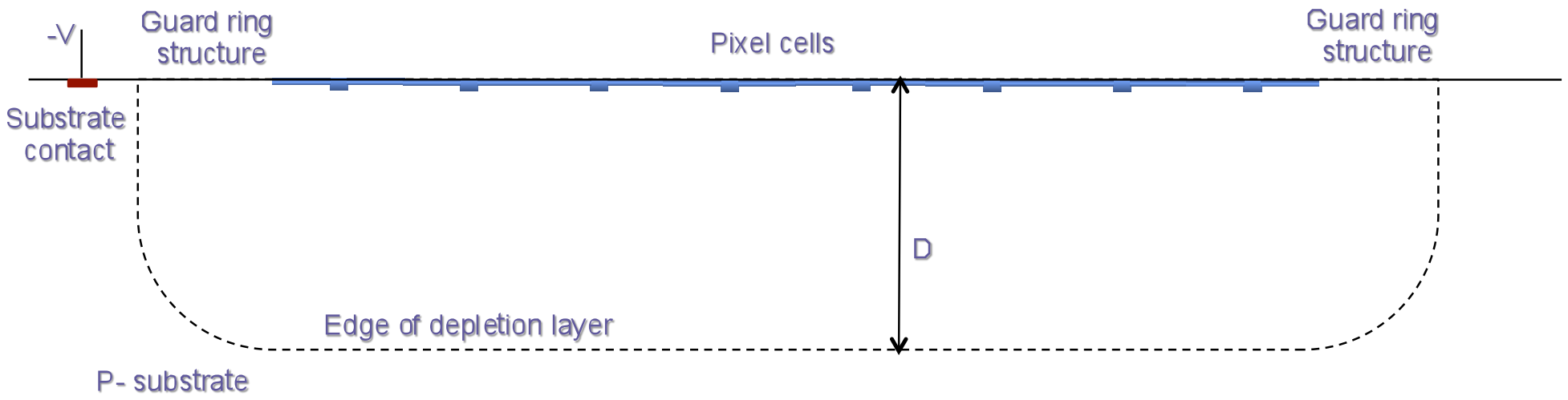
Pixel 50x50µm²

Digital part





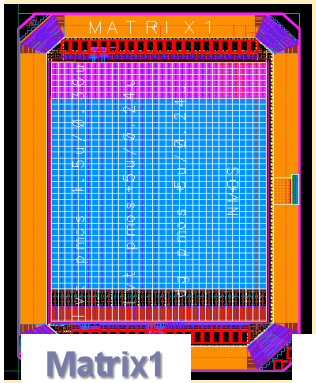
ElectroStatic Discharge (ESD) protection



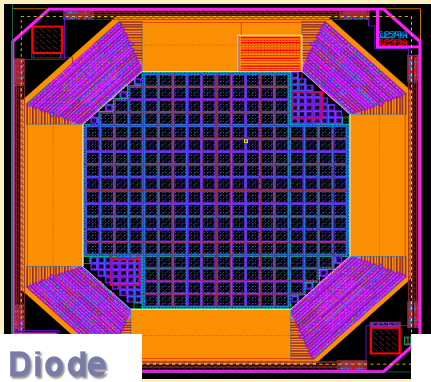
- Electrostatic Discharge is more and more important for very deep submicron CMOS due to the reduced oxide thickness. Extensive protection is needed.
- Normally protection structures are heavily connected to the substrate usually connected to GND (but here NOT) (there are some alternatives, triple well…).

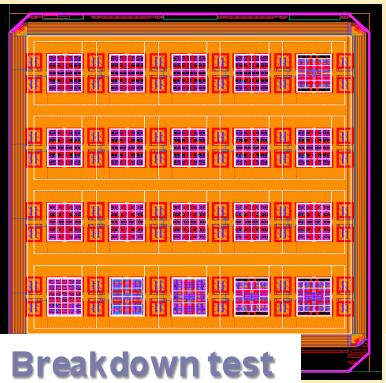
LePIX: SUBMISSION FOR FABRICATION

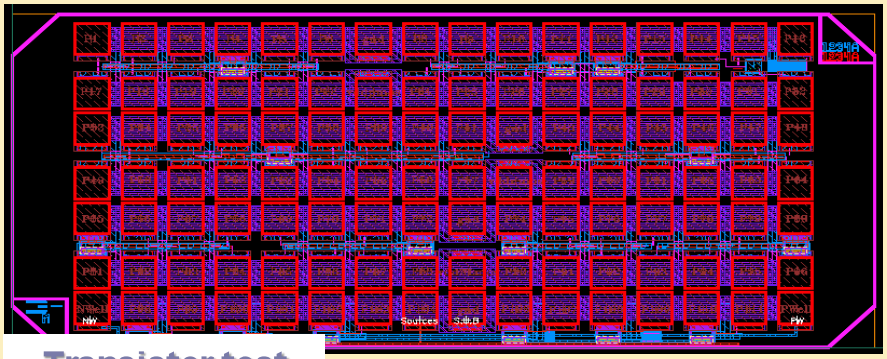
- Non-standard: ESD protection, special layers, mask generation, guard rings
- Received chips on standard substrate, put lot on high resistivity on hold
- 7 chips submitted :
  - 4 test matrices, 2 types of readout and 2 collection electrode sizes
  - 1 diode for radiation tolerance
  - 1 breakdown test structure
  - 1 transistor test: already submitted once in test submission



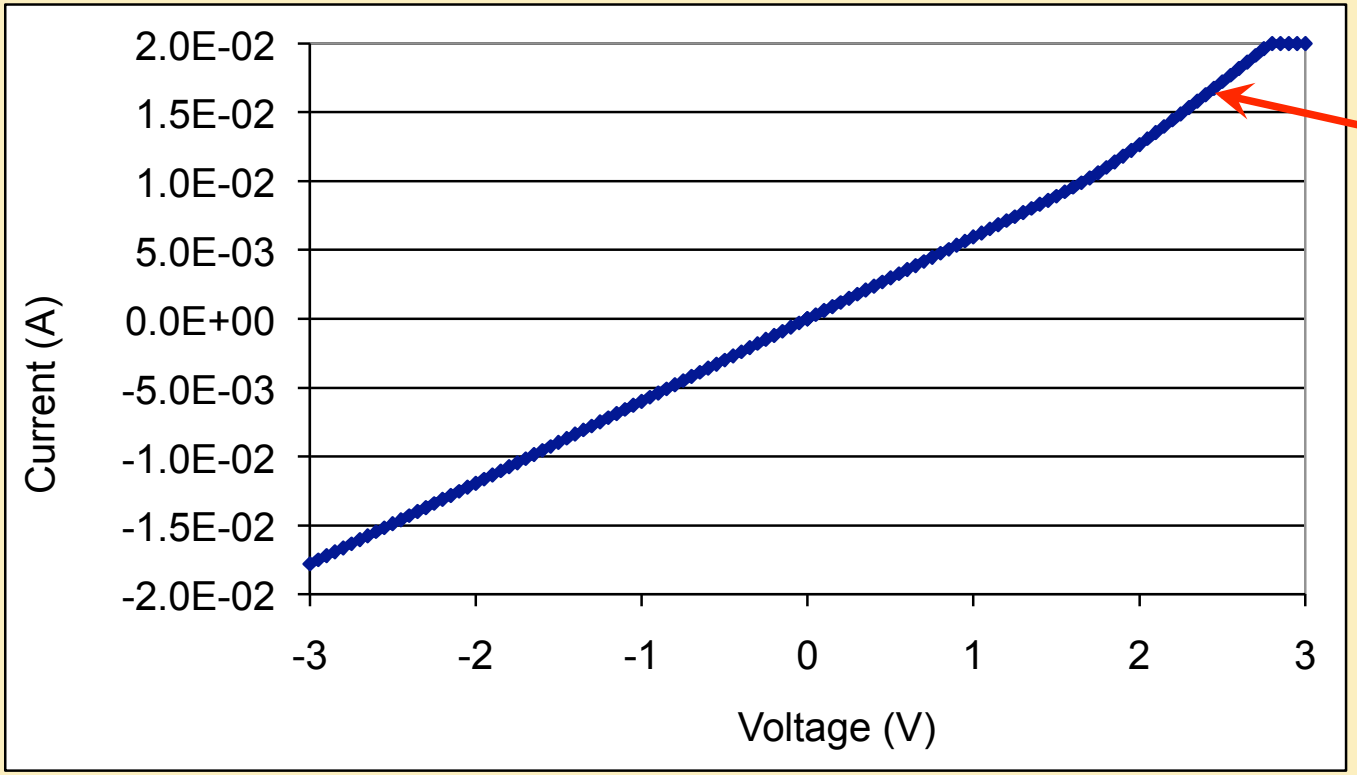
Matrix1


Diode


Breakdown test


Transistor test

The bad news: short due to mask generation issue



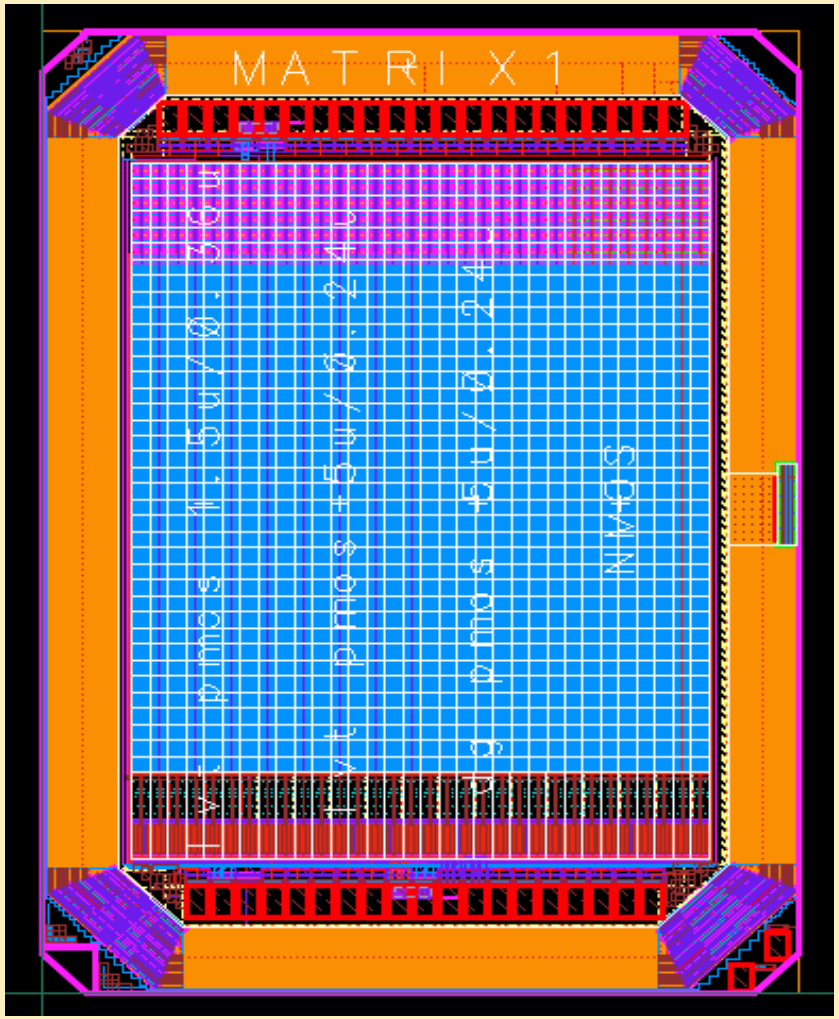
Forward 'diode'

The guard ring received p+ implant creating a short

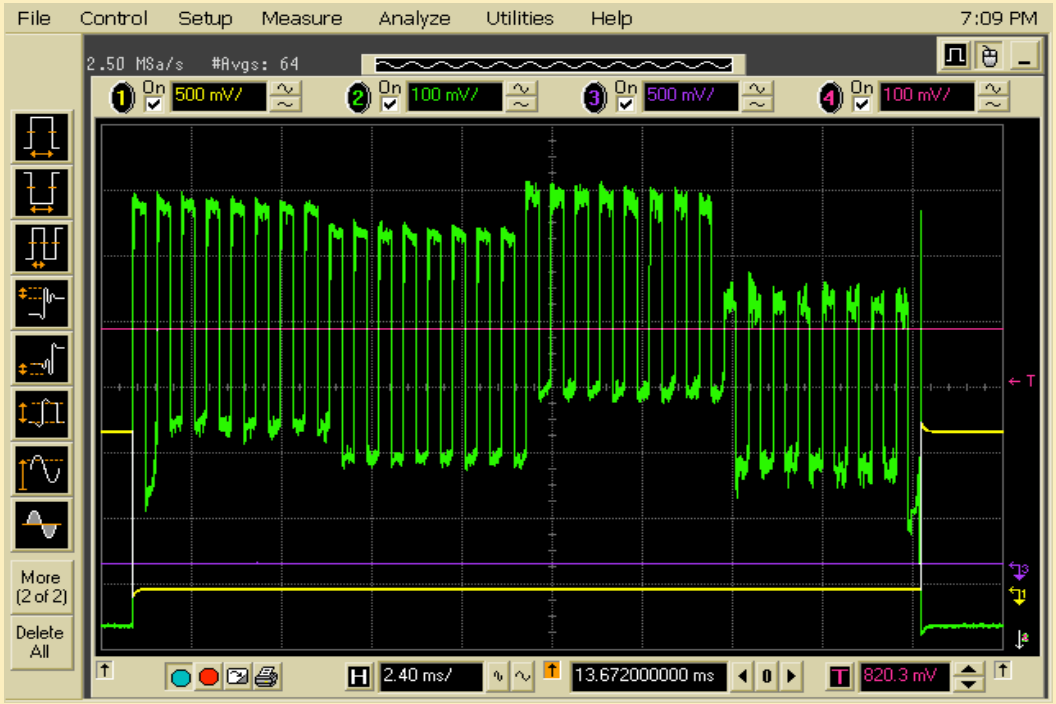
(which transforms to a ~80 ohm resistor due to series resistance)

SUBMISSION WITH CORRECTION IMMINENT

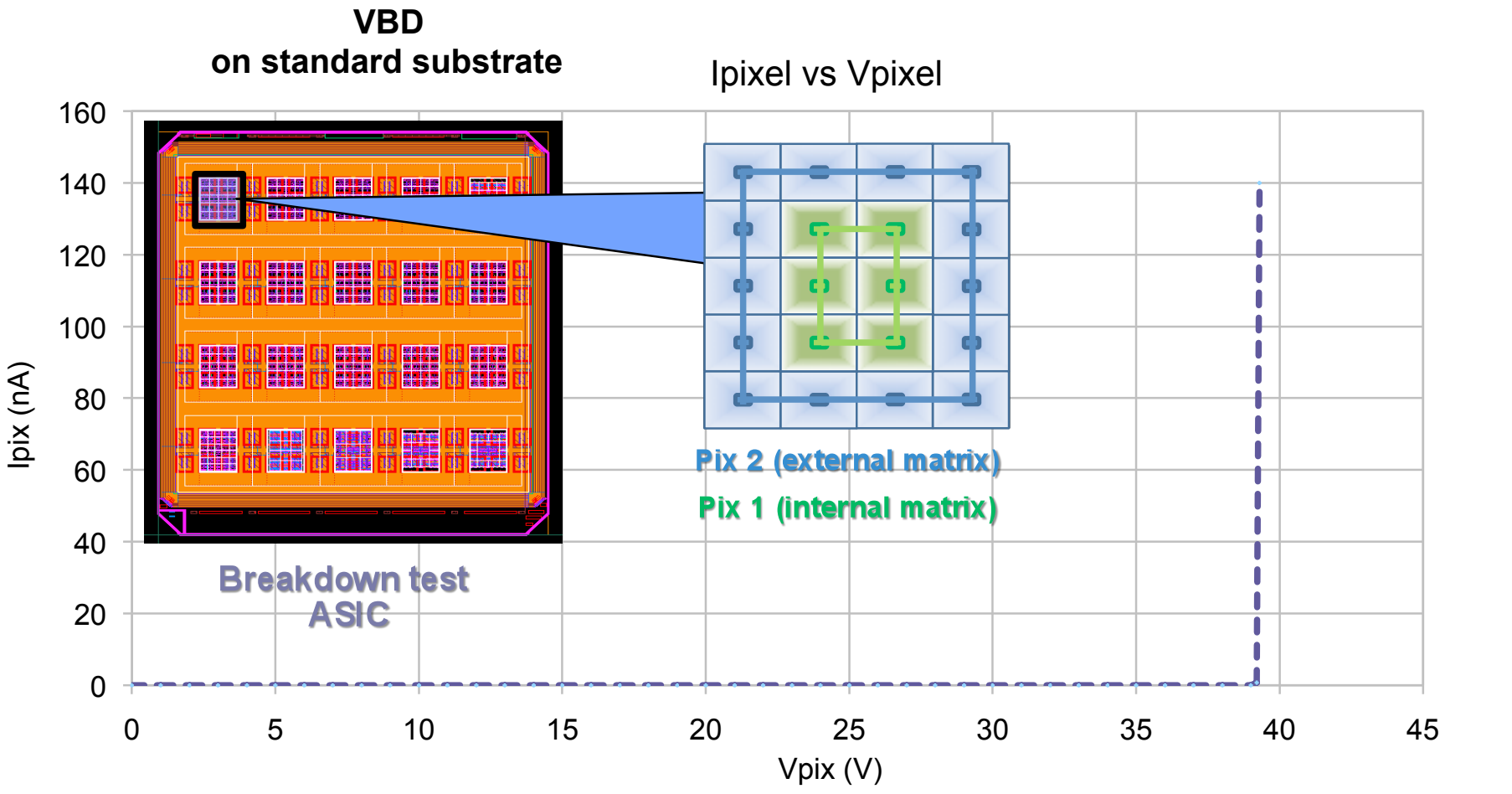
The good news: circuitry of first matrix 1 operational



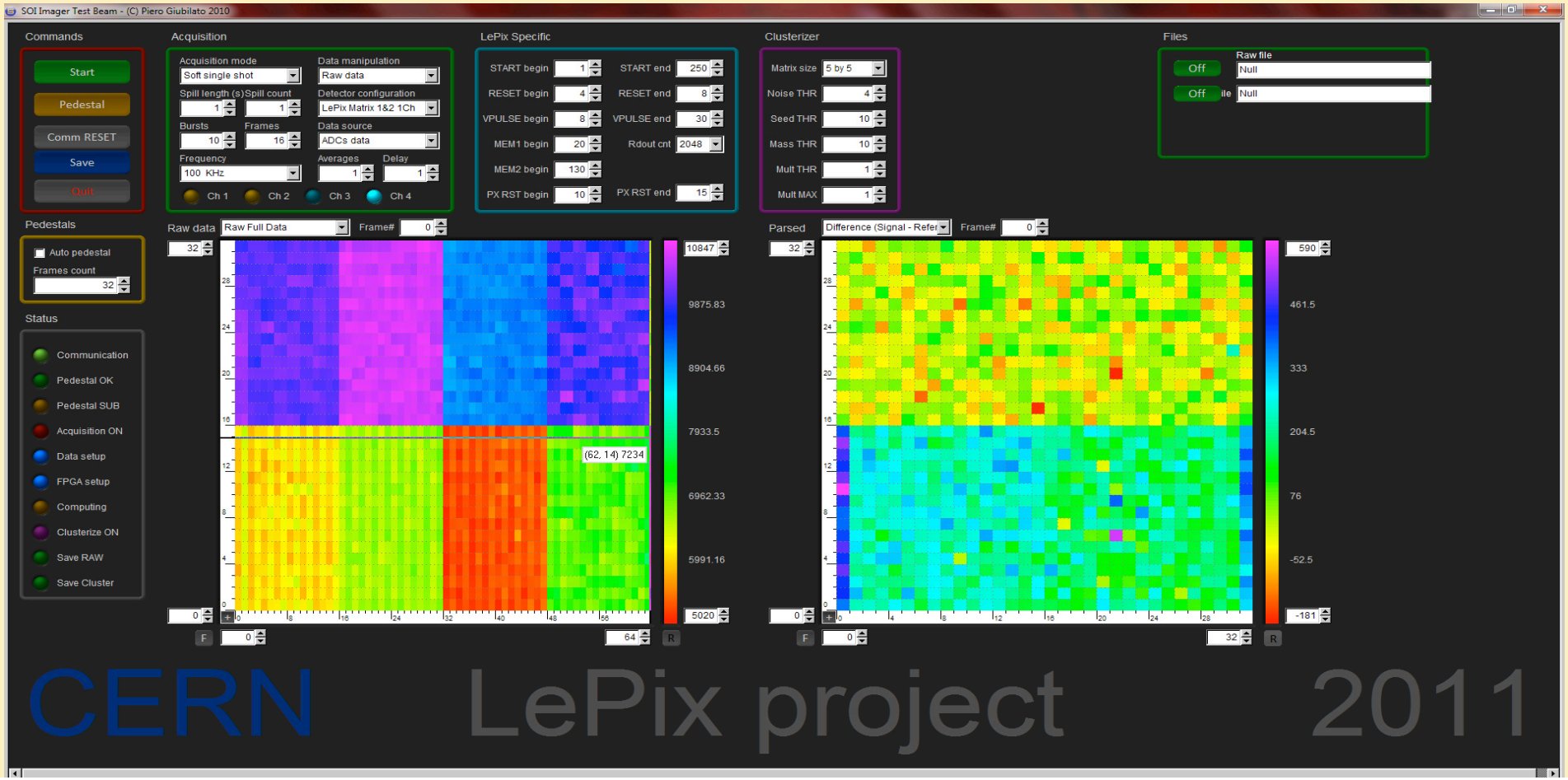
- 4 zones of 8 columns with different input transistor clearly visible
- Difference between active and diode reset



The good news : Breakdown > 30 V … on standard substrate, close to expected value for planar junction



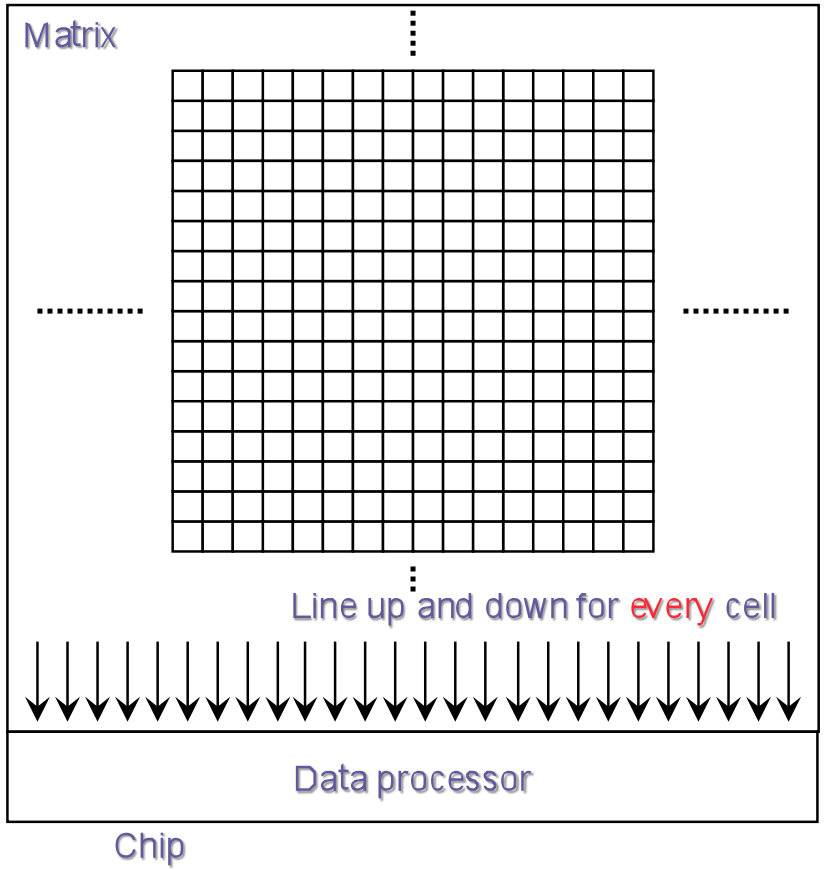
Test setup (P. Giubilato, D. Pantano (INFN Padova) et al)



Very promising, about to submit correction
Measurement setup prepared

- Motivation :
  - Impact of power consumption on material in high energy physics experiments
  - The importance of Q/C for power consumption
- Some examples of monolithic detectors
- Device design & device simulations
- Processing
- Monolithic detectors in deep submicron CMOS : example LePIX
  - Q/C and segmentation
  - Device design
  - Some (analog front end) readout circuits
  - Status of first prototype submission & measurement setup
- Digital part of the readout and power consumption
- Radiation tolerance

Save analog power, how about digital ?



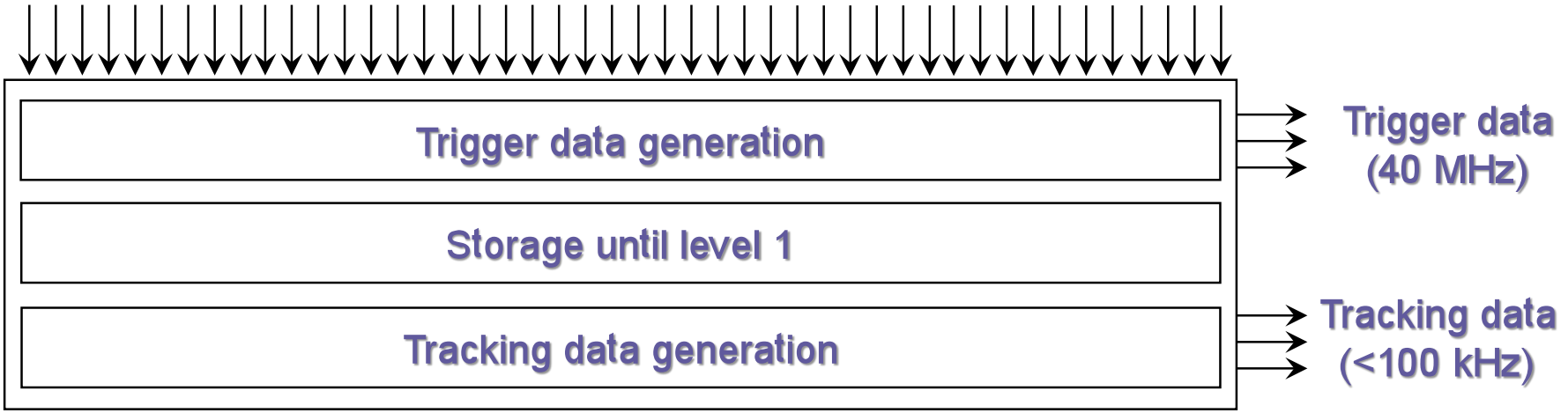
Challenge is efficient data processing at the edge of the chip and communication to the outside for trigger and tracking signals

Occupancy D. Abbaneo	Element 100x100 micron	Superelement 256x100x100 micron
PXB Layer 1	5.56E-03	1.42E+00
PXB Layer 2	2.41E-03	6.16E-01
PXB Layer 3	1.39E-03	3.55E-01
TIB Layer 1 int	3.39E-04	8.69E-02
TIB Layer 1 ext	2.82E-04	7.23E-02
TIB Layer 2 int	2.18E-04	5.58E-02
TIB Layer 2 ext	1.88E-04	4.82E-02
TIB Layer 3 int	1.28E-04	3.29E-02
TIB Layer 3 ext	1.14E-04	2.91E-02
TIB Layer 4 int	9.32E-05	2.39E-02
TIB Layer 4 ext	8.55E-05	2.19E-02
TOB Layer 1	5.94E-05	1.52E-02
TOB Layer 2	4.58E-05	1.17E-02
TOB Layer 3	3.54E-05	9.06E-03
TOB Layer 4	2.78E-05	7.11E-03
TOB Layer 5	2.57E-05	6.58E-03
TOB Layer 6	1.97E-05	5.05E-03

In the following some ideas on architecture – not final at all, would like to point out the thinking, do not want to give impression things are fully solved…

ALICE: inner layer 200 tracks/sq cm, or 0.02 for 100x100 micron…

Data processor



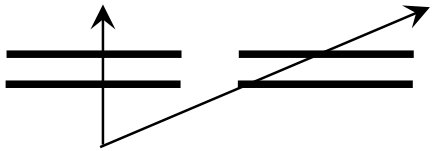
- Advantages of having all bits at the edge:
  - Can handle them in a programmable way
    - Trigger: from 'fast or', could also have fast multiplicity, topological …
  - Do not need to distribute the clock to all elements (cannot would take a good fraction of 10 mW/sq cm), save power by not doing so

Strategy for trigger: example of compression of data, folding

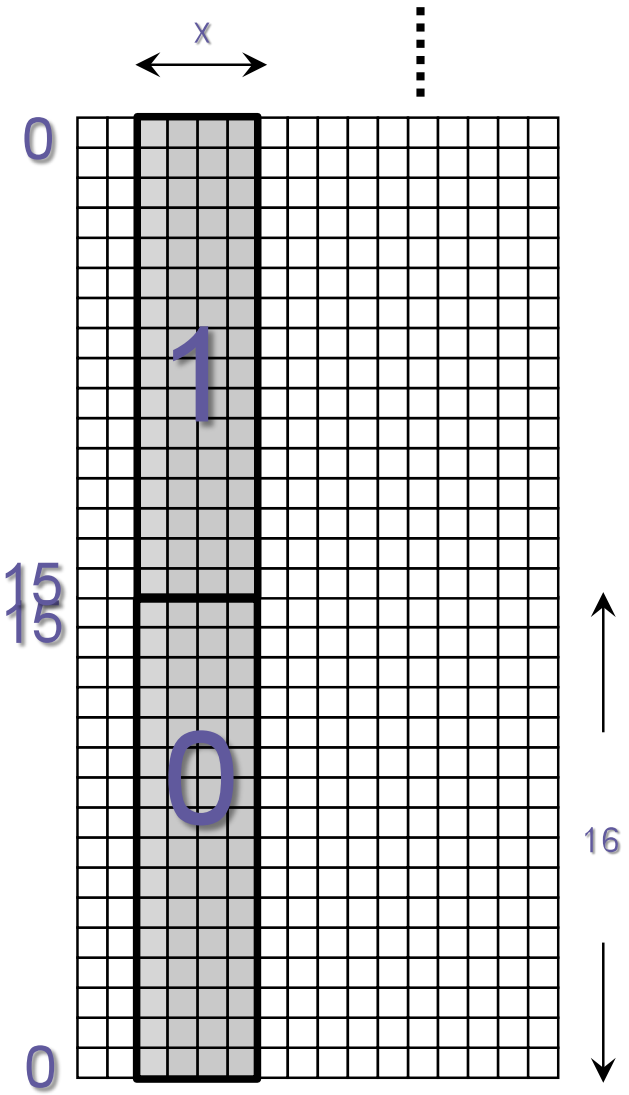
- Idea is to reduce data/number of outputs without big increase in activity in the bits while at the same time being robust in situtations of charge sharing/multiple hits
- Make column wider so that average occupancy in column =< 0.25, TOB6 128 wide, TOB1 16, TIB4 8, TIB1 2 , so in general x
- Do folding 256 -> 16+16 coordinates = per supercolumn 32*40Mbit/s = 1.28 Gb/s
- If 8 bit address, for one hit (no charge sharing, 4x less data, but no tolerance for charge sharing and double hits.
- Power: if local transmission in CMOS @ 40 MHz

Changing bits/hit*0.25*40 MHz*2pF < 40 uW

- Need programmable shift :



Stitching

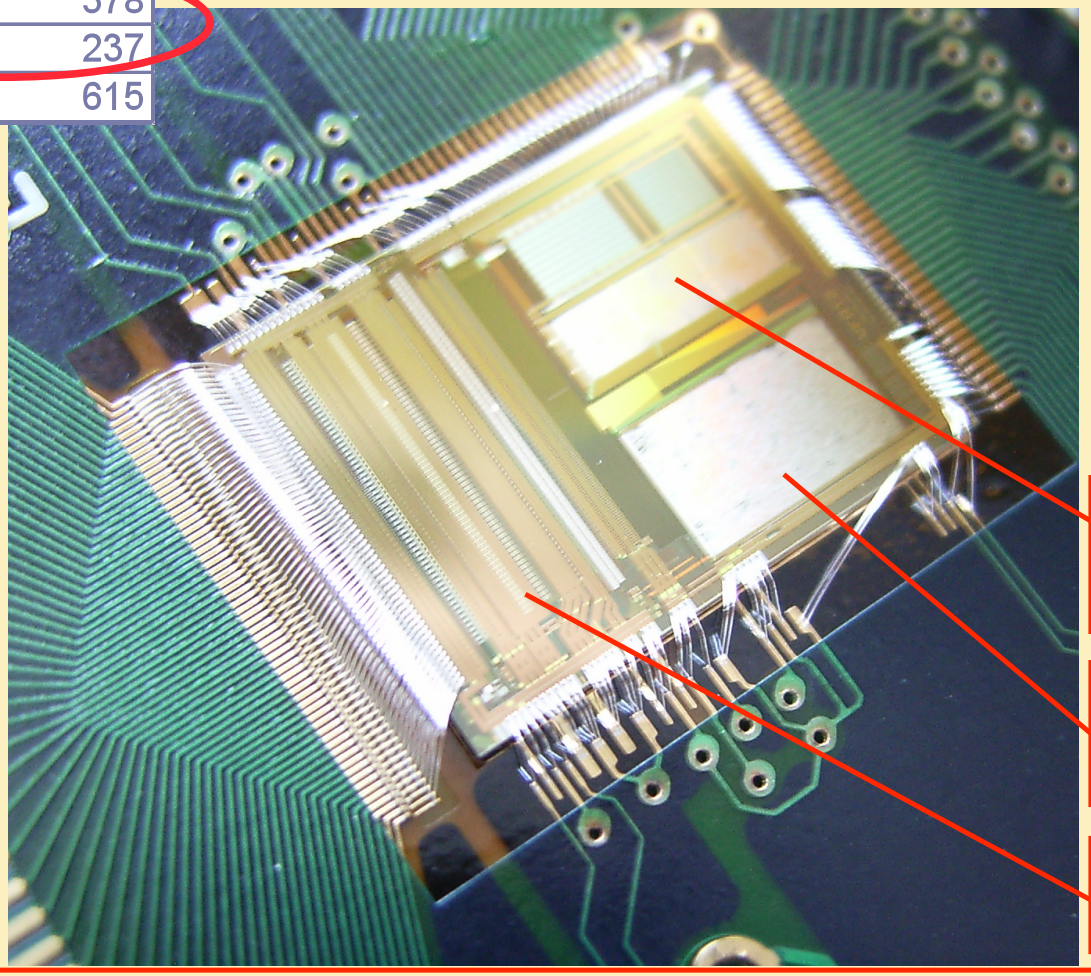


Digital power consumption: TOTEM VFAT chip

VFAT power consumption			
(mW)	Sleep	Run (nominal)	Run (max)
Analog	33	378	378
Digital	135	194	237
Total	168	572	615

VFAT sends digital data to GOH hybrid, which serializes and optically transmits this data

P. Aspell et al. TWEPP 2007



Designers :
Paul Aspell
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Herve Mugnier
Jan Kaplon
Kostas Kloukinas
Pierre Chalmet

CERN C4i

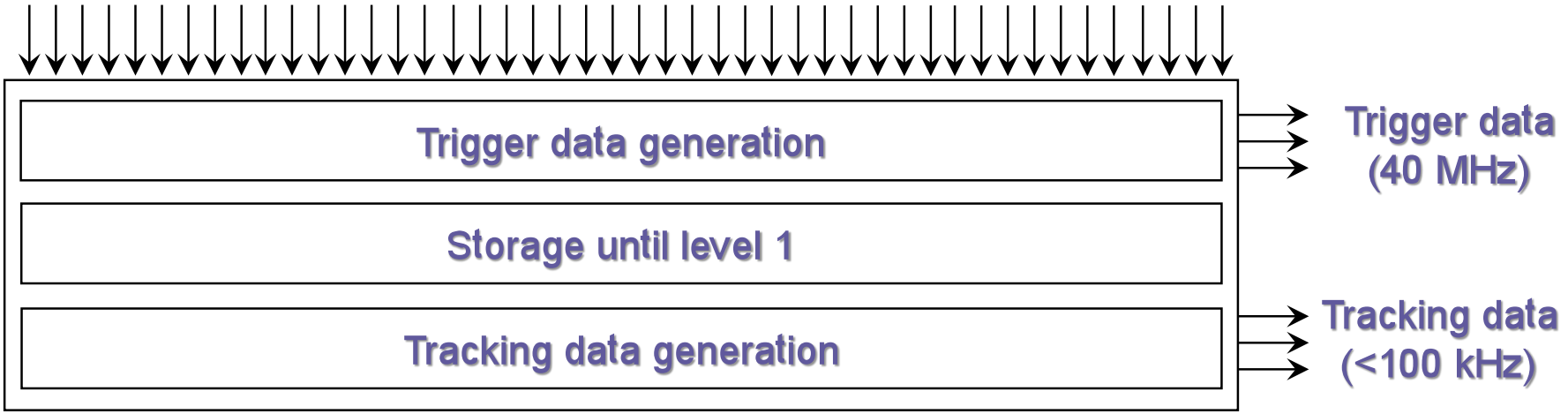
Data treatment and memories

Slow Control Registers

Frontend

128 channels of tracking front end with digital storage and data transmission
8 programmable trigger outputs, designed for radiation tolerance

Storage until level 1



- Full memory for storage until level 1?
  - In principle space not prohibitive
  - In VFAT (TOTEM) ~2 mW/channel for this (including many whistles and bells)
  - Gain in technology max 20x, need much better than this:
- Need less than 1uW/channel (= 10 mW/sq cm)
  - Need encoding before writing into memory
  - Could go to full address generation
  - Can ‘or’ channels, so reduce apparent segmentation

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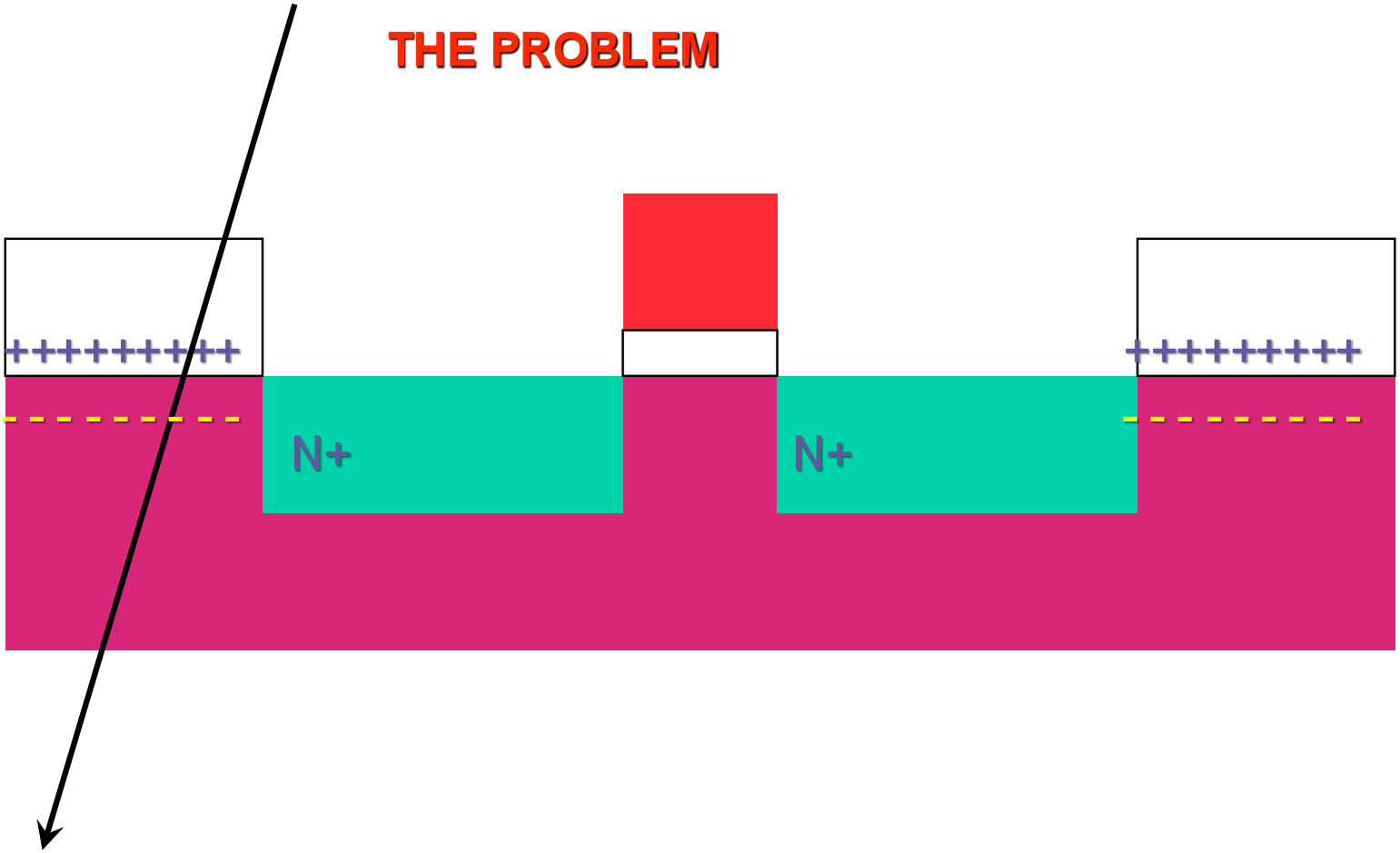
NMOS TRANSISTOR LEAKAGE

THE PROBLEM



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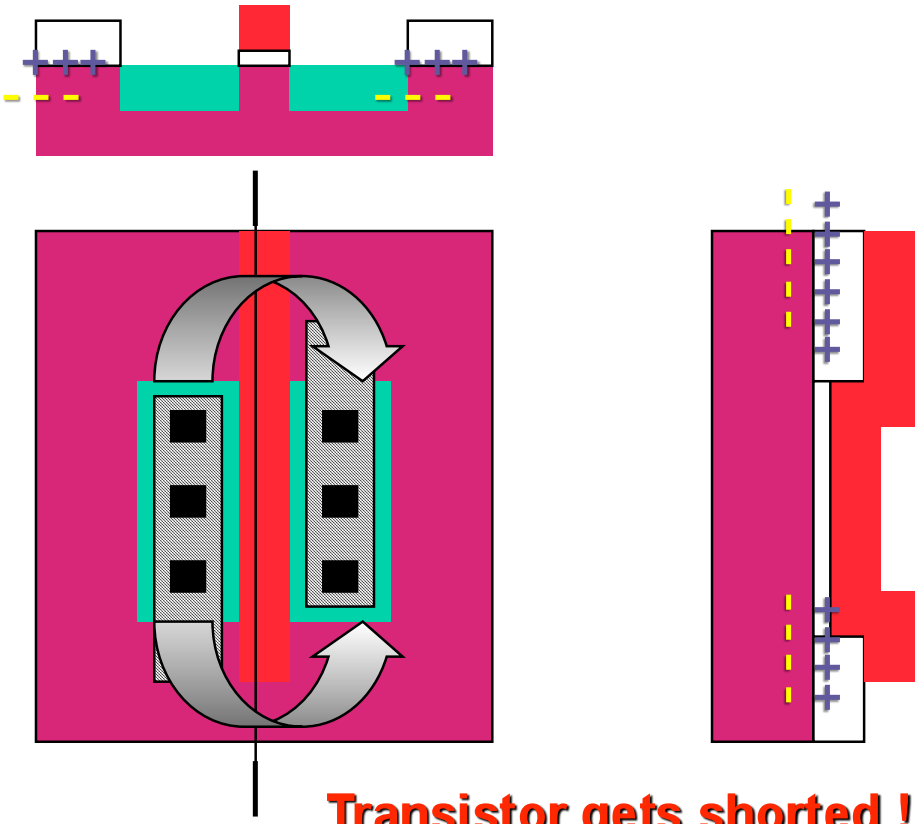
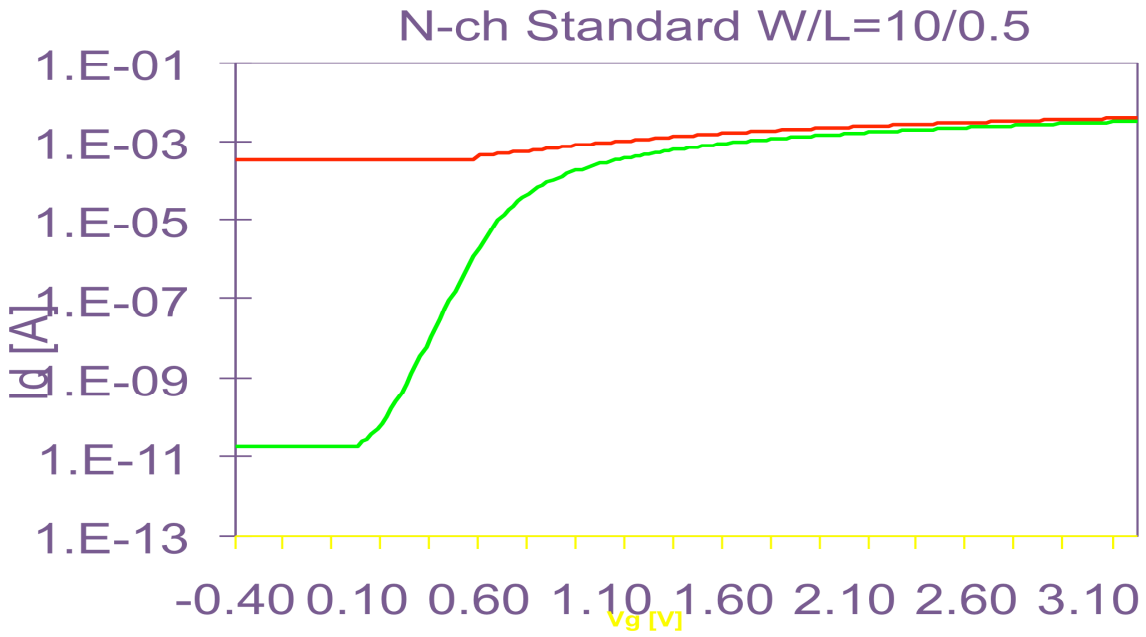


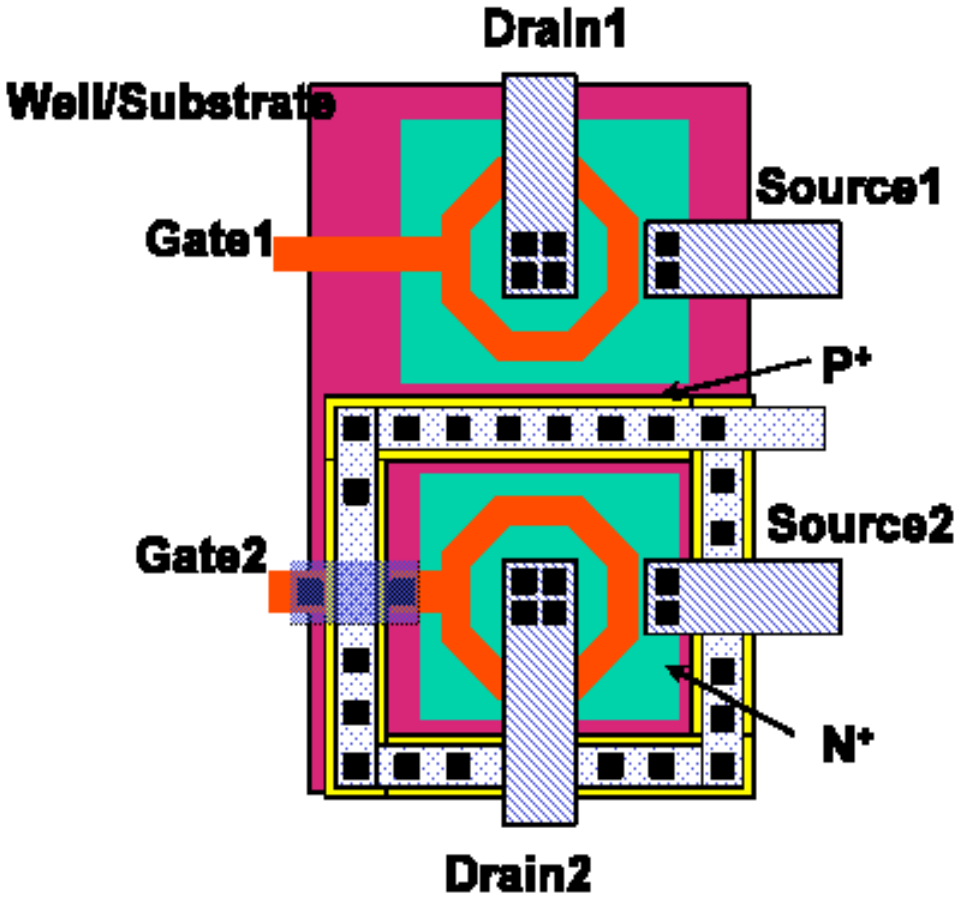
Transistor gets shorted !

Total ionizing irradiation dose problem in commercial CMOS

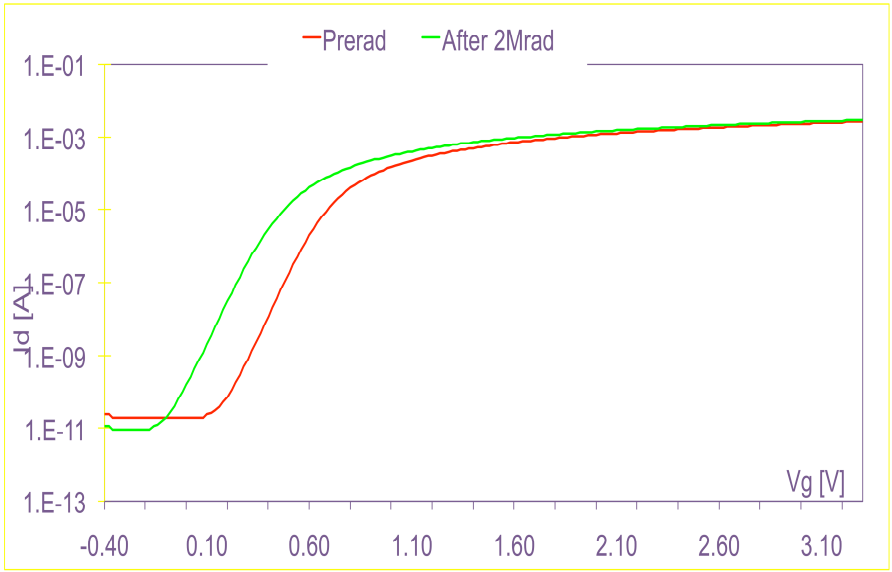
- Vt - shift
- weak inversion slope change
- LEAKAGE in NMOS transistors



Gate enclosed NMOS devices

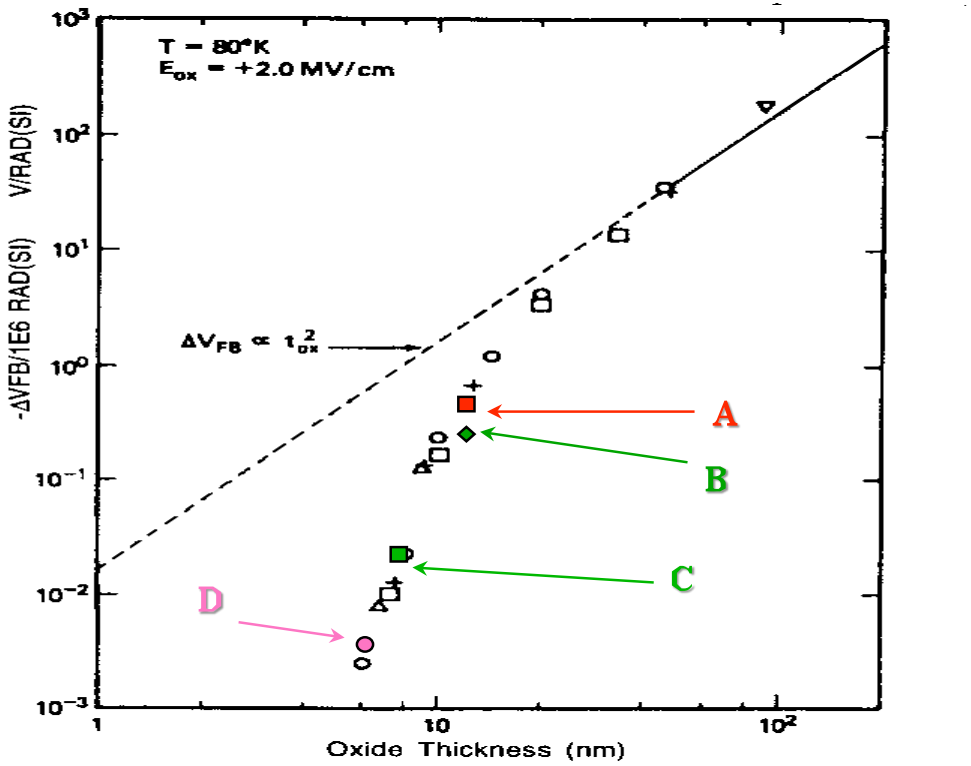


- Special layout eliminates radiation induced leakage
- modelling issue
- density impact but much finer linewidth
- CAD tools



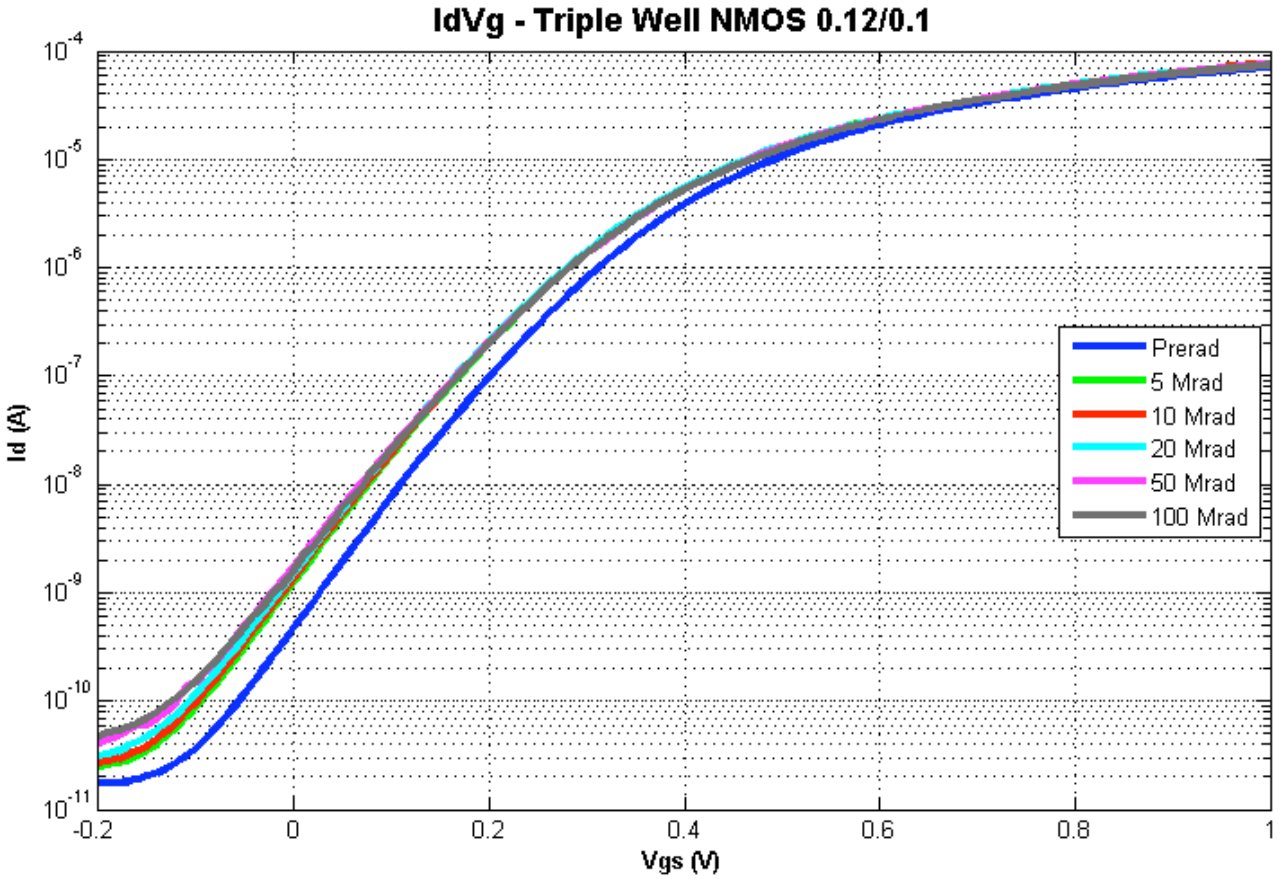
MOS Flatband voltage shift versus gate oxide thickness after 1MRad(Si) @ 80°K

- Tunneling to eliminate trapped charge in thin oxides
- DVT ~ $1/tox^2$ for tox > 10nm
- DVT ~ $1/tox^3$ for tox < 10 nm

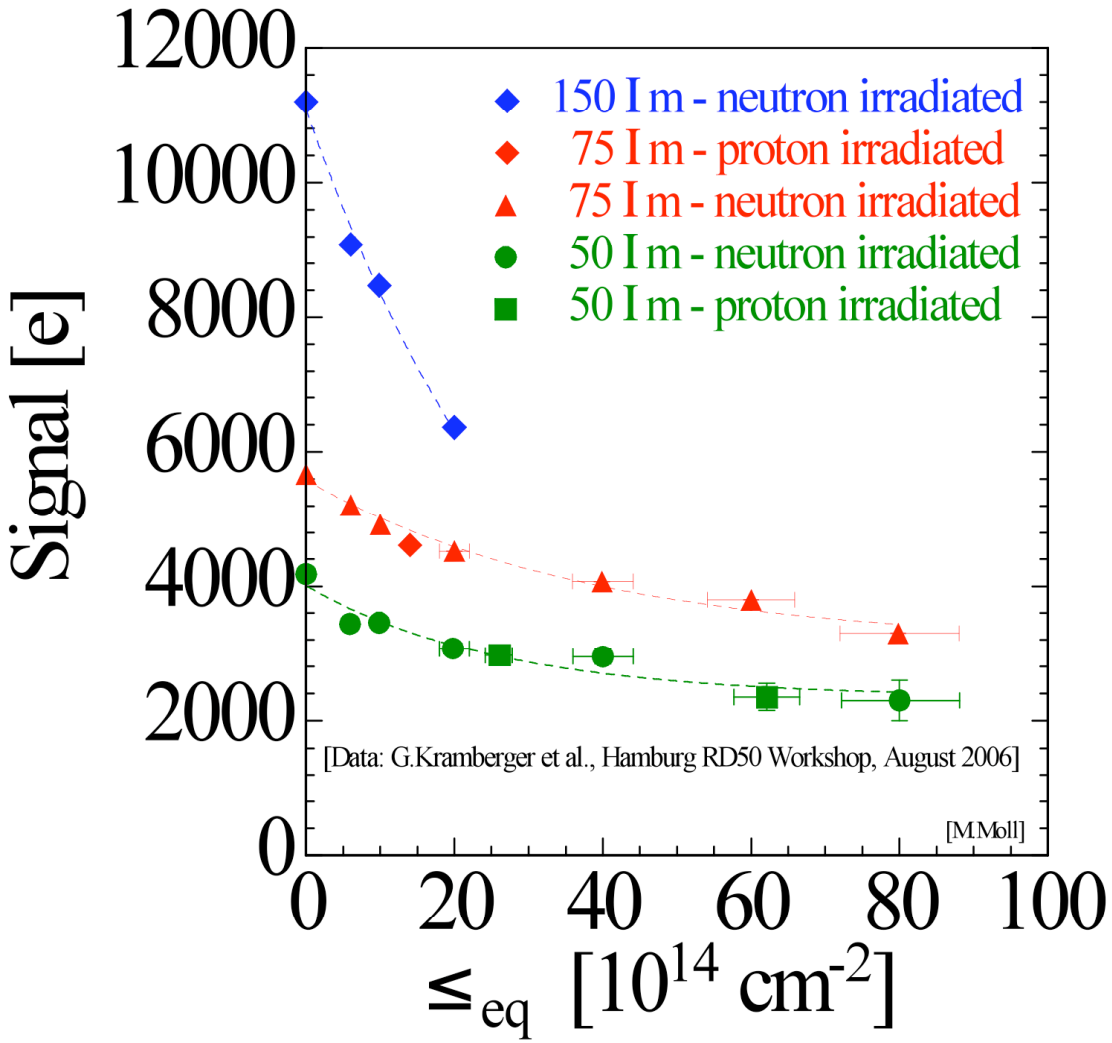


After N.S. Saks, M.G. Ancona, and J.A. Modolo, IEEE Trans.Nucl.Sci., Vol. NS-31 (1984) 1249

- Enclosed layout might no longer be necessary…



Example in 90nm no enclosed layout (measurements L. Pierobon)



- Charge collection by drift essential (see MAPS in the beginning)

Data in the plot (N-type)

- Doping of 50 and 75 micron thick material is 50 Ωcm
- Doping of 150 micron thick epi is 400 Ωcm
- Higher resistivity clearly degrades faster
- Therefore expect better radiation tolerance but need more measurements

Conclusions (I)

- In general lower power will be the key to reduce the material
- Monolithic offers several advantages, including low capacitance offering very favorable analog power consumption for a given S/N
- Several aspects : device design, processing, circuit design
- Availability of more lightly doped substrates opens perspective for monolithic detectors in 90nm deep submicron CMOS. LePIX project is trying to exploit this
- Analog power can be reduced by segmentation and device design
- Need work on digital (and the analog !), would like to exploit having all bits at the bottom of the matrix
- Is very much work in progress, need to implement some corrections and resubmit, looks quite promising.

Conclusions II

- Radiation tolerance:
  - going to very deep submicron is an advantage, may not need special layout
  - need charge collection by drift in the detector, so need bias to create an electric field

THANK YOU