Preparatory meeting for

LAPPD Beam Test in October 2022 at CERN

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Motivation

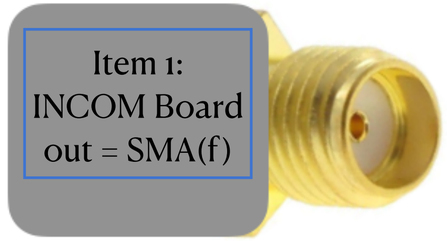
- **Identify the logistics**
- **Procure them**

Considering to readout 32 channels of the LAPPD

Scaling up to 64 channels would be considered in the next phase,

taking into account the non-magnetic materials for the cables/connecters.

Item 1:
INCOM Board
out = SMA(f)

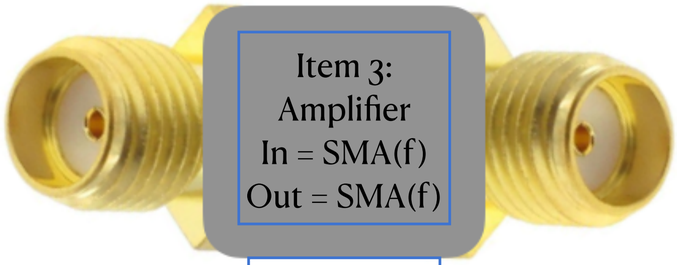


32+32 = 64 channels

Item 2:
SMA(m)-SMA(m)
Cable = 0.5 m

Item 2 and 4:
We have = 43
We need = 64
need to oder = 21

Ordered 30 of them



Item 3:
Amplifier
In = SMA(f)
Out = SMA(f)

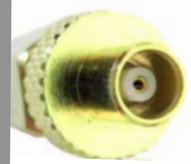
Item 3:
We have = x
We need = x

Item 4:
SMA(m)-SMA(m)
Cable = 0.5 m

Item 5:
We have = 68
We need = 64

Item 5:
In = SMA(f)
Out = SMA(f)
Connector = feedthrough

Item 8:
VME
In = MCX(f)

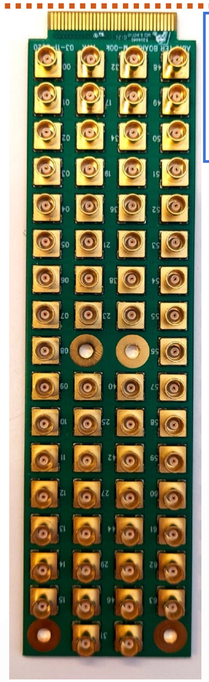


Item 7:
MCX(m) - MCX(m)
Cable = 1.5 m

Item 7:
We have = 40
We need = 32

Item 6:
SMA(m)-MCX(f)
Connector/Adapter
(because we have many of the item 7)

Item 6:
We have = 52
We need = 32



Item 0:
BNL Board
Out = MCX(f)

Item 1:
Cable-Adapter
In = MCX(m)
Out = SMA(f)

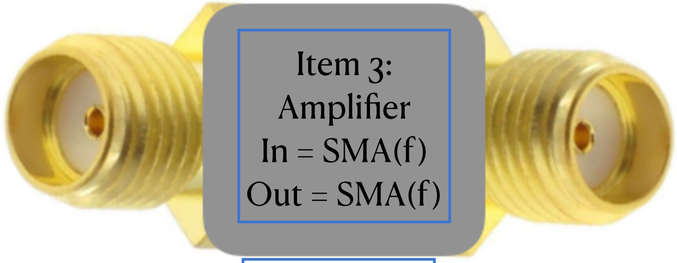
Item 1:
We have = 3
We need = 32
need to oder = 29

Ordered 35 of them

Item 2:
SMA(m)-SMA(m)
Cable = 0.5 m

Item 2 and 4:
We have = 43
We need = 64
need to oder = 21

Ordered 30 of them



Item 3:
Amplifier
In = SMA(f)
Out = SMA(f)

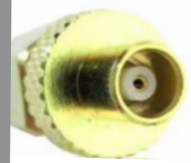
Item 3:
We have = x
We need = x

Item 4:
SMA(m)-SMA(m)
Cable = 0.5 m

Item 5:
We have = 68
We need = 64

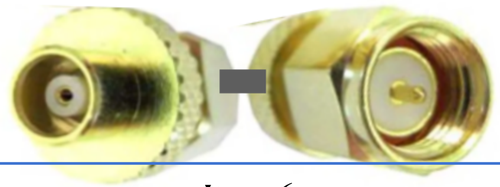
Item 5:
In = SMA(f)
Out = SMA(f)
Connector = feedthrough

Item 8:
VME
In = MCX(f)



Item 7:
MCX(m) - MCX(m)
Cable = 1.5 m

Item 7:
We have = 40
We need = 32



Item 6:
SMA(m)-MCX(f)
Connector/Adapter
(because we have many of the item 7)

Item 6:
We have = 52
We need = 32

Calibration of the DRS4 chip on the CAEN V1742 Board

A guidline:

First report on LAPPD tests

Federico Betti, Fabio Ferrari,
Stefano Perazzini, Vincenzo Vagnoni

INFN Bologna

18 September 2020

Domino Ring Sampler (DRS) 4 chip:

- max 5 GS/s (=200 ps)
- can readout 32 input channels from the LAPPD
- 1024 capacitor cells per channel
- full acquisition window of 204.8 ns

Calibration of the DRS4 chip on the CAEN V1742 Board

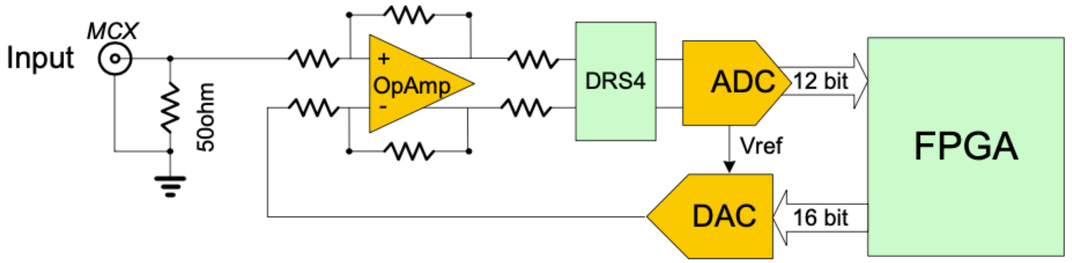
- **Voltage Calibration**
- **Time Calibration**

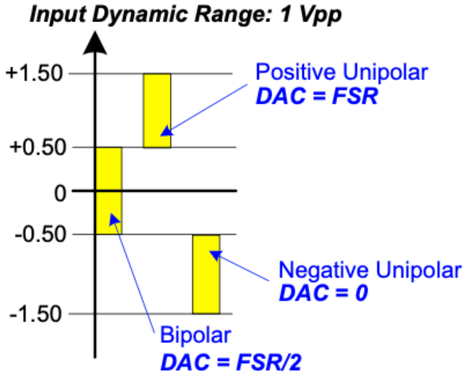
I can share Vincenzo's slides.

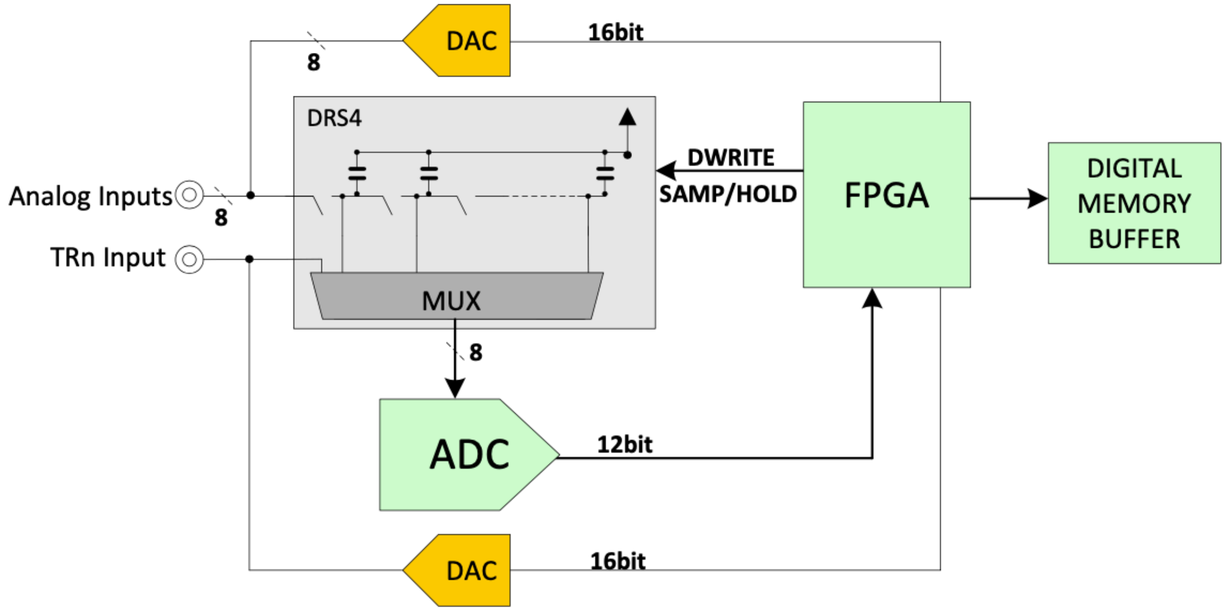
We have some questions

conceptual : what are actually these cells?

some technical: tools, software needed ?


Input
MCX
50ohm
+
OpAmp
-
DRS4
ADC
12 bit
Vref
DAC
16 bit
FPGA


Input Dynamic Range: 1 Vpp
+1.50
+0.50
0
-0.50
-1.50
Positive Unipolar
DAC = FSR
Negative Unipolar
DAC = 0
Bipolar
DAC = FSR/2


DAC
16bit
8
DRS4
DWRITE
SAMP/HOLD
FPGA
DIGITAL
MEMORY
BUFFER
Analog Inputs
8
TRn Input
MUX
8
ADC
12bit
DAC
16bit

Thank you!

Comments/Questions?