Stato produzone e tests FE-I4

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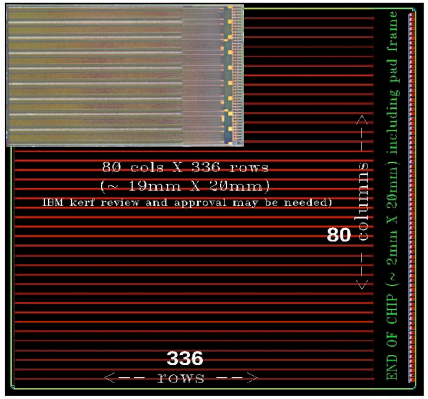
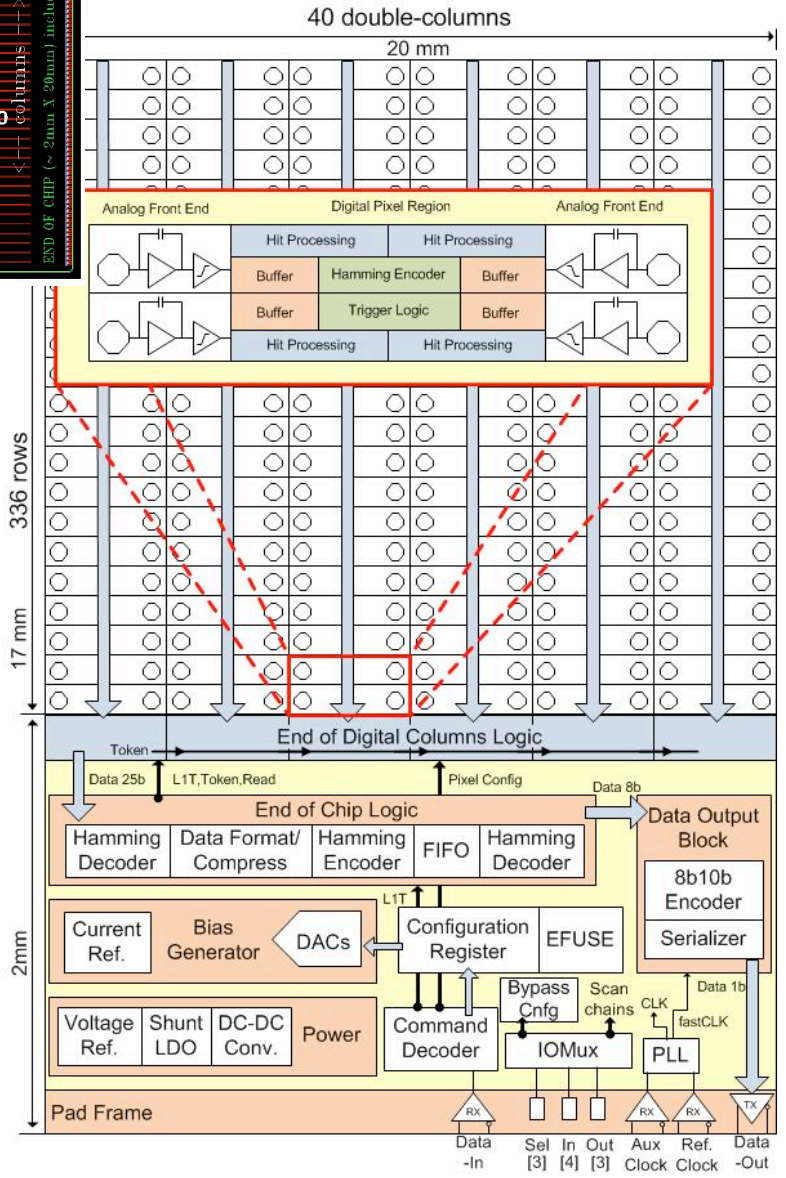
FE-I4

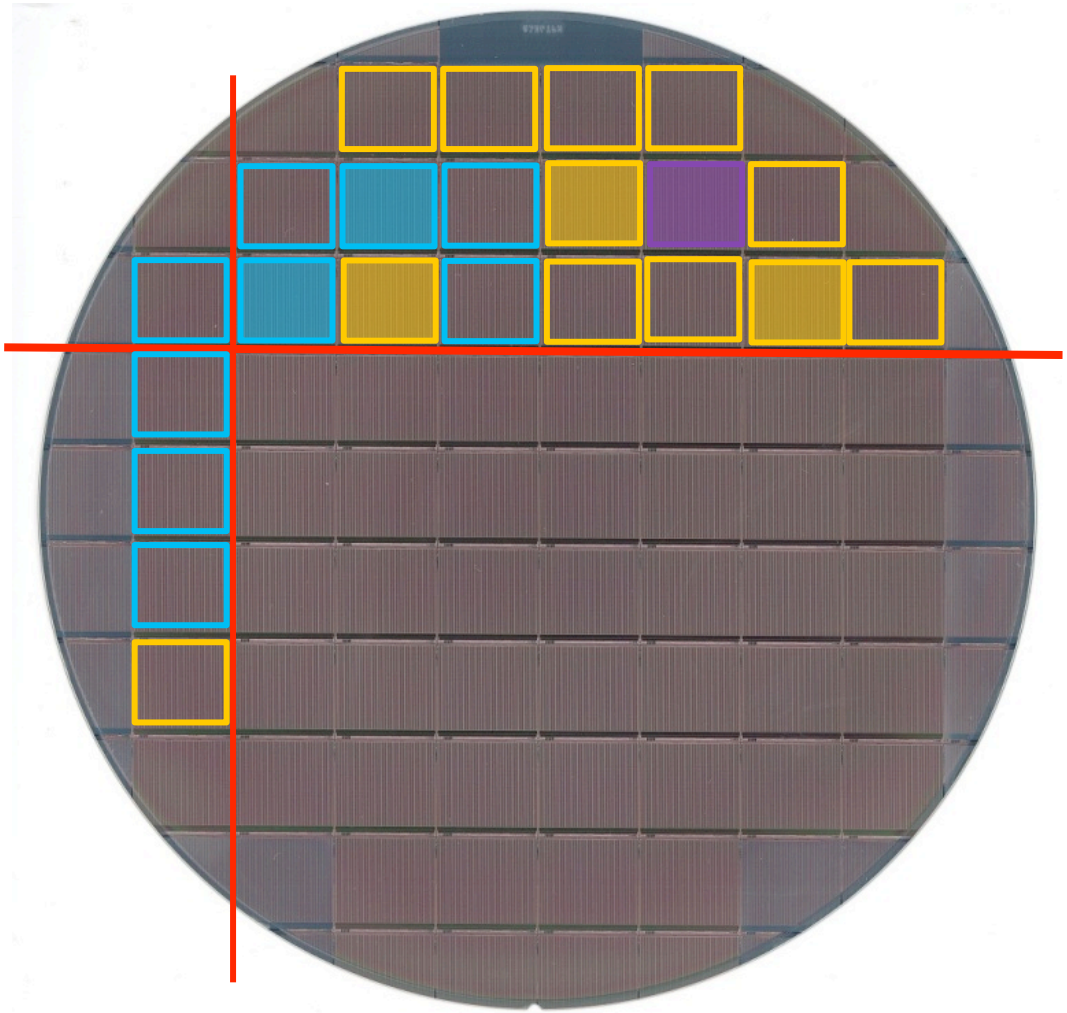


- ~6 times size of FE-I3
- Pixel size 50 x 250 µm
- 26.880 pixels
- 336 rows, organized in 40 DCs
- Readout organized in four pixel regions, hits buffered at pixel level until LV1-trigger
  → cope high occupancies
- Global EoDCL, EoCHL, Data Output Block
- Two configuration modes:
  - CMD decoder configuration
  - bypass configuration

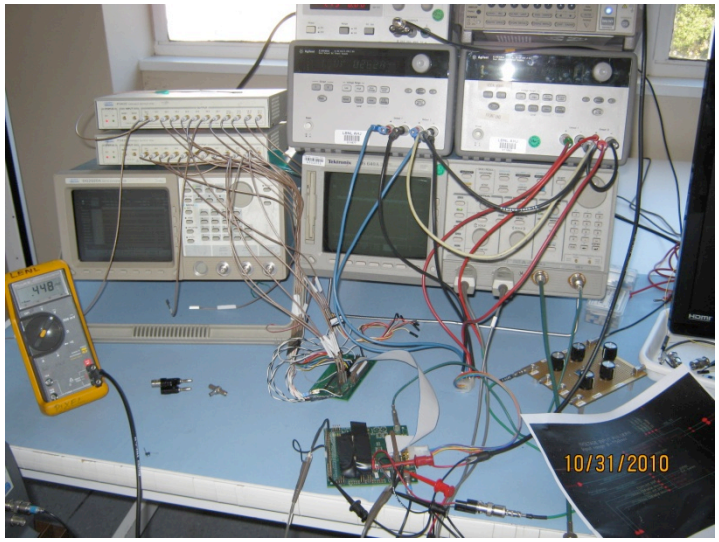


1st wafer diced

- 1st wafer was diced at 11th of october at LBNL.
- 22 single chips, 6 mounted on SCC
  - Chips at LBNL
  - Chips at Bonn
  - Chip at SLAC
  - Cut lines
- So far all 6 chips working
  - no detailed tests done on all

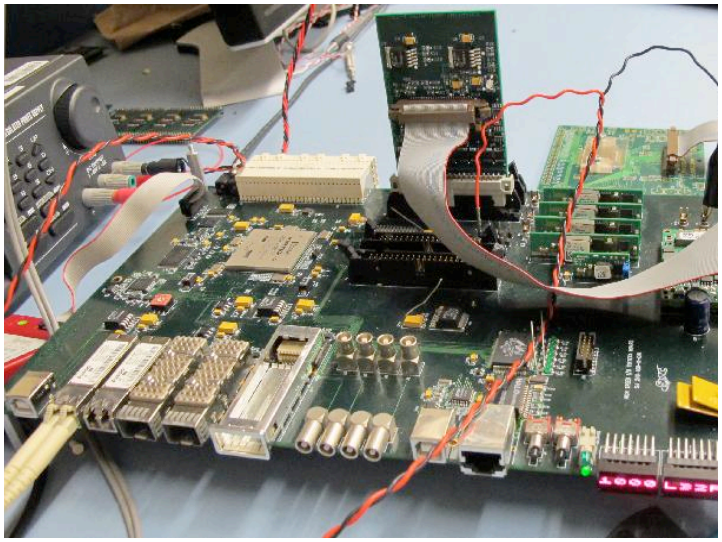


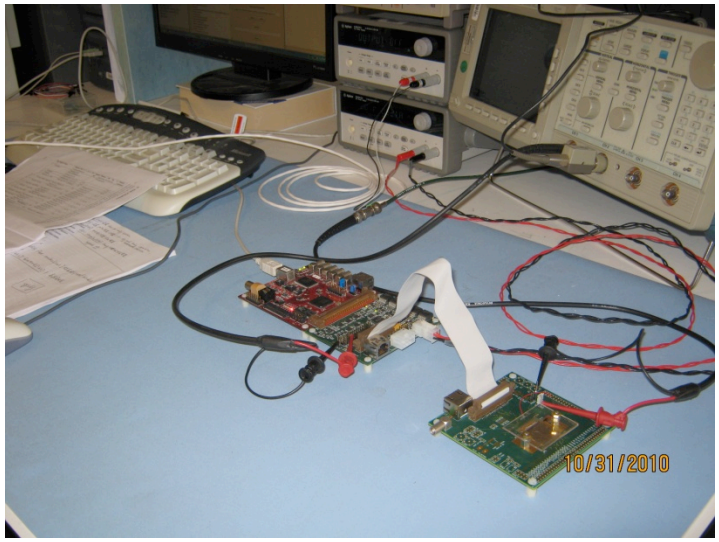
Test system overview



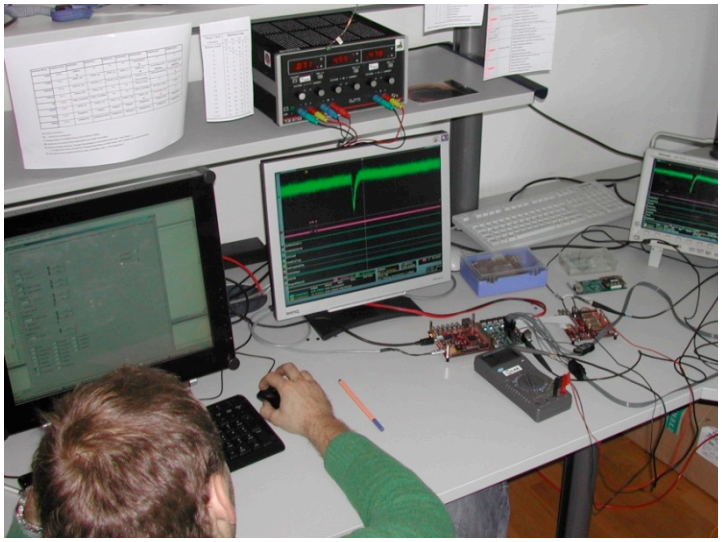
Tektronix DG2020A
based @ LBNL
←

ATCA
@
SLAC
→

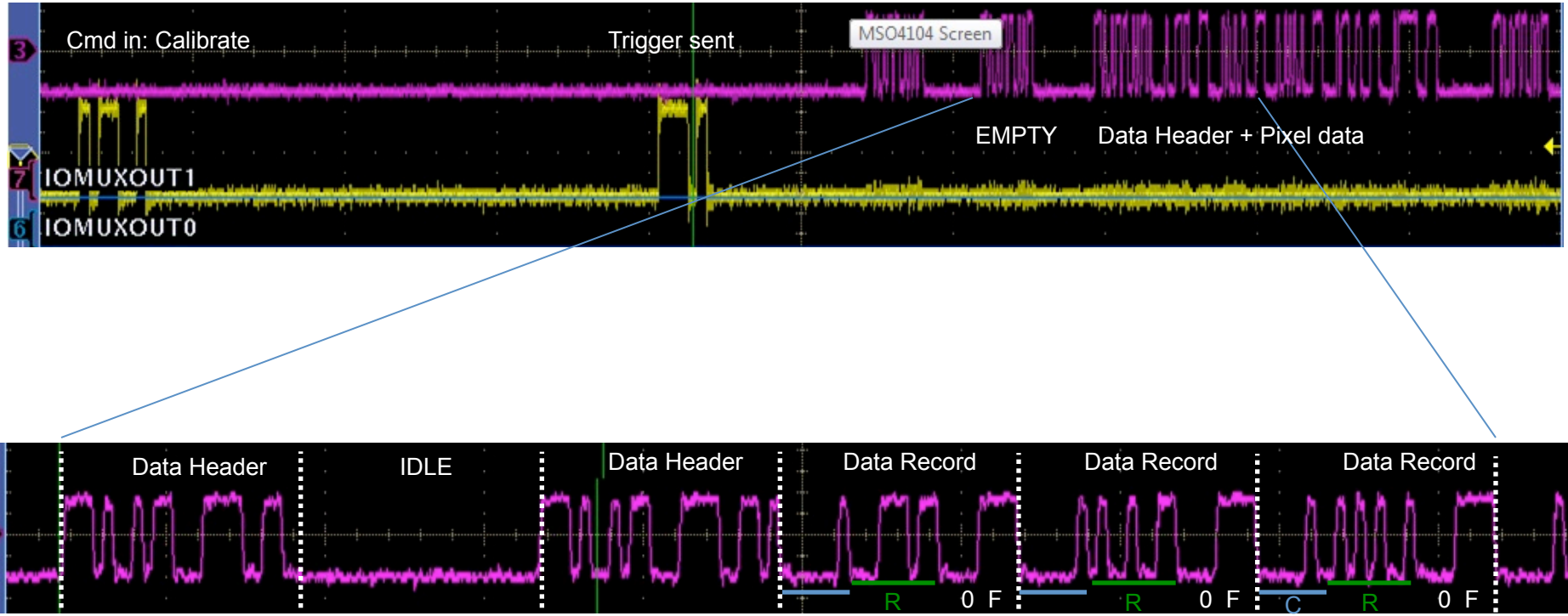




USBpix
@
←LBNL | Bonn →

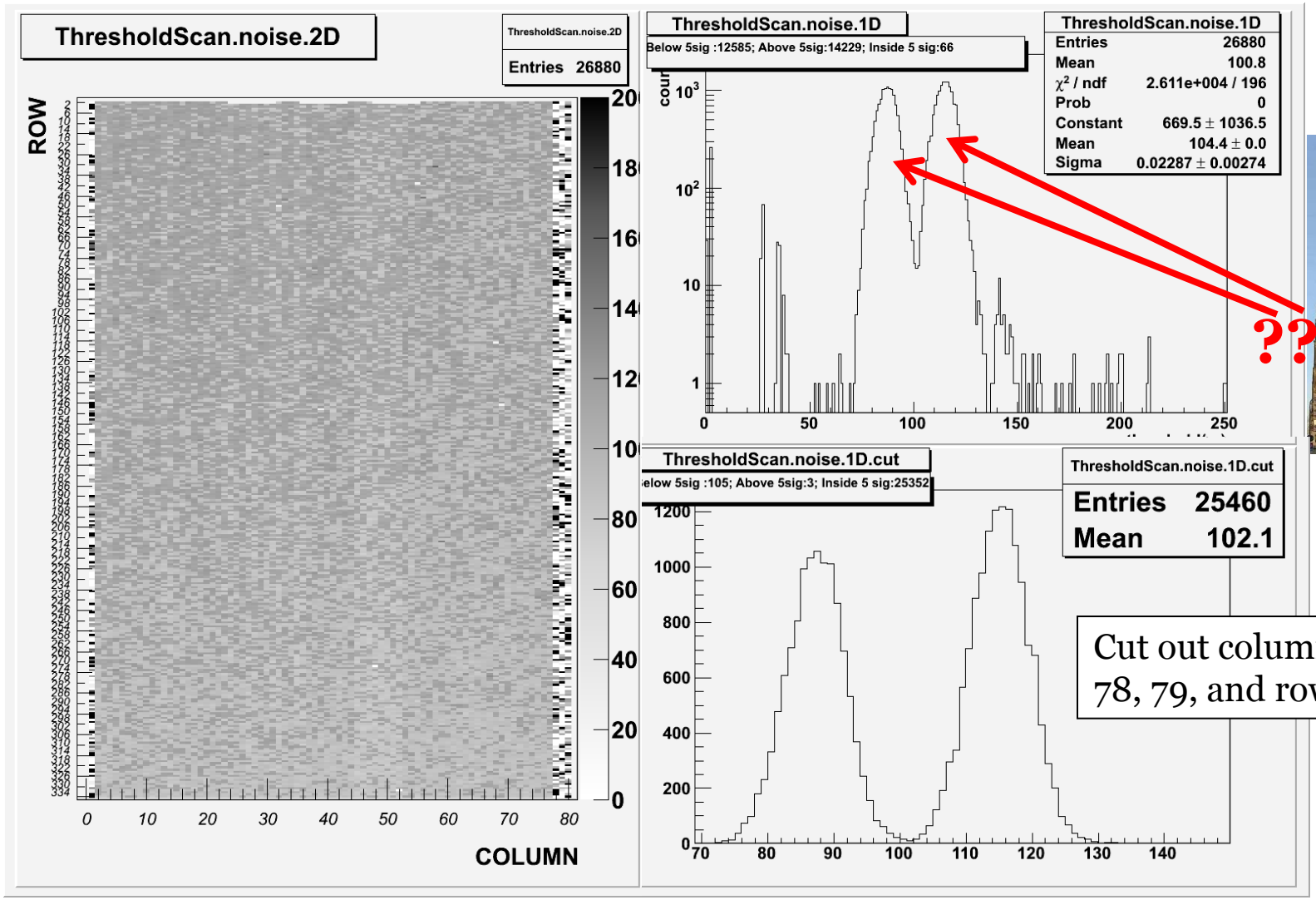


Digital injection



- Inject hit **after** analog pixel (digital injection) to selected pixel, send trigger cmd
- Data output looks as expected
- Raw data file looks fine (example on next slide…)

IC #6 noise distribution (reminder)



Cut out columns 0, 77, 78, 79, and row 0

Studying Double-Peak effect

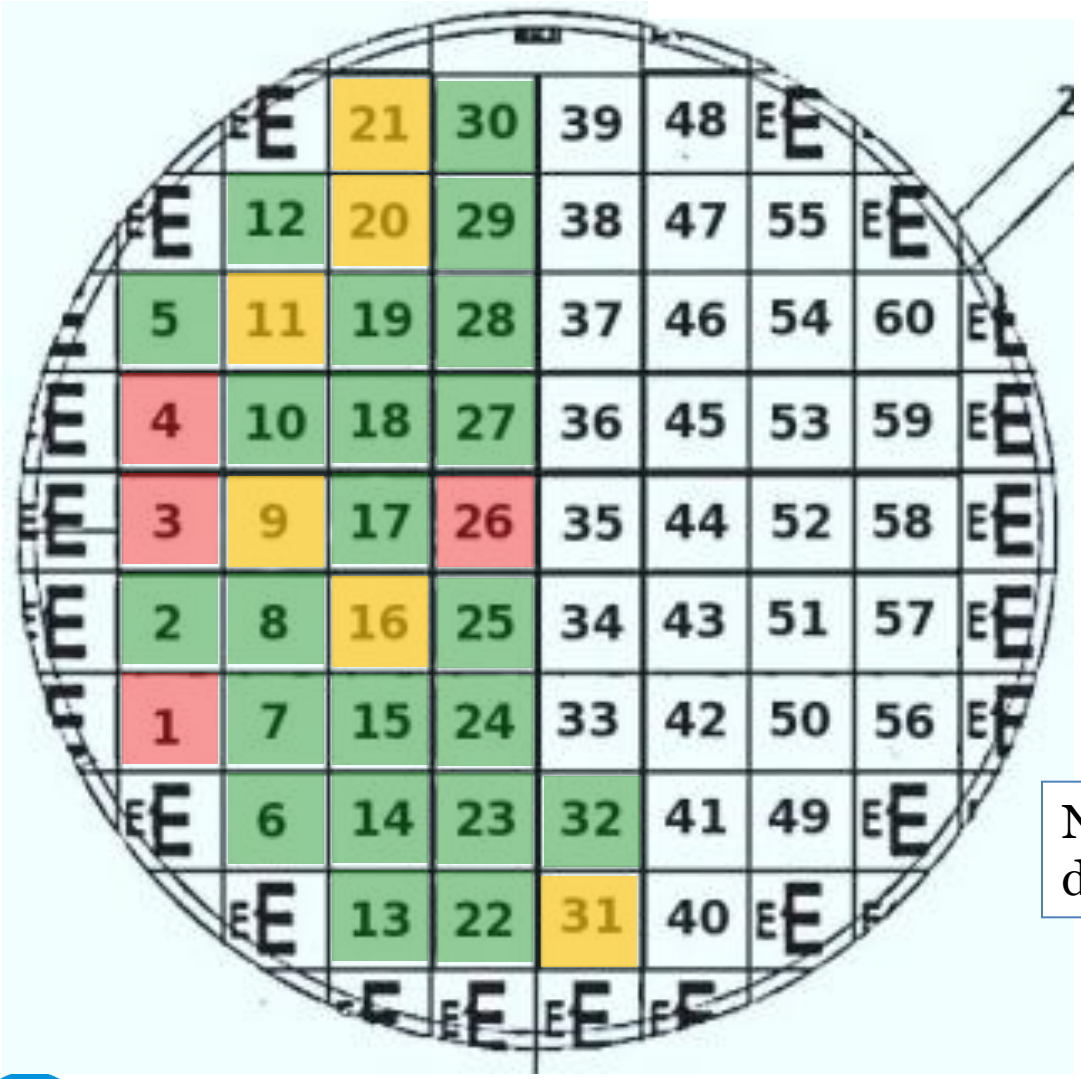
We have tried two different options to study double peak (Kölner Dom) effect.

- Option 1: Varying the "DAC8SPARE4" value to decrease VCAL DAC step. This changes the X axis scale of the s-curve.

- Option 2: Change of the fitting function. Using native ROOT s-curve (error function).

IC tested on wafer AWN6TUH

PRELIMINARY



: IC w. small number of defects.

: IC broken, can not be operated.

: IC with >= 1DC showing defects

No threshold distribution / noise distribution cut applied so far

Details

IC 21: 2 DCs have problems

IC 20: 1 DC broken. Column 53+ problematic

IC 11: 2 DCs broken

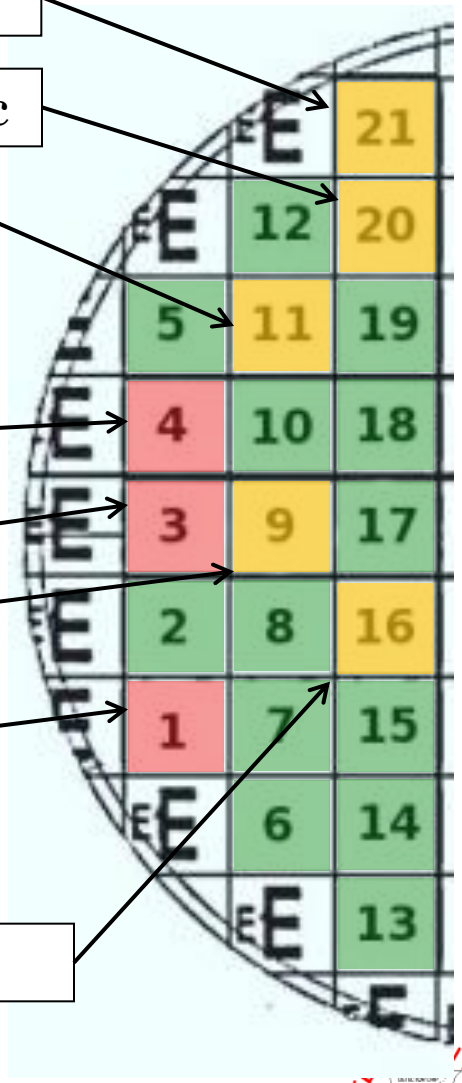
IC 04: Lots of activity. FE hangs

IC 03: DC(s?) problematic (injection?), noise 250e-

IC 09: DC(s?) problematic (injection?)

IC 01: No power discriminator

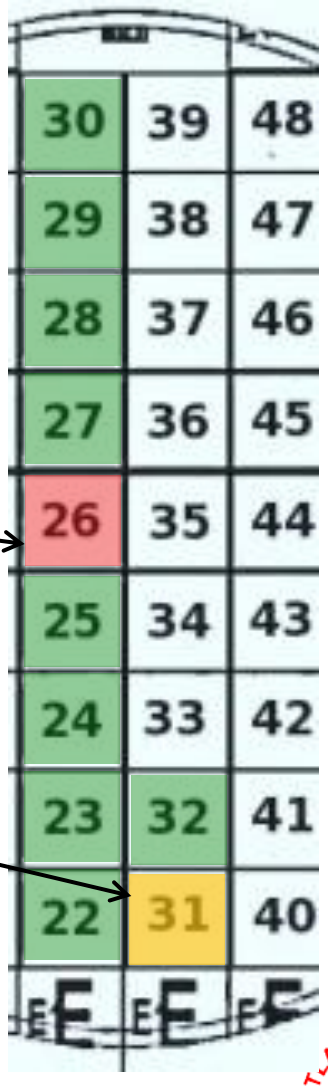
IC 16: 1 DC broken



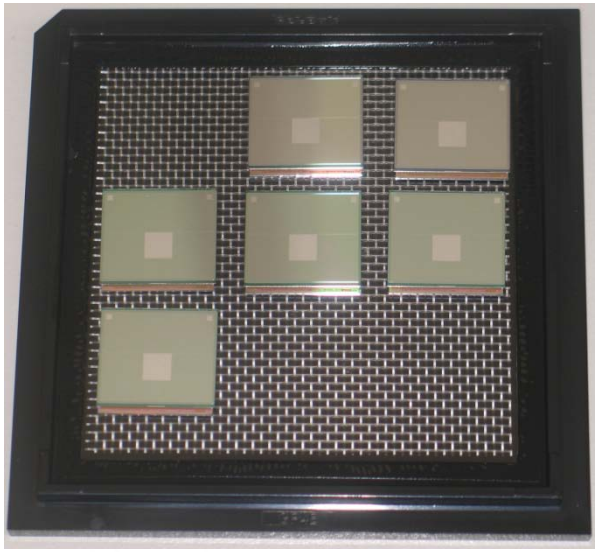
Details

IC 26: Lots of activity. FE hangs

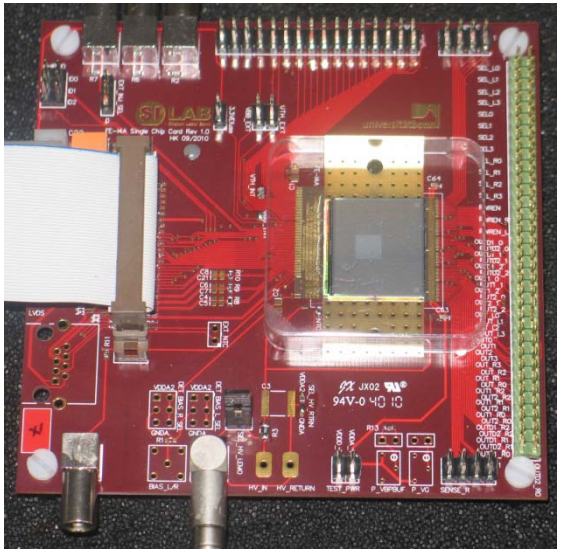
IC 31: Some double-counts with digital inject



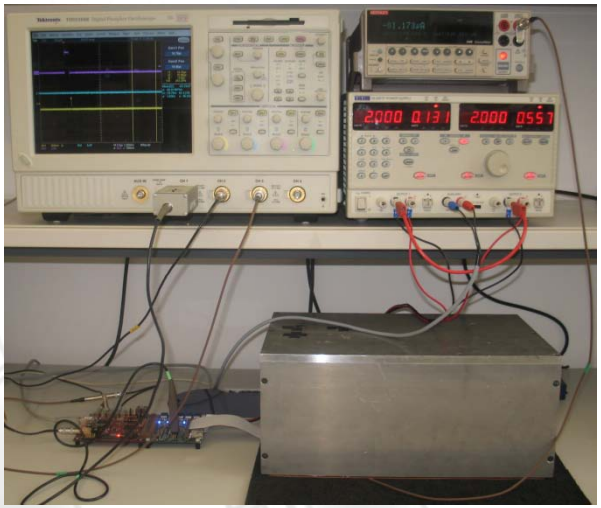
Some pictures



FE-I4 assemblies



Module one on SCC

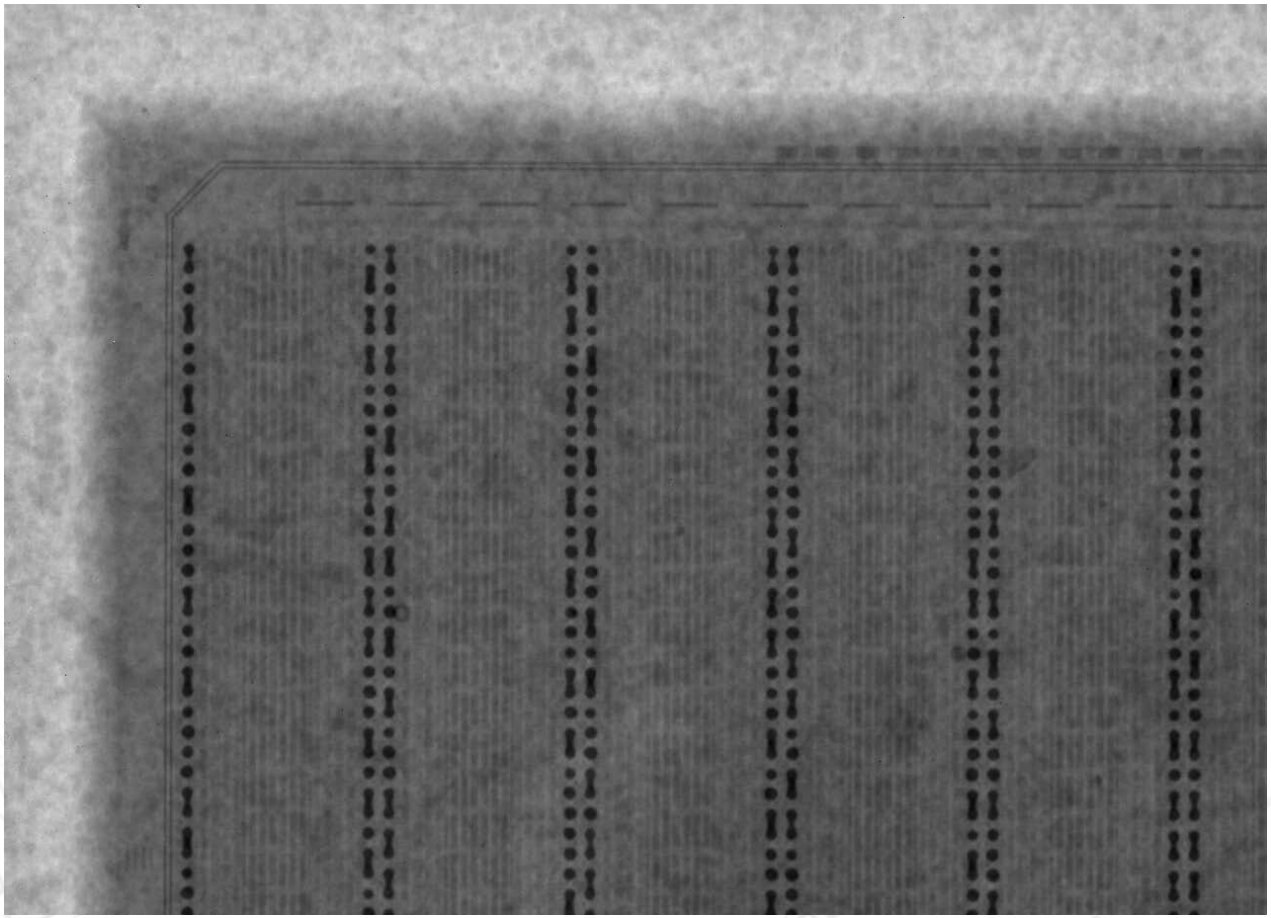


Test setup in Bonn

Tests started today, so all results very PRELIMINARY

Module 1 - bumps

- …we chose a module with a lot of shorted bumps to learn handling it.



- Problems with analog pixels expected, but still a lot of good bumps.

FE-I4 tests and committments

1) SR read back tests - Bonn, SLAC

2) Efuse programming . - LBNL

3) Shuldo operation. Powering chip through Shuldos. Also Shuldos used as standard LDO. -Bonn

4) DC-DC operation. Powering digital or analog through DC-DC. - LBNL

5) Temperature dependence of threshold. Different VTH generation options and temperature

dependence of each. - LBNL

6) Stop mode operation. Tests of region memory. Fill all 5 memories, test all latency values. -

Bonn

7) Measure digital current as a function of memory occupancy -Bonn

*** 8) Timewalk measrements vs. front end bias settings. Timewalk dispersion over array. Small

hit recovery vs. digital threhsold settings.

9) Implement monleak scan (needs external instrument).- Goettingen

10) Characterize all bias DACs over their full range. - LBNL

11) Study PLL. Regenerated clock vs raw clock coming from BPM decoder -Bonn

12) Low threshold characterization . - will be done by everyone testing sensors

13) Chip threshold tuning with TDACs. -Goettingen

14) Usage of alternative SR. -SLAC

*** 15) CPPM columns.

*** 16) Self triggering mode. Self trigger scan

*** 17) Service records.

*** 18) Analug muxes at the to of the chip

19) Better characterization of pulser. -SLAC

20) Power supply rejection ratio. -NIKHEF

21) Fully exercise and validate scan chanis. -NIKHEF

*** 22) Analog power vs. performance

23) Determine external TDACVbp resistor value - LBNL

*** 24) Precision comparison of threshold dispersion and noise between VNCAP columns and

nominal columns. Is there any change with temperature ?

25) Collect all wafer probing functionality into single software - Goettingen

26) Measure limits of operating frequency and voltage. Where do things stop working? - NIKHEF

Hardware update

- Adapter cards:
  40 new FE-I4 adapter cards arrived.
  - need to be calibrated, tested, numbered, …

  → shipping will start in next days.

- Single Chip Cards:
  4 from CERN production, 20 from Bonn production.

- Bare ICs:
  - Bonn: 2 on SCC
  - LBNL: 2 on SCC, 1 on „Abder‘s PCB“
  - SLAC: 1 on SCC
  - Göttingen: 1 on SCC
  - Stony Brook: 1 on SCC
  - Los Alamos: 3 on SCC

  Information are updated on:
  „http://icwiki.physik.uni-bonn.de/twiki/bin/view/Systems/USBpixTables

- Assemblies:
  The first FE-I4 assembly mounted on SCC and wire bonded in Bonn. Tests ongoing, see this talk.